EMI Associated with Inter-Board Connections for Module-on-Backplane and Stacked-Card Configurations

Xiaoning Ye
Electromagnetic Compatibility Laboratory
University of Missouri - Rolla
Email: xiaoning@umr.edu

I. Introduction

The module-on-backplane and stacked-card are both common configurations in high-speed digital designs. A typical module-on-backplane or stacked-card structure is of appreciable electrical extent, and functions as an EMI antenna at several hundred MHz. Three issues to be considered for understanding EMI related to inter-board connection include the connection itself, the signal routing on the PCBs, and the radiating EMI antenna. In this work, the signal routing on the PCBs is omitted. The FDTD method was utilized to model this problem because of the capability for analyzing multiple frequencies with a single time-domain simulation, and further, FDTD is well-suited for low loss cases with rectilinear geometries.

II. Problem Description

Three testfixtures including both the module-on-backplane and stacked-card configurations were built for study. Each testfixtue included a mother-board, a daughter-board, a inter-PCB connection between two boards, and a piece of semi-rigid cable attached to the mother-board. Common-mode current on the attached cable was measured. The FDTD method was applied and modeled results were compared to the measurements. The general setup of the three measurements is similar. A demnonstration of the setup with the module-on-backplane configuration is shown in Figure 1. The signal was fed from Port 1 of the HP 8753D Network Analyzer, through the 20 cm long semi-rigid cable which was soldered to the ground plane of the mother-board, then through the connection and shorted to the ground plane of the daughter-board. Two AWG 24 wires were used to mimic the right-angle connector, one as the signal pin and the other as the signal return. A Fischer F-2000 clamp-on current probe was placed around the semi-rigid cable and |S21| was measured. The 60 cm x 60 cm aluminum plate was used to separate the test fixture from the network analyzer and connecting cables to enhance the repeatability of the experiment.The probe response was compensated for in the calibration procedureThe three cases studied are:

1. The module-on-backplane configuration with a one-signal-one-return conneciton.
2. The stacked-card configuration with a one-signal-one-return connection.
3. The stacked-card configuration with a one-signal-six-return connection.

Which are shown in Figures 2, 3, and 4, respectively.

The cell size in the FDTD modeling for the module-on-backplane configuration was 10 mm x 4 mm x 5 mm and the time step was 8.285004e-12 s. With this approach, the largest cell size dimension (10 mm) was oriented along the longest board dimension, and the total cell number including the perfect matched layers was minimized to around 380,000 cells. The white space placed at each direction was 7 cells. The aluminum plate was modeled as an infinite ground plane. The computing time was reduced when Prony's or the GPOF method was applied.

FDTD method with a finer mesh was used to model the two stacked-card configurations and the reults will be shown in Section III.

III. Results and Discussion

Measurements and modeled results for the three cases described in Section II are shown in Figures 5, 6, and 7, respectively. The discrepancies may be due in part to:

- The dielectric layer of the PCBs was not included in the modeling,
- The finite aluminum plate was modeled as an infinite ground plane, and
- Measurement errors.

Acknowledgement:

This work was supported in part by AMP, Inc. through the UMR EMC Consortium.

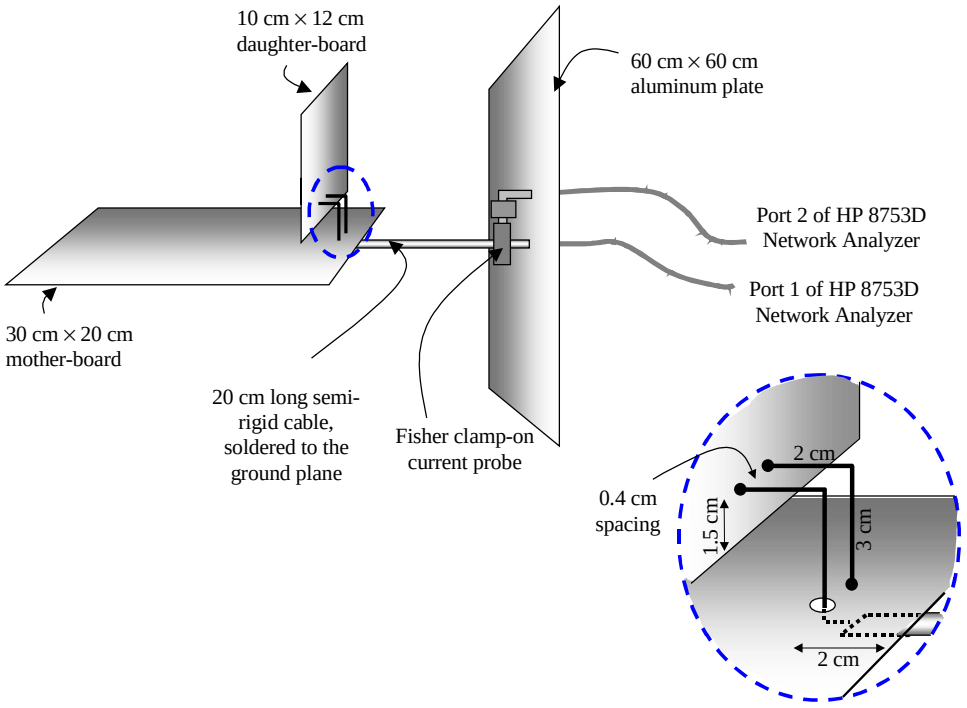

Figure 1. Experimental setup of the study of EMI associated with inter-board connection for the module-on-backplane configurations.

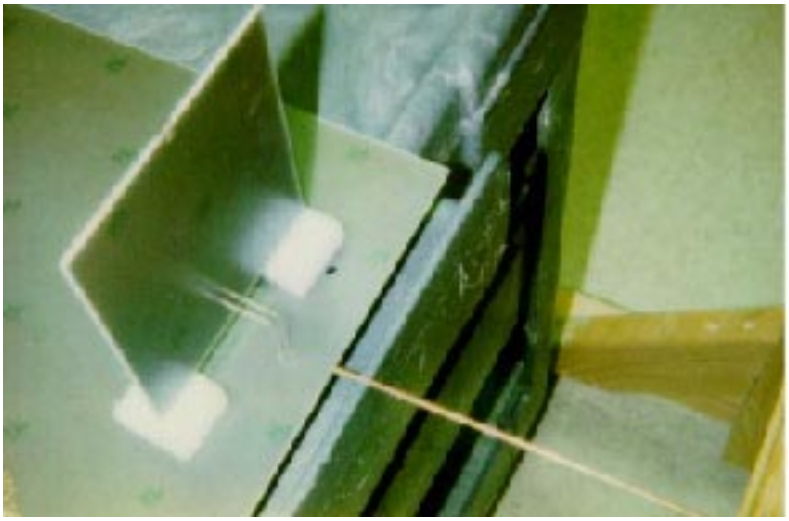

Figure 2. Picture of the setup at the inter-board connection area for the module on backplane configuration.

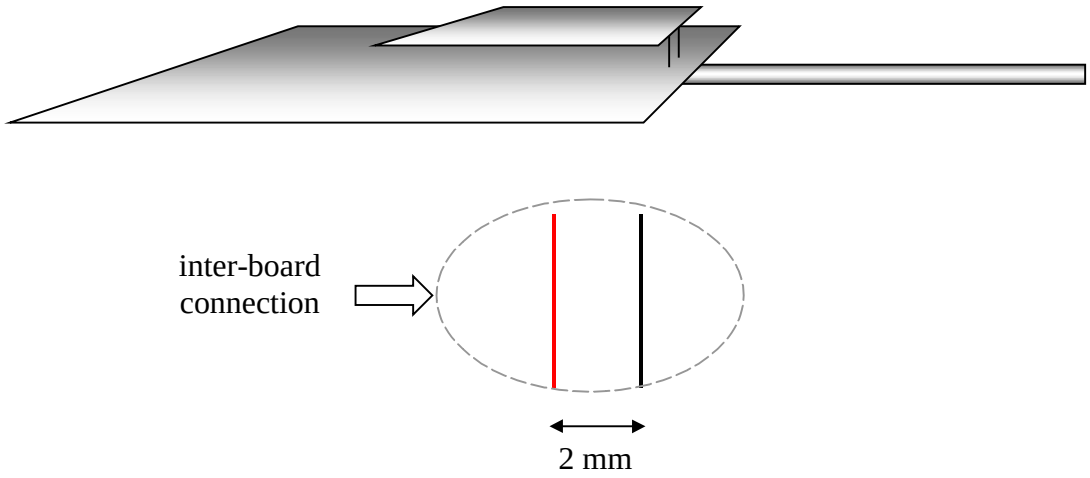

Figure 3. The stacked-card configuration with one-signal-one-return inter-PCB connection. (red indicates the signal pin, black the return)

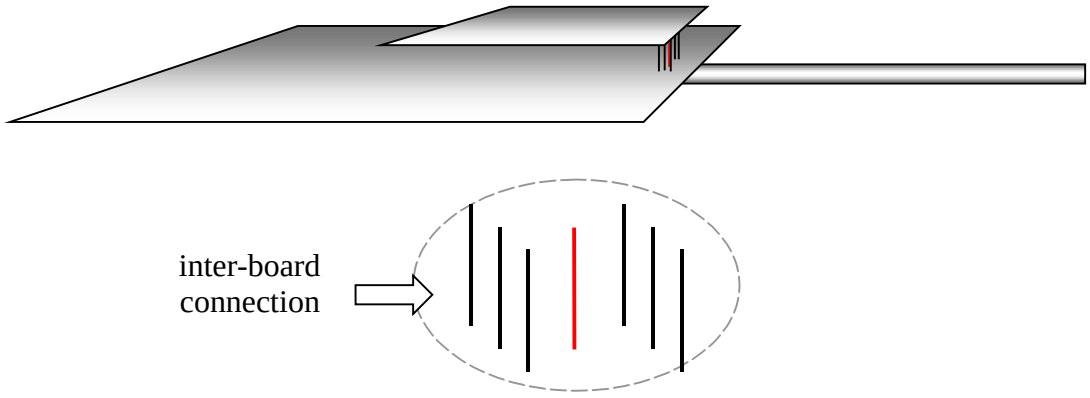

Figure 4. The stacked-card configuration with one-signal-six-return inter-PCB connection. (red indicates the signal pin, black the return)

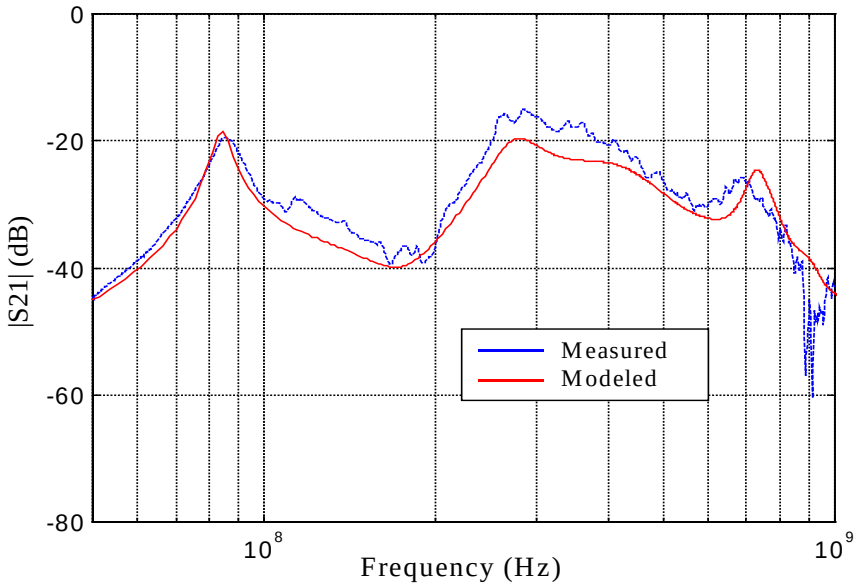

Figure 5. Measured and modeled common-mode current on the attached cable for the module-on-backplane configuration.

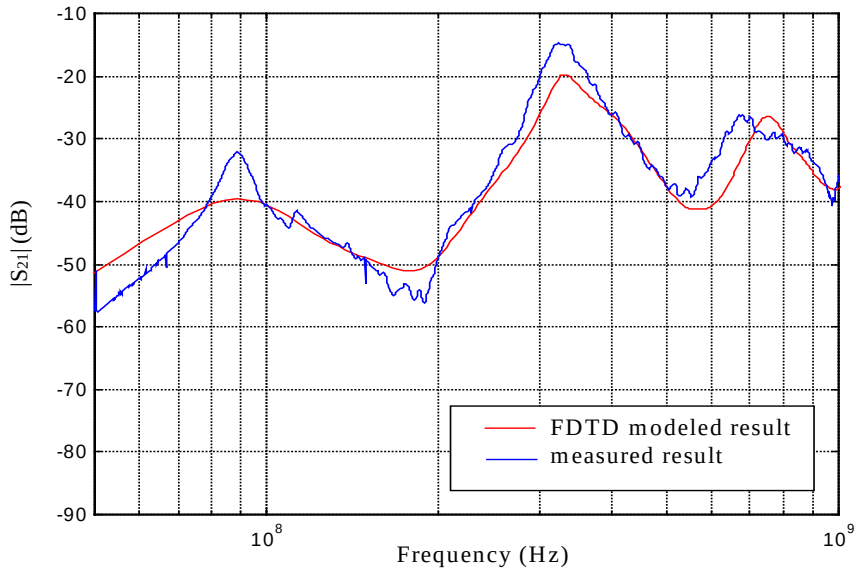

Figure 6. Measured and modeled common-mode current on the attached cable for the stacked-card configuration with a one-signal-one-return connection.

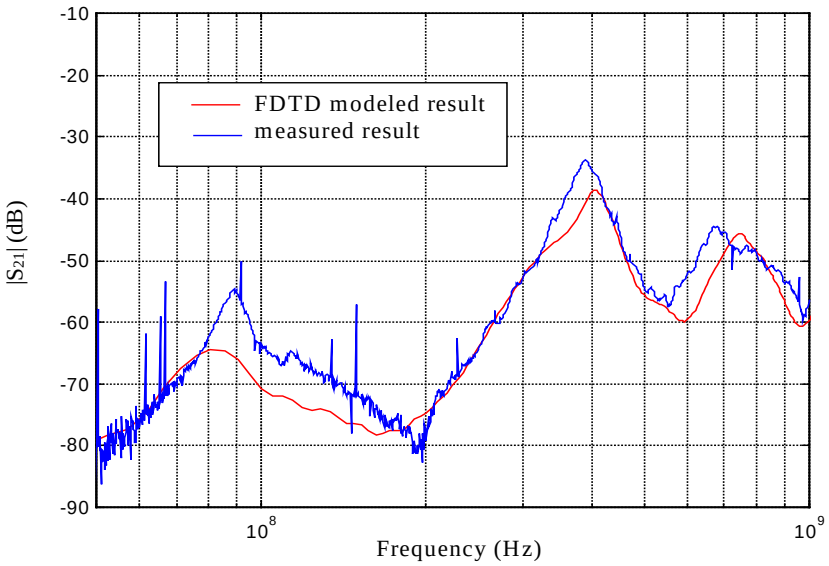

Figure 7. Measured and modeled common-mode current on the attached cable for the stacked-card configuration with a one-signal-six-return connection.