A Proposed Set of Specific Standard EMC Problems To Help Engineers Evaluate EMC Modeling Tools

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INTRODUCTION

As the complexity of high-speed electronic system packages increase, engineers and designers are required to take control of more and more aspects of electrical and mechanical engineering early in the design cycle.
In order to achieve the objective of faster time-to-market and to be cost effective one needs to be able to predict the electromagnetic radiated emission noises of the system design by using full-wave simulation tools. Modifications and improvements of the design can be easily tested with simulators to reach the best possible compromise between EMC requirements and cost/thermal/etc considerations.

Electromagnetic compatibility regulations, CISPR, FCC, and VDE, for example, require costly testing on electronic products for acceptable levels of electromagnetic emissions. The cost of building a prototype for EMC testing and the subsequent engineering modifications for compliance is very expensive and time-consuming and can be reduced through full-wave simulation software that can accurately predict the electromagnetic radiated emissions.

There are several software tools available today that use advanced numerical methods to perform full wave analysis of the system. These tools not only differ in terms of computational techniques (with their associated strengths and limitations) but also due to the source/component modeling techniques and near/far field data post-processing methods.

The key contribution of this work is to provide a collection of a set of four standard problems faced by any typical system designer and example solutions from different tools by different users. The proposed standard problems include a power/ground plane decoupling problem, a printed circuit board with a microstrip trace which runs over a split in the ground-reference plane, a heatsink emissions problem, and a shielding effectiveness problem. In this paper, each of these problems will be described, and an example result provided. A more complete set of results for each problem is available on the joint IEEE/EMC TC9 and ACES Model Validation Web site (www.emcs.org/tc9).

STANDARD PROBLEM #1
DECOUPLING POWER/GROUND PLANE
PROBLEM DEFINITION

The proper decoupling of Power/Ground planes is important to both EMC and signal integrity applications. This problem defines a realistic-sized PC board, with capacitors distributed across the entire board. The specifications are given below and a diagram is provided in Figure 1. Due to space restrictions in this paper, all example results are shown in the individual reports on each Standard Problem, available on the Joint Model Validation web site.

General Board Description: 4 layer board with 2 solid planes in inner layers, solid planes are separated by 40 mils dielectric FR4 (relative dielectric constant = 4.5)
Plane size: 10” x 12”
Capacitors: 96 capacitors evenly spaced 1” apart, include 30 mohms series resistance and 2 nH series inductance
Source: Located in center of board, 1 volt sinewave, frequency scanned from
10 –1000 MHz
Figure-of-merit: Voltage at output #1, #2, and #3, relative to input voltage

Compare the results for the following cases:

1. Board with no capacitors
2. Board with four capacitors only around source
3. Board with fully loaded 95 capacitors
4. Use capacitor values of 0.01 uF, 0.1 uF and 100 pF

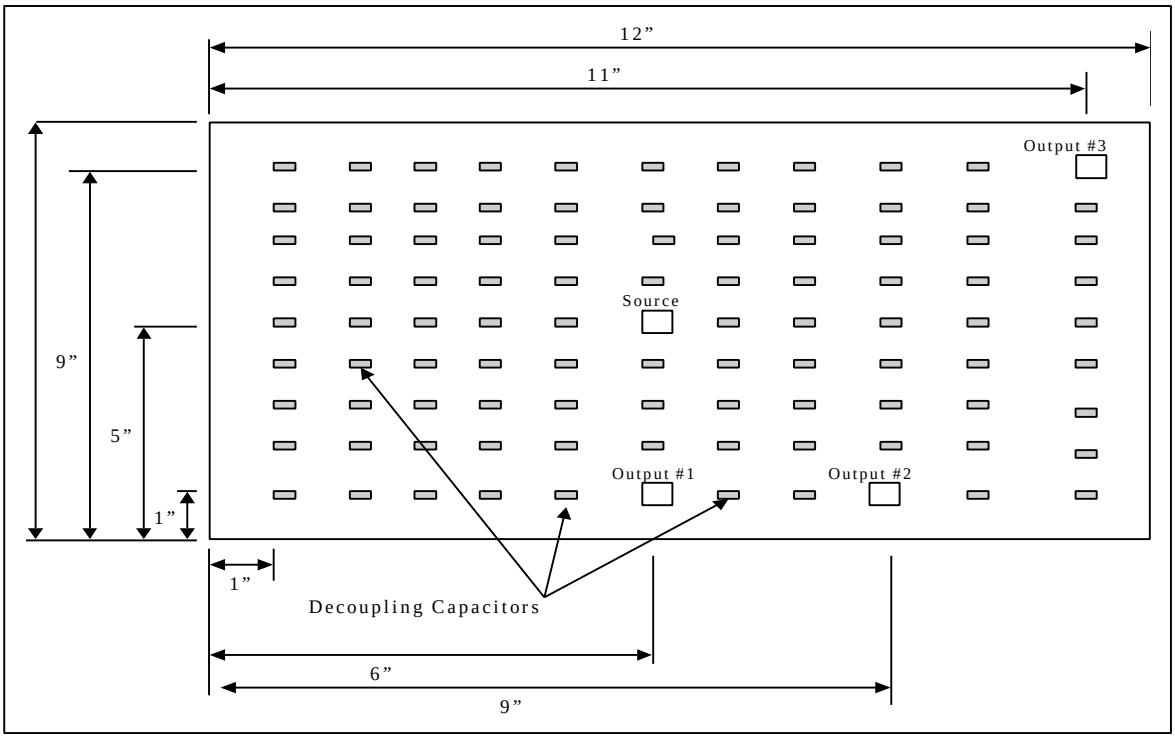

Figure 1 Decoupling Capacitor Standard Problem Geometry

STANDARD PROBLEM #2
TRACE-OVER-SPLIT-IN-GROUND-PLANE
PROBLEM DEFINITION

The emissions from a PC board where a trace is run over a split in the ground-reference plan is due to a complex interaction of the return current ‘loop’ in the ground-reference plane, and the extra ‘bunching’ of return current near the edge of the ground-reference plane These effects result in an increase of radiated emissions, and a negative EMC impact. The problem described below (and illustrated in Figure 2) compares the radiation levels with and without plane splits, as well as the effect of (realistic) stitching capacitors. Due to space restrictions in this paper, all example results are shown in the individual reports on each Standard Problem, available on the Joint Model Validation web site.

Plane size: 10” x 12”
Trace: 5-mil wide, 10” long, 5 mils above the plane, center or close upper edge; dielectric material is FR4.
Slot: 8” long, 20-mil wide, center
Stitching cap: 0.1 uF/470 pF, consider 2 nH/1.88 nH connection inductance and 0.5 ohm parasitic resistance in serial, place right next to the trace.
Source: 3.3 volts spread spectrum source from 100 MHz to 2 GHz, 50 ohms source/load termination.
Figure-of-merit: percentage of power radiated into free space, or maximum E field 3m away at 100MHz-2GHz range.

Compare the results for the following cases:

1. Board without slot, trace in the middle
2. Add slot to plane
3 .Move trace to board edge
4. Add 0.1 uF cap close to trace
5. Replace 0.1uF cap with 470 pF cap

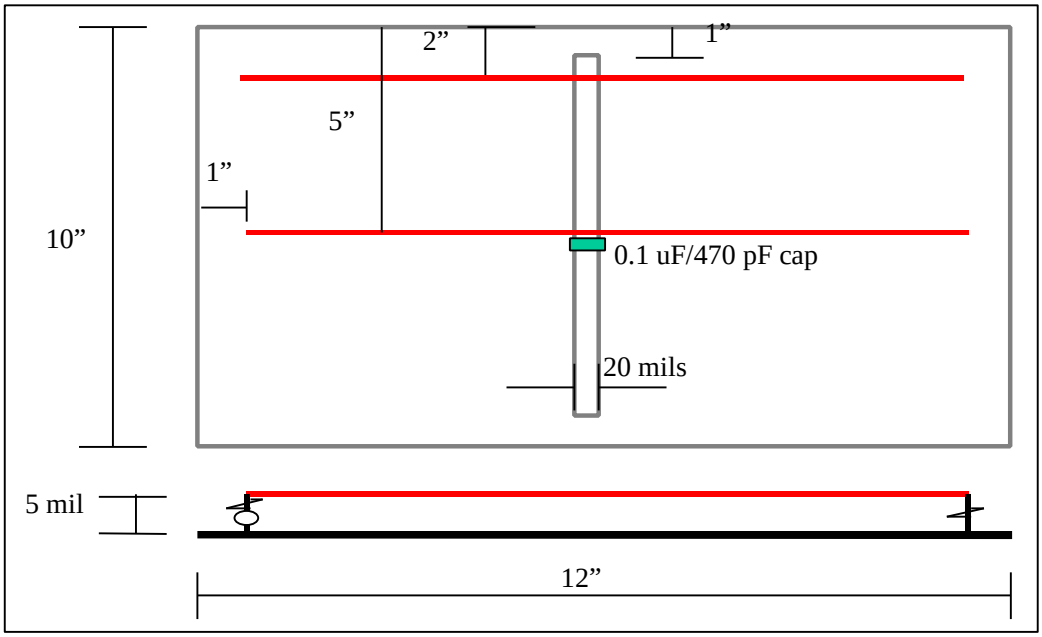

Figure 2 Trace over Split Plane Standard Problem Geometry

STANDARD PROBLEM #3
HEATSINK PROBLEM DEFINITION

Containing emissions from heat sinks on high power microelectronics is rapidly becoming a necessity caused by higher power levels and faster clocking of digital circuits. The expectation of the microelectronics industry not to deviate from Moore's law is driving microprocessors requiring power levels in the 10s of watts and clock frequencies well into the microwave region. As a result, EMC engineers must no longer determine *if* heat sinks must be grounded but *how many* ground points must be used and where they should be located. This problem uses a standard size heatsink for a commonly used processor. The geometry is shown in Figures 3 and 4. Due to space restrictions in this paper, all example results are shown in the individual reports on each Standard Problem, available on the Joint Model Validation web site.

Heatsink Size: conducting block measuring 88.9 mm (3.5 in.) long, 63.5 mm (2.5 in.) wide and 38.1 mm (1.5 in.) high.
Heatsink Location: The conducting block was located in the center of the simulation region, 6.0 mm (0.2362 in.) above a perfect electrical conducting (PEC) ground plane.
Ground Plane Size: 160 x 120 mm (6.290 x 4.740 in.).
Source Location: The heat sink was excited by a vertical source extending form the ground plane to the base of the heat sink and was offset 12.7 mm (0.5 in.) in the x and y directions from the center of the heat sink. (An offset source was chosen so that both even and odd modes would be excited.)
Grounding Posts: The heat sink was connected to the ground plane through 6mm (0.2362 in.) square legs. Different grounding configurations were chosen as shown in Figure 4.

We have introduced a figure of merit called "advantage" to facilitate comparison of results generated using different sources. We define "advantage" as the difference between a reference (no ground posts) and trial case expressed in decibels. For example, a given simulation of a heat sink having no ground points produces a maximum radiated field, "A". After adding ground points, the simulation produces a maximum radiated field 30 dB below "A". We refer to the reduced emissions at that frequency as a 30 dB advantage, viz.,

Advantage (dB) = reference (dB) – trial (dB)

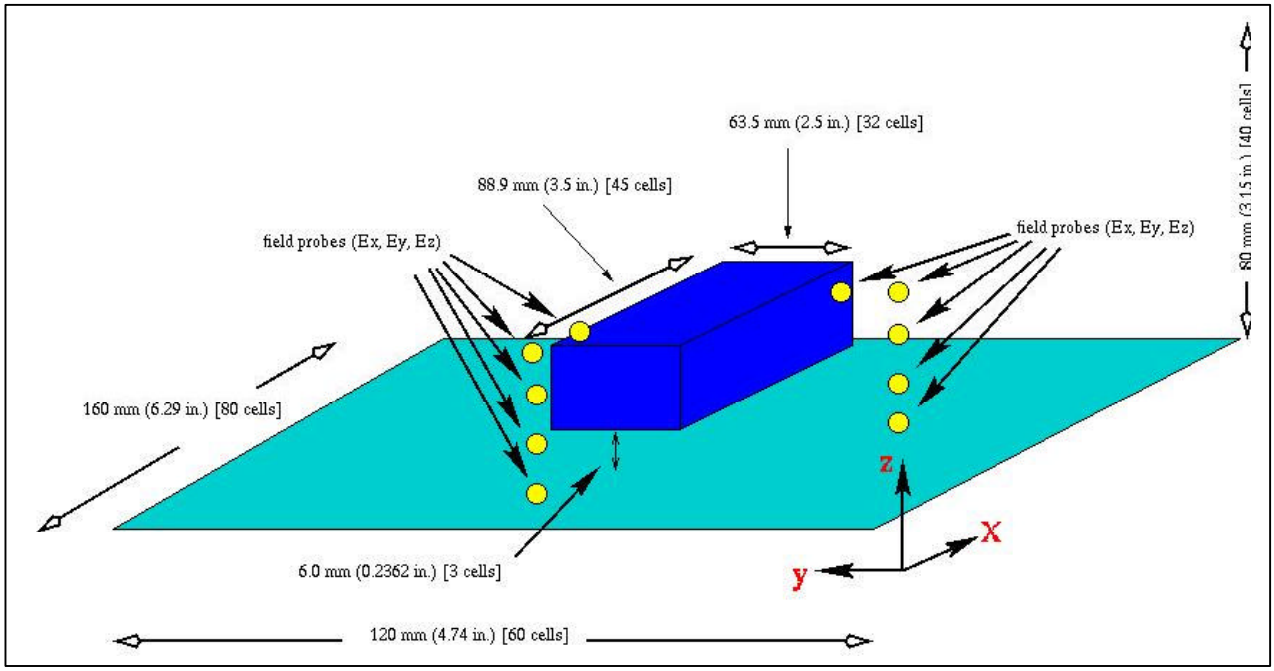

Figure 3 Heatsink Standard Problem Geometry

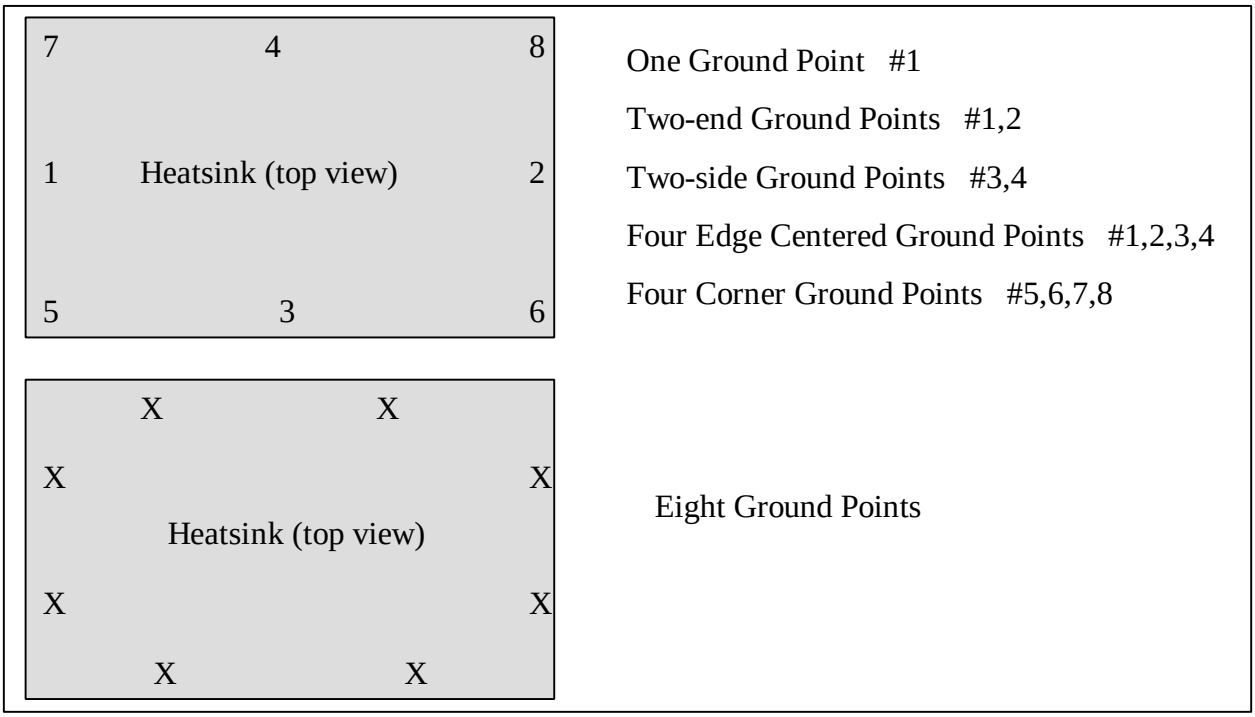

Figure 4 Heatsink Ground Posts Standard Problem Geometry

STANDARD PROBLEM #4
SHIELDED ENCLOSURE PROBLEM DEFINITION

Shielding effectiveness of an enclosure is a complex matter, in which a lot of different phenomena are involved, for example, electrical and geometrical parameters of the material of the walls, apertures and grids, joints and contacts (connections) (including the use of gaskets, springs, overlaps,…), internal and external cabling and cable feed-through or connectors, and internal boards and backpanels. In most cases, the total shielding effectiveness is determined by the combination of all these effects, some with greater impact than others. As a consequence, determining the shielding effectiveness of a real enclosure is not at all a simple matter. For this problem, a complex metal enclosure has been defined, and is shown in Figure 5. This enclosure includes an internal source, and apertures with different holes sizes. Due to space restrictions in this paper, all example results are shown in the individual reports on each Standard Problem, available on the Joint Model Validation web site.

Enclosure Dimension: 37cm x 30cm x 9cm ; All enclosure walls are made up of perfect electric conductor.

Aperture Dimension: a big hole of 8cm*6cm, the small holes are 0.2cm*0.2cm, and the spacing between each small hole is 0.2cm. There are 4 rows and 17 columns of these small holes.

Source Location: A metal plane (26 cm x 28 cm) representing the PCB reference plane and the trace over a dielectric (FR4) bed (thickness: 0.0127cm) driven by constant amplitude harmonic excitations. Plane is 1cm away from the slotted panel and 1cm above the bottom enclosure wall. Trace is centered in the plane perpendicular to the slotted panel. A heatsink (metal plate) of 16cm x 10 cm is placed 0.5 cm above the reference plane covering the trace.

Source Definition: A 3.3 volts spread spectrum source from 500 MHz to 2 GHz, 50 ohms source/load termination.

Compare the results for the following cases:
(a) With no Shield
(b) with small holes and big hole
(c) with small holes only
(d) with large hole only

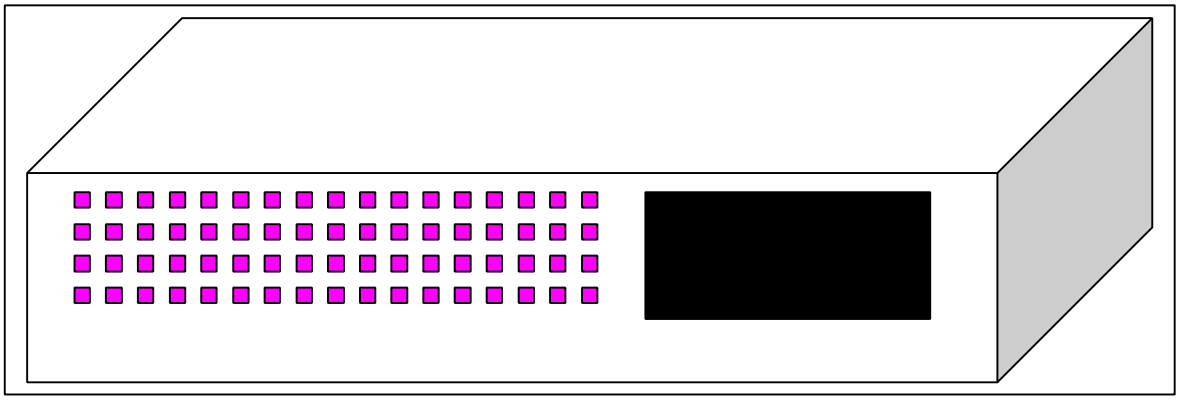

Figure 5 Shielding Effectiveness Standard Problem Geometry

NUMERICAL MODELING TOOLS AND TECHNIQUES

To help evaluate each of these proposed standard problems, each of the problems was analyzed with different software tools, and including different numerical modeling techniques. As mentioned earlier, the results from all the various tools and techniques are available on the Model Validation web page.

Overall, the Finite-Difference Time-Domain (FDTD) technique, the Method of Moments

(MoM), the Finite Element Method (FEM), and the Transmission Line Method (TLM) was used against these standard problems to provide a good cross section of results without any standard problem being specially designed to 'fit' a given modeling technique.

Three separate FDTD tools were used: EZ-EMC distributed by EMS-PLUS, Ocotillo FDTD distributed by Ocotillo ElectroMagnetics Inc. and an FDTD code developed at the University of Missouri at Rolla.

Two method of moments codes were used: EMSIM is an internally developed code at IBM and COMORAN is distributed by INCASES).

One finite element method was used: HFSS is distributed by ANSOFT.

The TLM method (Transmission line modeling) tool was used: Micro-Stripes(tm) 3D Electromagnetic Simulator is distributed by Flomerics.

SUMMARY

A set of standard modeling problems and some example results has been presented. The intention of these standard problems is to provide engineers with straightforward, well-defined, and reasonable real-world problems that can then be used to evaluate other modeling software and/or other numerical techniques. It is hoped that others will use these problems (when appropriate) to evaluate possible vendor software, and be able to compare the results from the software-in-question to the results here, to gain confidence in the results of the tool under investigation. A more complete report of the results from the modeling activities of this standard modeling problem, and other standard modeling problems, can be found on a joint IEEE/EMC TC-9 and ACES Modeling Validation web site (www.emcs.org/tc9).