



IEEE Crosstalk



The Newsletter of the Mid-Hudson Section of the IEEE

Volume XLVI, No 6, November 2007

Chairman's Corner

This is definitely the season for giving thanks for all the wonderful, hard-working volunteers in the Mid-Hudson Section. The Section has held four events so far and we have one more very exciting event planned for December.

October had two technical events: thanks to Mike Spector, our new PES Chairman, for organizing an excellent and informative talk and tour of the Sturgeon Pool Dam pinning. There was a good turnout and even the weather cooperated! The second October event was an awe-inspiring tour of two simulation centers at West Point, thanks to the Education Society Chair, LTC Rob Kewley. Unfortunately, turnout was light, which meant that a lot of people missed out on some very impressive virtual reality displays and test-firing a variety of real weapons in an indoor range (firing laser beams instead of bullets). Army training has come a long way!

November started with our 4th annual SUNY/IEEE Workshop masterminded by Casimer DeCusatis. This year's topic was Engineering Education, focusing on pre-college education to help shape the workforce for the next 30 years. Casimer is tireless in organizing these events, from developing the agenda to gathering qualified and interesting speakers, to arranging for CEU credits.

Finally, our December event is the first International Electron Devices Mini-Colloquium to be held at IBM East Fishkill. There are full details including a program and speaker bios and abstracts on pages 2-10 of this newsletter, but I would like to **congratulate** one of the principal organizers, **Fernando Guarin, on becoming an IEEE Fellow!** The elevation is effective January 1st and is for "*contributions to semiconductor materials and reliability*" Fernando joins an elite group - fewer than 0.1% of IEEE members are elevated each year. There are only 11 fellows and 11 life fellows in the Mid-Hudson section, out of 900+ members. I would be remiss if I didn't also mention that Casimer DeCusatis is one of those 11 fellows.

Finally, we will hold elections in December. The details are on the last page of this newsletter.

Upcoming Events

Friday, December 7th, 2007: International Electron Devices Mini-Colloquium at IBM East Fishkill from 8:15 AM to 1 PM. There is no fee, but **registration is required by Dec 4th**. To register, email Fernando Guarin (guarinf@us.ibm.com).

Mid-Hudson Section Leadership

Chair:	Lisa Shay
Immediate Past Chair:	Rob Atkins
Vice Chair:	Michael Otis
Treasurer:	David J. Dittmann II
Secretary:	Baback Izadi
Members-at-Large:	Larry Boland Bill McCarthy * opening
Program Chair:	Kwok Soohoo

Society Chairs:

Computer:	Baback Izadi
Education:	Robert Kewley
Electron Devices:	Fernando Guarin
Power:	Michael Spector
WIE Affinity Group:	Rebecca Gott
GOLD Affinity Group:	Ravi Todi

Student Activities	Robert Kewley
Membership:	Casimer M. DeCusatis
Awards Chair:	Lisa Shay
Newsletter Editor:	Brett Arteta
Associate Editor:	* opening

PACE Chair:	Larry Winkler
Publicity Chair:	* opening
Engineer's week:	* opening
Webmaster:	Larry Winkler



Mid-Hudson Section Website

<http://www.ewh.ieee.org/r1/mid-hudson/index.htm>



Mid-Hudson Section General Contact

izadi@computer.org (845) 257-3823



IEEE

**International Electron Devices
Mini-Colloquium**

Friday, December 7, 2007

8:00 AM – 1:00 PM

Building 330 Cafeteria (South end)

IBM East Fishkill

Co-Sponsored by

IEEE Mid-Hudson Section



Program

- 8:00 8:30 Continental Breakfast
- 8:30 8:40 Welcome NoteGary Patton
- 8:40 9:20 Future Gate Stack Technology
.....Hiroshi Iwai
- 9:20 10:00 Beyond Scaling – Teaching the Old Dog some
New Tricks!Subramanian S. Iyer
- 10:00 10:10 Coffee Break
- 10:10 10:50 Robust Electrostatic Discharge (ESD)
Protection in BiCMOS/CMOS Technologies
.....Juin J. Liou
- 10:50 11:30 Electroabsorption Modulator for Transparent
Analog Fiber LinkPaul K. L. Yu
- 11:30 12:10 Processing and Defect Control of Advanced Ge
DevicesCor L. Claeys
- 12:10 12:15 Closing RemarksFernando Guarin
& Ravi Todi
- 12:15 1:30 Networking and Working Lunch

Welcome

On behalf of the Electron Device chapter of the Mid-Hudson Section, we would like to welcome you to the IEEE International Electron Devices Mini-Colloquium. This colloquium is packed with wealth of knowledge and information, with five internationally recognized distinguished lecturers presenting on different fields of interest in Electron Device Society. The colloquium will provide an excellent opportunity to attendees to interact and exchange their ideas with these experts. This colloquium is also aimed at providing networking opportunity for the IEEE members and non-members in the Mid-Hudson region.

We would like to thank all the sponsors of this event that includes the IEEE Mid-Hudson Section, the Electron Device Chapter of Mid-Hudson, the IEEE Electron Devices Society, Think Friday and IBM Semiconductor Research and Development Center. We would like to thank Dr. Gary Patton and his Think Friday initiative for his support of this event.

Last but not least, we thank all the distinguished lectures for taking time out of their busy schedules to come to East-Fishkill to participate in this event.

It is again our great honor and pleasure to extend a warm welcome to everyone attending this International Electron Devices Mini-Colloquium.

Fernando Guarín
Ravi Todi

Acknowledgements

The organizers would like to thank following individuals for their help and support that made this Mini-Colloquium possible

Gary Patton
LTC Lisa A. Shay
Subramanian S. Iyer
Cor Claeys
Juin J. Liou
Paul Yu
Hiroshi Iwai

Hiroshi Iwai



Hiroshi Iwai was born in Tokyo, Japan, on April 25, 1949. He received the B.E. and Ph.D. degrees in electrical engineering from the University of Tokyo, Japan in 1972 and 1992, respectively. In 1973, he joined the Research and Development Center of Toshiba Corporation, Kawasaki, Japan, where he developed the first generation of Toshiba's NMOS LSI technology. From April of 1999 to present, he is a professor of Dept. of Advanced Applied Electronics, Interdisciplinary Graduate School of Science and Engineering, Tokyo Institute of Technology, Nagatsuta, Yokohama, Japan. Currently, he is also a professor of Frontier Collaborative Research Center and a Research Planning Officer of Strategic Research Planning Office in the institute.

Since joining Toshiba, he has developed several generations of high density static RAM's, dynamic RAM's and logic LSI's including CMOS, bipolar, and Bi-CMOS devices. He has authored and coauthored more than 200 papers. He has served on many committees of conferences and editors of journals. His awards include Local Commendation for Invention from Japan Institute of Invention and Innovation (1990, 2005), Grand Prize of Nikkei BP Technology Awards (1994), IEEE EDS Paul Rappaport Award (1994), IEICE ES Electronics Award (1998), IEEE EDS J.J.Ebers Award (2001). His current research interests are Nano CMOS and Emerging Technologies: High-k gate insulator, plasma doping, Ni salicide, RF CMOS modeling, Ge transistor, etc. Dr. Iwai is, a fellow of IEEE, a member of Electrochemical Society, a member of the Japan Society Applied Physics, a member of the Institute of Electronics, Information and Communication Engineers of Japan, and a member of the Institute of Electrical Engineers of Japan.

Future Gate Stack Technology

So far HfO₂ based gate dielectrics are being introduced to advanced logic integrated circuits from 45 nm commercial technology node, there are many issues for the high-k and metal gate stack for use for the next generation.

First of all, the current HfO₂ based oxides need intentionally grown interfacial layer in order to arrange a good interface between the silicon surface and the gate insulator, and hence to suppress the mobility degradation of the channel carrier of MOSFETs. This interfacial layer is typically made of SiO_xN_y and its typical EOT is 0.7 nm. Maybe the interfacial layer EOT could be reduced to around 0.5 nm. However, the SiO_xN_y interfacial layer will certainly prevent the total gate dielectric EOT reduction less than 0.7 nm almost impossible, and thus, direct contact of the high-k gate dielectrics with silicon would be inevitable. For the rare earth oxide material such as La₂O₃, we have already demonstrated very low interface state density of $6 \times 10^{10} \text{ cm}^{-2}$, and nice peak mobility value of more than $300 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for channel electrons. However, this is supposed to be the hydrogen or maybe even OH termination effects of the dangling bonds at the Si surface. The hydrogen and OH are supposed to be introduced moisture absorption of water with the La₂O₃ exposure to air before the gate electrode deposition. The problem for this termination is that at least the interfacial concentration of the hydrogen decreases during the anneal at higher temperature above 300°C. Thus, the interface state density increases and the mobility degrades after higher temperature. Another problem is that higher temperature anneal around at 500°C make an interfacial silicate layer grow and this silicate layer increases the EOT of the gate oxide and interface state density. It is known that higher temperature annealing in hydrogen ambient decreases the interface state density, however the interfacial silicate layer formation is a problem. Another way to improve the interfacial layer is to add

other 3rd elements, such as Al. It seems that the Al repairs the oxygen vacancy and probably annihilates the interface states. We did confirm these effects but they are not sufficiently large at this moment and process optimization or maybe quest of more effective another 3rd element is necessary.

Further solution is to insert higher k interfacial layer than that of SiO_xN_y . Using Sc_2O_3 as the interfacial layer, we have achieved good suppression of the silicate interfacial layer growth at 500°C . However, interface state density between the Sc_2O_3 and Si is still necessary to be improved at this moment.

Fermi level pinning is another important factor to be considered. Eventually, the process temperature for the high-k will goes down to $400 \sim 500^\circ\text{C}$, as the gate stack process moves from 'gate first' to 'gate last' process and the Fermi level pinning effect will become less significant. However, it cannot be ignored. Addition of the 3rd element will be again a solution.

When, the EOT value of the gate insulator becomes less than 1 nm, the channel carrier mobility degradation due to the remote Coulomb and remote roughness scattering caused by the charge and roughness at the interface of high-k gate dielectrics and gate electrode becomes very significant. Thus, good mobility cannot be obtained without improving that interface.

For the middle and long term issues for the gate stack, we have to consider that the MOSFETs structure will change from planar to 3-dimensional structure, such as FinFET. Eventually, the FinFET will changes to nanowire MOSFETs, and maybe to CNT MOSFETs. Or maybe other semiconductor substrate such as GaAs or Ge could be used. Source and drain will be changed from semiconductor to metal. In the case of metal source drain, maybe process temperature could be decreased to $300\sim 400^\circ\text{C}$, which would solve some critical issues of interfacial problems of high-k/semiconductor and high-k/metal gate. Some more details of gate stack for next 25 years will be explained.

Subramanian S. Iyer



Subramanian S. Iyer is Distinguished Engineer and Chief Technologist for the Semiconductor Research and Development Center, IBM Systems & technology Group, and is responsible for setting semiconductor technology direction. Till recently he was Director of 45nm CMOS Development. He obtained his B.Tech in Electrical Engineering at the Indian Institute of Technology, Bombay, and his M.S. and Ph.D. in Electrical Engineering at the University of California at Los Angeles. He joined the IBM T. J. Watson Research Center in 1981 and was manager of the Exploratory Structures and Devices Group till 1994, when he founded SiBond LLC to develop and manufacture Silicon-on-insulator materials. He has been with the IBM Microelectronics Division since 1997. Dr. Iyer has received two Corporate awards and four Outstanding Technical Achievement awards at IBM for the development of the Titanium Salicide process, the fabrication of the first SiGe Heterojunction Bipolar Transistor and the development of embedded DRAM technology and the development of eFUSE technology. His current technical interests and work lie in the area of 3-dimensional integration for memory sub-systems and the semiconductor roadmap at 22nm and beyond. He holds over 40 patents and has received 19 Invention Plateau awards at IBM. He received the Distinguished Alumnus award from the Indian Institute of Technology, Bombay in 2004. Dr. Iyer has authored over 150 articles in technical journals and several book chapters and co-edited a book on bonded SOI. He has served as an Adjunct Professor of Electrical Engineering at Columbia University, NY. Dr. Iyer is a Fellow of IEEE and a Distinguished Lecturer of the IEEE.

Beyond Scaling – Teaching the Old Dog some New Tricks!

While the semiconductor industry has been focused on the challenges of scaling, it has become quite apparent that one must take a broader view of delivering productivity and performance gains in this new regime of non-classical scaling. While transistor level and interconnect performance will continue to make strides through the innovative use of stress engineering, novel materials such as high k dielectrics in the front end and low k dielectrics and high conductivity interconnects in the backend, there is much more to be gained by addressing the issues of memory integration including three dimensional integration, on-chip decoupling and autonomic chip functions.

The scaling of memory poses a very significant challenge as it is quickly becoming a dominant part of the chip real estate and easily exceeds 70% of the chip area and contributes immensely to processor performance. We will examine the tradeoffs and technological and design advances that have made possible the use of embedded DRAMs to replace large blocks of SRAM and are being used extensively in network switches and high performance computing. More recently, we have been able to integrate trench based eDRAM in high performance processor technology as well and show a significant improvement in DRAM performance through a combination of process technology, DRAM architecture and circuit design. However, even with these innovations, on-chip memory is necessarily limited and it will be necessary to explore the third dimension.

While scaling and innovative new materials will continue to provide density and performance improvements to CMOS technology, a judicious use of memory technologies, the innovative use of on-chip structures such as trenches for decoupling and the innovative use of phenomena such as electromigration and 3-D integration will continue to provide huge benefits in altogether new dimensions.

Juin J. Liou



Juin J. Liou received the B.S. (honors), M.S., and Ph.D. degrees in electrical engineering from the University of Florida, Gainesville, in 1982, 1983, and 1987, respectively. In 1987, he joined the Department of Electrical and Computer Engineering at the University of Central Florida, Orlando, Florida where he is now a Professor. His current research interests are Micro/nanoelectronics computer-aided design, RF device modeling and simulation, and electrostatic discharge (ESD) protection design and simulation. Dr. Liou has filed 3 patents, and has published 6 textbooks, more than 210 journal papers, and more than 160 papers in international and national conference proceedings. He has been awarded more than \$7.0 million of research contracts and grants from federal agencies, state government, and industry, and has held consulting positions with research laboratories and companies in the United States, China, Japan, Taiwan, and Singapore.

He was awarded the UCF Distinguished Researcher Award three times (1992, 1998, 2002), UCF Research Incentive Award two times (2000, 2005), and IEEE Joseph M. Biedenbach Outstanding Educator Award in 2004 for his exemplary teaching, research, and international collaboration. His other honors include Fellow of the IEE, Trustee Chair Professor of UCF, Cao Guang-Biao Endowed Professor of Zhejiang University, China, Consultant Professor of Huazhong University of Science and Technology, Wuhan, China, Courtesy Professor of Shanghai Jiao Tong University, Shanghai, China, IEEE EDS Distinguished Lecturer, and National Science Council Distinguished Lecturer. Dr Liou is a recipient of U.S. Air Force Fellowship and National University Singapore Fellowship. Dr. Liou served as the IEEE EDS Vice-President for Regions/Chapters, IEEE EDS Treasurer and many other positions within EDS.

Robust Electrostatic Discharge (ESD) Protection in BiCMOS/CMOS Technologies

Electrostatic discharge (ESD) is a process in which a finite amount of charge is transferred from one object (i.e., human body) to the other (i.e., microchip). This process can result in a very high current passing through the microchip within a very short period of time, and more than 35% of chip damages can be attributed to such an event. As such, designing robust on-chip ESD structures to protect microchips against ESD stress is a high priority in the semiconductor industry. An overview on the ESD sources, models, and protection schemes will first be given in this talk. This is followed by the examples of robust ESD solutions for protecting data communication transceivers, high voltage IC, gas-sensor microchips, and low voltage RF IC.

Paul K. L. Yu



Dr. Yu is a professor at the Department of Electrical and Computer Engineering at the University of California at San Diego (UCSD). At UCSD he is teaching courses in solid state electronics and optoelectronics as well as conducting research on semiconductor materials and devices for various photonics and microwave applications. His research interests

include: lasers in the near infrared wavelength region for optical communication and optical interconnection; optical/RF schemes for narrow-band, high center frequency microwave transmission; high speed, high power optical detectors and high speed waveguide modulator devices for both digital and analog modulation; high power semiconductor optical switches for microwave generation; and electronic analog-to-digital conversion using high speed optical switches. He is a founding member of the IEEE AP/ED/MTT Chapter of San Diego, and is presently the Vice-President of Education Activities at IEEE Electron Devices Society. He is a Senior Member of IEEE and a Fellow of Optical Society of America.

Electroabsorption Modulator for Transparent Analog Fiber Link

This presentation gives an overview of the requirements of the photonic components in their insertion in applications such as CATV, antenna remoting and base station connections in wireless communication systems. The fiber-optic links are commonly used in these systems. For analog transmission, the gain and linearity properties are critical in the overall performance of the transmission system. Among the components of a fiber-optic link, the performance of optical modulator is of primary importance and has been broadly studied for advancing the analog fiber link.

The presentation reviews the advances in the state-of-the-art photonics devices for external modulation. Particular emphasis will be given to semiconductor electroabsorption modulator (EAM). The negative feedback in the EAM attributed to the photocurrent generation improves the modulator linearity but causes the transmission to saturate at high optical power. The implications for high link gain, low noise figure analog link will be presented.

Cor L. Claeys



Cor Claeys was born in Antwerp, Belgium. He received the electrical-mechanical engineering degree in 1974 and the Ph.D. degree in 1979, both from the Katholieke Universiteit Leuven (KU Leuven), Belgium.

From 1974 to 1984 he was a Research Assistant and Staff Member, respectively, of the ESAT Laboratory of the KU Leuven and since 1990, a Professor. In 1984, he joined IMEC as Head of Silicon Processing Group. He is for IMEC on the management board of several projects funded by the European Commission. He is also a member of the European Expert Group on Nanosciences. His main interests are in general silicon technology for ULSI, device physics, including low-temperature operation, low frequency noise phenomena and radiation effects, and defect engineering and material characterization. He also authored and co-authored eight book chapters and more than 700 technical papers and conference contributions related to the above fields. He has been involved in the organisation of a large number of international conferences and edited more than 35 Proceedings Volumes. He is an associated Editor for the *Journal of the Electrochemical Society*.

Prof. Claeys is a member of the European Material Research Society, a Senior Member of IEEE and a Fellow of the Electrochemical Society. He was the founder of the IEEE Electron Devices Benelux Chapter and was EDS Vice-President for Chapters and Regions during 2000-2006. Since 2000 he is an EDS Distinguished Lecture. In 2006, he has been elected as EDS President-Elect. He also received the IEEE Third Millennium Medal. Within the Electrochemical Society he has been serving in different committees and was Chair of the Electronics Division (2001-2003). In 2004 he received the Electronics Division Award of the ECS.

Processing and Defect Control of Advanced Ge Devices

The boost up the device performance, strain engineering is gaining much interest and has already been successfully implemented for 65 and 45 nm technology nodes. However, for sub 32 nm another interesting approach is based on using again Ge as a substrate. Worldwide there has been much interest in investigating the potential of Ge processing.

This presentation will review the advantages and challenges of advanced Ge processing for future logic applications. Attention will be given on the processing challenges such as ion implantation, shallow junctions, passivation, germanidation, contact technology, etc. For all the steps a good control of both the grown-in and the process-induced defects is crucial. Although very good electrical performances have been achieved for p-channel devices processed on Ge and GeOI high-mobility substrates, this is not the case for the n-channel ones. The future outlook will be briefly addressed.

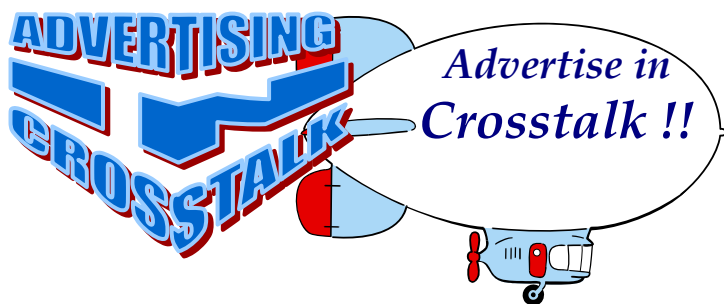
Directions to IBM East Fishkill Building 330 Cafeteria Hudson Valley Research Park

There is no fee for this colloquium, however advanced registration required by December 4th.

To register: email Fernando Guarin at guarinf@us.ibm.com



Obtain a visitors badge at the security guards' desk located in the lobby of Building 330 D. Escorts will be available from 8 - 8:30 AM to lead visitors to the conference area.



Reach over 900 engineers and professionals in the Mid-Hudson Valley. Place an ad with the Editor:

<i>Business Card:</i>	<i>\$ 30.00</i>
<i>1/4 Page:</i>	<i>\$ 50.00</i>
<i>1/2 Page:</i>	<i>\$100.00</i>
<i>Full-Page:</i>	<i>\$200.00</i>

Discounts available for long-term advertising.

Are you an IEEE Senior Member?

Becoming a Senior Member is not as difficult as you might think. According to the IEEE bylaws, "a candidate shall be an engineer, scientist, educator, technical executive or originator in IEEE-designated fields. The candidate shall have been in professional practice for at least ten years and shall have shown significant performance over a period of at least five of those years."

More information on Senior Member Elevation:
<http://www.ieee.org/organizations/rab/md/smforms.htm>

Congratulations to the recently elevated senior members:

Paul Patterson
Oliver Patterson
Murali A Padaparambil
Mohammad Zunoubi
Damu Radhakrishnan

Mid-Hudson Section ballot for 2008:

There are 7 elected positions in the Mid-Hudson Section: Chair, Vice-Chair, Secretary, Treasurer, and 3 members-at-large. The following individuals have volunteered for the positions below and have agreed to run for office and serve for the calendar year 2008.

Chair: Lisa Shay
Vice-Chair: Baback Izadi
Secretary: Gregory Kilby
Treasurer: David J. Dittman II
Members-at-Large Larry Boland, Bill McCarthy, (vacant)

Currently, there are no contested positions and there is one vacant position. If there are other members who would like to run for an office, we will conduct secret ballot elections using both paper and electronic processes. Please contact Rob Atkins at ratkins@us.ibm.com by December 7th if you are interested in running for an office.