

Joint Boston – NH – Providence Reliability Society Chapter Meeting

Super-Linear Increase in Soft Error Rate from Doubling the Cache Size: Bug or Phenomenon?

**Dr. Shubu Mukherjee IEEE-Fellow, Principal Engineer, Intel Corp.
6:00 PM, Wednesday, 15 April**

It has been discovered that processors can experience a super-linear increase in Detected Unrecoverable Errors (DUE) when the write-back L2 cache is doubled in size. This talk will explain how an increase in the cache tag's Architectural Vulnerability Factor or AVF causes such a super-linear increase in the DUE rate.

AVF expresses the fraction of faults that become user-visible errors. It is hypothesized that this increase in AVF is caused by a super-linear increase in "dirty" data residence times in the L2 cache. Using proton beam irradiation, the DUE rates from the write-back cache tags are measured and data has been analyzed to prove the hypothesis. A combination of simulation and measurements are performed to help develop and prove this hypothesis. The investigation reveals two methods by which dirty line residency causes super-linear increases in the L2 cache tag's AVF. One is a reduction in the miss rates as we move to the larger cache part, resulting in fewer evictions of data required for architecturally correct execution. The second is the occurrence of strided cache access patterns, which cause a significant increase in the "dirty" residency times of cache lines without increasing the cache miss rate.

This is joint work with Arijit Biswas, Charles Recchia, Vinod Ambrose, Leo Chan, Aamer Jaleel, Athanasios E. Papathanasiou, Mike Plaster, and Norbert Seifert.

Dr. Shubu Mukherjee is a Principal Engineer and Director of Intel's SPEARS Group (Simulation and Pathfinding of Efficient and Reliable Systems). The SPEARS Group is responsible for spearheading architectural change and innovation in the delivery of enterprise processors and chipsets by building and supporting simulation and analytical models of performance, power, and reliability. Dr. Mukherjee received his B.Tech. from the Indian Institute of Technology, Kanpur and M.S. and PhD from the University of Wisconsin-Madison. He is an IEEE Fellow. He was the General Chair of ASPLOS (Architectural Support for Programming Languages and Operating Systems), 2004. He has co-authored over 40 external papers. He holds 17 patents and has filed over 25 in Intel.

The meeting will begin with personal networking and a light dinner at 5:30 PM. The presentation will follow at 6:00 PM. IEEE members and non-members are welcome. There is no charge for the dinner or presentation, but we request that you **register to attend by Monday, April 13th**, so we can plan the refreshments. You can register online by visiting the Reliability Chapter's website at <http://www.ieee.org/bostonrel>.

The meeting will be held at EMC Corporation, 176 South Street, Hopkinton, MA. From Rte. 495 North or South take exit 21B, West Main Street. At the end of the ramp head West. At the first set of traffic lights (after the on/off ramp) take a left onto South Street. Building 176 will be about 1.5 miles on your LEFT. There is a traffic light just beyond the entrance to Building 176. For a map and more directions, see the EMC website at: <http://www.emc.com/about/facilities/index.jsp>