SOLID-STATE CIRCUIT SOCIETY

GREEN MOUNTAIN CHAPTER EVENT

December 02, 2006, 105 Votey, UVM

Time	Topic
1:00PM	**APPLICATION CUSTOMIZED CPU DESIGN FOR MICROSOFT XBOX 360** *BOB DREHMEL AND MATT GRADY, IBM*
2:00PM	**XBOX 360 AMB BRIDGE DEVELOPMENT AND ARCHITECTURE** *ROSS OGILVIE, BOB DREHMEL AND CHARLIE WOODRUFF, IBM*
3:00PM	**CIRCUIT TECHNIQUES FOR SPEEDING UP THE INTERNET FOR REAL-TIME GAMING EXPERIENCE** *IGOR ARSOVSKI, IBM*
4:00PM	**REFRESHMENT,** **XBOX 360 DEMONSTRATION AND GIVEAWAY**

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1:00PM	**APPLICATION CUSTOMIZED CPU DESIGN FOR MICROSOFT XBOX 360** *BOB DREHMEL AND MATT GRADY, IBM* **Abstract** The Engineering & Technology Services Division of the IBM Corporation, in cooperation with Microsoft, developed an advanced CPU component for the XBOX360 game console. This custom chip includes 3 PowerPC CPU cores; a 1MB shared L2 cache, and a high speed serial front side bus (FSB). Specially architected features were developed and integrated into the CPU. The high frequency and power optimized PowerPC CPU core was originally developed for high performance low power applications. In the XBOX360 application, it was adapted for the specific requirements of Microsoft's gaming architecture. The shared L2 cache, which supports the multiple cores, provides coherent memory operations. The FSB interface into the cache was architected to optimize the bandwidth and control operations between the CPU and the custom graphic accelerator chip. This presentation will describe the CPU chip structure and advanced features developed for this unique product. High quality and first time right development were essential to success of the program. The presentation will also describe the world class development methodology and verification practices which were key enablers for this program's aggressive schedule and crucial time to market. **Speaker Bio** **Bob Drehmel** is a Senior Technical Staff Member in IBM's Systems and Technology Group Development. His areas of expertise encompass a wide range of chip development disciplines including architecture, design, implementation, and delivery. He has worked on several ASIC memory controller, switch, and CPU designs for IBM servers including iSeries, pSeries, and BlueGene. Bob worked closely with Microsoft in the architecture and development of the Waternoose CPU for the XBOX360 and continues to collaborate with them on future cost reductions. He is currently the Chief Engineer for the XBOX360 cost reduction CPU project. Bob received his BS degree in Electrical Engineering from the University of Minnesota, Twin Cities campus in 1985 and joined IBM in Rochester, Minnesota, thereafter.

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2:00PM	**XBOX 360 AMB BRIDGE DEVELOPMENT AND ARCHITECTURE** *ROSS OGILVIE, BOB DREHMEL AND CHARLIE WOODRUFF, IBM* **Abstract** With rapidly growing demand for cutting-edge electronics, such as Microsoft's XBOX360, development teams are under extreme pressure to deliver unprecedented performance in record times using a first time right methodology. Early prototyping by a focused and independent team is a key element in delivering an early base for software and hardware evaluation, while relieving pressure on the main product development. This presentation touches on the development of such a prototype system for the XBOX360 using the existing IBM PowerPC 970 processor chip and incorporating selected elements of the target system. The focus of this presentation is on the development and architecture of the processor bus bridge (AMB) in the prototype system, allowing communication between the existing IBM 970 multi-processor coherent processor bus (API) and the target multi-processor coherent processor bus (MPI). **Speaker Bio** **Ross Ogilvie** is a Senior Technical Staff Member at the IBM ASIC Design Center, Williston, VT. Ross joined IBM in 1978. He received his BSEE from the University of Maryland in 1977, and his MSEE from the University of Vermont in 1983. His experiences include Architecture, Logic, and Circuit development of Processors, Digital Signal Processors, and Systems. Ross's interests include real time systems and systems on chips. He is currently responsible for benchmarking ASIC design system libraries. He has filed 46 US Patents with 24 granted, and is a co-author and presenter of multiple papers regarding Systems On a Chip and Digital Signal Processors. He is a senior member of IEEE and lives with his family in the woods of Vermont. **Charlie Woodruff** is an Advisory Engineer in IBM's System and Technology Group. His background in hardware and software engineering led to his current interest in functional verification of complex digital designs such as System-On-Chips. Charlie currently works as a verification engineer for next generation POWER Processor Cores. Charlie received his Master's Degree in Electrical Engineering from the University of Pennsylvania in 1990 and has been with IBM for 7 years.

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Time	Topic
3:00PM	**CIRCUIT TECHNIQUES FOR SPEEDING UP THE INTERNET FOR REAL-TIME GAMING EXPERIENCE** *IGOR ARSOVSKI, IBM*

Abstract

The explosive growth of the Internet has placed tremendous strain on network hardware. The number of networked devices is growing, while Internet traffic is doubling every year. Today, major Internet nodes receive and forward billions of data packets every second. Network routers at each node forward these data packets by comparing the destination address embedded in each packet to the shortest-path information found in the router look-up table. With network transmission channels being capable of sustaining very high data rates, the bottleneck in high-speed networking is network address look-up. In the past, look-up tables were searched using hashing or binary search algorithms implemented in software. Hashing was relatively fast but required a non-deterministic number of probes, while binary search required a pre-sorted look-up table. As networks grew in size and speed, the performance requirements for these look-up tables grew accordingly. Today, the internet traffic through major nodes has reached data rates that make software approaches impractical. To implement a nanosecond address look-up, high-speed network routers use Content Addressable Memory (CAM). In a single cycle, a CAM searches the entire memory array and returns an address. This address is then used to access an embedded RAM, which returns the next hop for the data packet. Since data packets arrive at high-rates and usually pass through many routers, the time-saving of using CAMs adds up very quickly. However, today's CAM chips suffer from relatively low density and relatively high power consumption, both with respect to SRAM and DRAM. Technology scaling has been improving these performance metrics, but not enough to meet the demands of today's CAM market. New high-speed, low-power architectures and circuits need to be developed.

This talk will focus on a novel memory sense-amplifier circuit that self-calibrates during sense-line pre-charge to reduce signal development and minimize timing uncertainty caused by random device variation. Compared to conventional single-ended sensing, this method reduces sense-time by 70% while also decreasing sense-power by 40%. The self-referenced sensing scheme is implemented in a 64x240bit Content Addressable Memory (CAM) testchip. Fabricated in 1V 65nm CMOS, this scheme achieves 2.2ns search-access on a 240bit CAM word while consuming 10mW. Hardware shows robust operation across 0.6V to 1.7V.

Speaker Bio

Igor Arsovski received the Bachelor and Master's degrees from the Department of Electrical and Computer Engineering at University of Toronto, Canada. He has published numerous papers at ISSCC, CICC, ITC, and JSSCC, and has a number of applications and patents in this field of Content Addressable Memory. In the past, he has worked with Mosaid Technologies on development of high-density content-addressable memories for network processors. He is currently working with IBM Silicon Solutions on the design of high-performance low-power embedded Content Addressable Memories.