

IEEE MEETING

*A joint meeting of the UVM IEEE student branch &
The IEEE Vermont Solid-State Circuit Chapter*

Speaker: Kerry Bernstein, Senior Technical Staff Member
IBM T.J. Watson Research Center

Caution Flag Out: Micro-architecture's Race for Power Performance

**Thursday, April 21st
6:00 p.m., Lafayette L102**

RSVP to Pascal Nsame: pnsame@ieee.org by the 19th.

FREE PIZZA will be served! Everyone is invited!

Presentation Abstract: *Micro-architecture and technology scaling have historically shared responsibility for the microprocessor's phenomenal generation-over-generation performance improvement. The era marked by lavish use of successively scaled, leakier MOSFETs to achieve incremental architectural transaction rate growth is coming to a close, however. Increased pipeline depth has caused supra-linear latch density expansion; shorter FO4-equivalent cycles have made control logic substantially more complex. The resulting energy per operation, scaled-process-induced delay variation, and erosion in die area access latency has become real-world constraints. This talk will explore how features of past technologies have influenced high speed micro-architectures, and how the characteristics of proposed new devices and interconnects for lithographies beyond 90nm may shape future machine design. Given our industry's power-restricted ability to continue scaling, and the approach of fundamental, quantum-mechanical boundaries, the role of micro-architecture in extending CMOS performance will be more important than ever.*

Speaker Bio: Kerry Bernstein is a Senior Technical Staff Member at the IBM T.J. Watson Research Center, Yorktown Heights, NY. He is currently responsible for future product technology definition, performance and application. Mr. Bernstein received the B.S degree in electrical engineering degree from Washington University in St. Louis, and joined IBM in 1978. He holds 44 US Patents, and is a co-author of three college textbooks and multiple papers on high speed and low power CMOS. His interests are in the areas of high performance / low power circuit technology, delay variability, and CMOS Single Event Upsets. He is a senior member of IEEE, and is a staff instructor at RUNN/Marine Biological Laboratories, Woods Hole Oceanographic Institute. He and his family live in northern Vermont.