



Technical Vitality Seminar

65nm CMOS 6.4 Gbps Source Synchronous Communication Interface

By John Bergkvist

IBM System and Technology Group, Essex Junction Vermont

Tuesday, November 17, 2009

At The College of Engineering and Mathematical Science,
University of Vermont Campus, Votey 105

Technical Talk

(Including Complementary Pizza and Drinks)

Starts at 6:00 pm (EST)

RSVP by Nov. 16, 09. To Register or for questions, please contact: pnsame@us.ibm.com

Abstract - An overview of a 6.4Gbps source synchronous communication interface implemented in a 65nm CMOS process will be presented. Such interfaces are used in numerous industry standards today where power and area efficiency as well as low latency are critical design objectives. The featured design employs impedance controlled source series terminated differential drivers with three tap feed forward equalization. The receiver function employs a dual termination mode, continuous time linear equalized sampler with variable eye tracking bandwidth.

John Bergkvist received his B.Sc. in Electrical Engineering at the Pennsylvania State University at State College, Pennsylvania in 1985. He joined IBM General Technology Division in Burlington, Vermont as a reliability engineer in 1985. In 1988, he was involved in the design and development of x86 and Power PC based microprocessors. In 1996, he was involved in the Application Specific Integrated Circuit (ASIC) intellectually property development of numerous designs including USB Host Controllers, ARM based microprocessors, Digital Signal Processors, and high speed memory interfaces. John is presently a Senior Engineer working in the ASIC IP development business designing high speed communication link interfaces.



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