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FROMTHEEDITORIALTEAM

Ifyouareacommunicationengineer,thereisnoneedtotellyou how exciting the rapid progress in the telecommunication domainhasbeen.AndthebestpartofitisthatIndiaisnolonger justanobserver.Wellmaybewearenotyetamajortechnology innovator, but we certainly are a technology driver. India with it'smassivepopulationisbeingrecognizedasamajormarketfor thetelecomindustryworldwide.

ThebloomofthemobileservicesindustryinIndiahasbeen phenomenal. However the broadband connectivity sector has beenlaggingbehind.Attheendof2005,therewereonlyaround 835,000 broadband subscribers. Not much, considering the 3 milliontargetsetbyTRAI.Butthingsarelookingup,especiallly with WiMAX leading the way. WiMAX (Worldwide Interoperability for Microwave Access) is a certification m ark for products that pass conformity and interoperability tests for the IEEE 802.16 and ETSI HiperMAN standards. WiMAX technology provides high-throughput broadband connections overlongdistancesandisapromisedsolutionto"lastmile"

broadband connections, cellular backhaul, and high-speed enterprise connectivity for business. Recently, the Department of Telecommunications (DoT) short listed four frequency bands for the allocation of spectrum for WiMAX services—2.5–2.69 GHz, 3.4–3.6 GHz, 2.3–2.4 GHz, and 700 MHz bands. You do get the feeling the allocation is pretty late, considering that WiMAX networks have already been deployed in a few cities across India (trials in Bangalore). But allocation of resources is never a trivial problem. Already the Department of Space (DOS) has opposed the allocation in the 2.5 – 2.69 GHz band, since various satellite-based mobile and broadcast applications, including disaster-warning dissemination, radio, and networking services use part of this band.

Anyway, looking at the current trend, broadband connectivity will invade our lives probably riding on WiMAX. Not just in the cities but also in the rural areas where wireless connectivity is preferred over any other kind of medium. Kicking off on this positive note, welcome to the 5th edition of the IEEE SP Bangalore chapter newsletter—SIGSALS. We have quite a few events lined up for you; check out the “upcoming events” section. Furthermore, as mentioned in the previous edition we are going to focus on tools used in our daily trade, which you can relate to. We start with that lifelong (but costly!) friend—MATLAB! Please share with us, all your homemade recipes and little magic tricks that years of practice has embedded into your way of working with MATLAB. In this edition, we have an article on Algorithm Development Life-cycle. We are also happy to announce that the SPSIG activity has been kicked off with the first Advanced DSP Architecture workshop to be held in Nov in Bangalore.

So go ahead and vibewiththeSIGNALS!

Looking forward to your active participation,

The Editorial team

ANNOUNCEMENTS

Let us talk tools

Tools are an engineer's best friend. The better we understand our tools, the better the quality of our work will be. As part of our widening sphere of activities, we would like to initiate a forum for IEEE members to share their expertise in tools used for DSP, with each other. Please send in articles on the latest tools used in any field of DSP and why you would recommend them. Articles on tips and tricks to make life simpler, are also welcome. "Dos and Don'ts", FAQs, To-do lists, you name them, we want them! Keep the spirit of sharing alive!

Send your feedback and contribution to ieesp@dsplab.ece.iisc.ernet.in

MAINCOURSE

Algorithm Development Life-cycle

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Introduction:

Algorithms are needed to process input information and generate output information. A/D converters are used for transforming analog (continuous) signals into digital signals (discrete). With availability A/D and D/A converters, and digital signal processors (DSP core, ASIC, or GPP core), the signal processing can be performed with a lot of ease in digital domain. This article describes the steps and tools that can be used to make the life of a Signal Processing engineer easier. Though MATLAB is described here, any other computational tool also can be used.

Algorithm Development:

Algorithms can be broadly classified as control and data processing elements. Control algorithms process relatively lower amount of data, ex. provided by sensors, to generate output control signal, for actuators. Data processing algorithms process large amount of data, as in audio and video algorithms.

Algorithm development typically has the following phases:

1. Requirement
2. Analysis
3. Studying available algorithm choices
4. Algorithm evaluation and selection
5. Design
6. Implementation
7. Test and performance measurements

Requirement:

Requirements could be problem statements. For example, remove noise from captured audio or synchronize audio and video. Sometimes the requirements could be the name of effects like audio equalizer. Also, the requirements could specify the algorithm name as in Automatic Gain Controller (AGC).

Analysis:

Requirements are carefully analyzed to generate algorithm specification. For example, remove noise from audio is very generic. This might need interaction with algorithm requirement generator so as to narrow down finer requirements like nature of noise, bandwidth of audio signal, nature of audio signal, desired SNR after filtering, SNR before filtering, and available hardware resource.

Study of available algorithms:

Algorithms may already exist to address the problem. Also, it may be possible to solve the given problem (or algorithm specification) using different algorithms. Further, different algorithms might exist to address the problem to varying degrees (for example, SNR and computation load might vary from one algorithm to another).

Algorithm selection:

The available algorithms are evaluated. MATLAB or C code can be used to evaluate algorithm complexity, and algorithm specifications. If none of the available solutions are good enough to address the problem, a new algorithm may be developed.

MATLAB provides easy means for selecting filters and tuning parameters. Filter design toolbox provides wide array of filter types.

Algorithm design:

Algorithm design might involve 2 phases: design, and tuning. Algorithm design, for example, could be a notch filter design using IIR. The design would decide the computation complexity (number of stages, filter order, time-domain/frequency-domain processing, etc.) to meet the algorithm specification. Tuning would typically involve in selecting filter coefficients or algorithm control parameters. Thus tuning may be needed even if algorithm pre-exists.

MATLAB code aids in faster design of algorithms. The algorithms can be developed and tested in MATLAB. Algorithm tuning is lot simpler with the aid of MATLAB tools. C code though requires more coding, would run faster compared to MATLAB. If the algorithm needs to be evaluated on many test cases, C code might prove to be advantageous for algorithm design.

Algorithm implementation:

Algorithms can be implemented entirely in hardware, software, or hardware and software. Algorithms implemented fully or partially on hardware allow for controlling algorithm response using programmable parameters. Algorithms can be implemented on a programmable processor code with or without the aid of accelerators. The algorithm partition between programmable core and accelerator/coprocessor is chosen based on run-time efficiency and resource availability. Often algorithm implementation needs fixed point representation and computation hardware for optimizing processing load requirement and gate count. While implementing algorithms in fixed-point, care needs to be taken to maintain desired precision, avoid saturation, and prevent

undesired overflow. The choice of programming language for algorithm part running on programmable core could vary from high level language like C and assembly language. Computation intensive code is better written in assembly language for optimizing computation load. Control code written in high level language might not change loads significantly if used with compiler optimization flags. Choice of language between C and assembly is based on load optimization, and code development and maintenance time.

Algorithm test:

Algorithm is tested for all possible input conditions, overflow, saturation, and error handling and recovery. Algorithm performance is measured against specific application. Performance includes meeting problem statement and computation complexity. Computational accuracy is often tested against reference code available in C or MATLAB (from design).

Algorithm maintenance:

Algorithms might require tuning or evolution based on new requirements or learning. It is advisable to keep reference code (from design) and actual platform implementation in synchronization, during maintenance phase.

Signal processing in digital domain and availability of tools like MATLAB has simplified algorithm development both in terms of complexity and development time. Fixed-point arithmetic library aids in faster development time high level reference code and reuse across algorithm development. MATLAB quantizer tools aid in fixed-point algorithm implementation.

Conclusion:

This article showed the steps involved in solving a given Signal Processing problem using tools like MATLAB. With advanced simulation software and easy to use tool-kits, such computational tools can be employed to great benefit by the SP community to reduce development and product release-to-market times.

UPCOMINGEVENTS

IEEE SP DSPA-SIG announces
**IEEE Advanced DSP Architectures &
 Programming Workshop**

Nov 9–Nov 10, 2006
 Hotel Capitol,
 Raj Bhavan Road
 Bangalore 560-001, India

Registrations are limited to 100 persons on first-come first-serve basis. This workshop is designed for DSP software & systems engineers with an interest in programming processors for DSP applications. The processors covered in this workshop are Texas Instruments c64x+, ARM, Analog Devices Blackfin & Freescale. The focus of the workshop will be on processor architecture, programming & optimization techniques. Basic knowledge of DSP concepts and C programming is assumed.

Agenda

Thursday, Nov 9, 2006		
9:00AM – 9:30AM	Registration	
9:30AM – 10:00AM	Inauguration & Welcome	
10:00AM – 1:00 PM	TI c64x+	Soyeb Nagori & Pankaj Rabha
1:00PM – 2:00PM	Lunch	
2:00PM – 5:00PM	ARM v7 Architecture	Keith Clarke
Friday, Nov 10, 2006		
9:00AM – 12:00 Noon	Analog Devices Blackfin Architecture	Rajesh Mahapatra & S. Sivaramakrishnan
12:00 Noon – 1PM	Lunch	
1PM – 4PM	Freescale	To Be Announced
4PM – 5PM	Panel discussion: "Are today's students well-prepared for DSP and Embedded systems careers"	

Organization Team

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How to register

This event needs advanced registration. Registrations are limited and on first-come-first-served basis. Please fill in the attached registration form and send it to Sharada Rao (Sharada@ece.iisc.ernet.in) by email. Also, mail a print-out of your registration form with your registration cheque for the registration amount in the name of "IEEE SP, Bangalore Chapter" to Sharada at the address below before Oct 30, 2006. You will receive an acknowledgment of your registration by email.

Registration Fees (includes lunch)
Regular (Non-IEEE member): Rs 2000/-
IEEE Member: Rs 1500/-
IEEE Student Member: Rs 1200/-

Contact Information:

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CALL FOR PAPERS

IEEE Signal Processing Magazine Special Issue on Multi-View Imaging and 3DTV

Multi-view imaging (MVI) has attracted increasing attention recently, thanks to the rapidly dropping cost of digital cameras. This opens a wide variety of new research topics and applications, such as virtual views synthesis, high performance imaging, image/video segmentation, object tracking/recognition, environments surveillance, remote education, industry inspection, 3DTV, gaming, etc. While some of these tasks can be handled with single view image/video, the availability of multiple views of the scenes significantly broadens the field of application, while enhancing performance and user experience.

Prospective authors should submit whitepapers to the web submissions system at <http://www.ee.columbia.edu/spm/> according to the following timetable. Whitepapers, limited to

6 single-column double-spaced pages, should summarize the motivation, the significance of the topic, a brief history, and an outline of the content.

Whitepaper due: December 15, 2006
Invitation notification: January 15, 2007
Manuscript due: April 15, 2007
Acceptance notification: June 15, 2007
Final manuscript due: July 15, 2007
Publication date: November, 2007

UPCOMING EVENTS IN BANGALORE

TIDeveloper Conference Bangalore (www.ti.com/tidcindia2006)

Venue: NIMHANS Convention Center

Date: 30th November – 1st December, 2006
Two-day detailed developer tutorials will be held prior to TIDC Bangalore at the same venue from 28–29th November, 2006.

FAQ:

Who should attend?

TIDeveloper Conference India 2006 is designed for:

- System, hardware and software design engineers working across DSP, microprocessor and analog technologies. Whether you are new to design or an experienced digital/analog designer seeking exposure to new applications and products, TIDeveloper Conference is right for you.
- Firms such as original equipment manufacturers, value added resellers, original design manufacturers, system integrators, hardware/software design firms, referenced design firms, component providers and technology consultants will find TIDeveloper Conference India 2006 an ideal platform to explore emerging technology areas and identify new partners with which to build their future offerings.

- University faculty, research staff and students specializing in digital signal processing, microcontroller and analog designs stand to advance their expertise from the TI Developer Conference India 2006
- Forty of TI's top hardware, software, component, service, design and manufacturing partners will exhibit their offerings. Multiple exhibition areas will be set up for visitors to view the diverse range of TI silicon-based IP, products & services these partners offer. The exhibition areas will be open during the full two days of the conference, in addition to which there will be dedicated breaks for all delegates to visit the exhibition floor.
- Booths and speaking sessions by tools & educational partners will showcase the advances in DSP, microcontroller and analog tools and educational options available to industry and universities.
- Discussion rooms will be provided for customers, partners and TI decision makers/specialists to conduct technology and business meetings.
- Visitors will be able to "Ask the Experts", i.e. highly specialized TI staff -wearing distinctive red TI caps- who can answer deep technical queries. Other TI staff at the venue will also be approachable for discussions.
- An expected 1,000 delegates will be present at TIDC India 2006 for you to network with and exchange information with. In addition, the exhibition floor will be opened for up to an additional 1,000 visitors.
- Multi-day hands-on pre-TIDC tutorial on key emerging areas will be conducted on 28-29 November 2006 by experts for developers wishing to upgrade their technology skills.

Schedule

TIDC India 2006 will be held at the NIMHANS Convention Center in Bangalore, India from 30th November - 1st December 2006. Delegate registration-cum-breakfast will be from 8:00am-8:45am, and the conference will be from 8:45am-7:00pm.

The Pre-TIDC India hand-on tutorial sessions will be held at the NIMHANS Convention Center on 28-29th November 2006. Delegate registration-cum-breakfast will be from 8:00am-8:45am and the tutorials will be from 9:00am-6:00pm.

For other IEEE SP Worldwide events including ICASSP, please see the IEEE SP Conferences webpage.

GETTING CONNECTED

MailinglistforIEEE SPBangalorechapter

To facilitate better information spread across the wide spectrum of members and volunteers of the SP Bangalore chapter, a LISTSERV list is available.

- To email all of the list's subscribers (please use this responsibly), send your mail to IEEE SP-BLR@LISTSERV.IEEE.ORG
- Creating a new subscription is easy. If you want to subscribe a member to the list, send a mail from your email to LISTSERV@LISTSERV.IEEE.ORG and type "subscribe ieesp-blr" without quotes in the body of the message. Leave the subject line blank. More information on using LISTSERV is available at <http://listserv.ieee.org/>

Links

This link contains information related to IEEE SP conferences
<http://www.ieee.org/organizations/society/sp/SPSConf.html>

IEEE SP Bangalore Chapter Homepage
<http://ewh.ieee.org/r10/bangalore/sps/>

CHAPTER INFORMATION

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