

Ultra-low Voltage Design Techniques for Nanoscale Silicon CMOS

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Abstract

Because of the quadratic relationship between power and voltage, supply voltage reduction has become an important method for reducing active power in VLSI systems, improving reliability in highly scaled MOSFETs, and minimizing the effects of heat dissipation in high-performance systems. As silicon CMOS is scaled beyond the 90 nm and 65nm to the 32 nm and 22 nm technology nodes, ultra-low supply voltage becomes one of the most critical and powerful mechanisms for improving device reliability and energy efficiency. Unfortunately, ultra-low voltage operation has been limited by performance constraints and other challenges. This presentation evaluates the current state of low-voltage VLSI design, provides techniques for maintaining acceptable throughputs at these sub-volt supplies, and suggests noise tolerant techniques to mitigate the reduced voltage margins. Trends and prospects for ultra-low voltage VLSI in nanoscale CMOS are discussed.

Biography

Paul Ampadu received the Ph.D. in electrical and computer engineering from Cornell University in 2004. Prior to receiving the doctorate, Paul worked at the IBM Thomas J. Watson Research Center, where he collaborated with researchers on multiple VLSI projects, resulting in practical technology transfer between research and development, as well as joint publications. Before IBM, Paul worked at Microsoft Corporation, where he helped ship the first Macintosh version of Japanese Word, defined technical features for the first 32-bit Windows version of Microsoft Word Far East (Japanese, Chinese and Korean versions), and was a co-technical editor of three Microsoft Press books. As an undergraduate, he was honored as an eminent scholar and a university scholar. During his graduate studies, he was awarded a Semiconductor Research Corporation (SRC) master's scholarship and an IBM doctoral fellowship. Currently, he is an assistant professor of electrical and computer engineering at the University of Rochester and directs the Embedded Integrated System-on-chip (EdISon) Research Group. His current research goals are to contribute to the extension of the use of silicon CMOS into the next several decades, through careful and intelligent design techniques and tools, and innovative integrated applications. Consequently, his research interests include energy-efficient nanoscale VLSI design, ultra-low voltage and reliable design of complex signal processing and communications fabrics, error-control coding, and systems-on-chip integration.