

Bio:

Carl Grace is a Senior IC Design Engineer with Analog Devices in Raleigh, North Carolina, where he is focused on RF transceiver design in deep submicron CMOS. Prior to ADI, Carl was with ClariPhy Communications in Irvine, California, where he was the chief architect for the world's first 10-Gigasample, 6-bit CMOS ADC. Before that, he was with Conexant Systems in Newport Beach, California, where he designed data converters and front-end circuits for DSL transceivers, 56k modems, and an 802.11 baseband processor. Carl began his professional career at Lawrence Berkeley National Laboratory in Berkeley, California, where he designed radiation-hard analog ICs for the instrumentation of subatomic particle detectors. Carl received his Ph.D. from the University of California, Davis, for his research on digital background calibration of pipelined analog-to-digital converters.

Abstract: NOISE IN COMMUNICATION RECEIVERS

Contrary to popular belief (and perhaps wishful thinking) noise is not a second-order effect; it is the fundamental factor in determining communication system performance. However, strange notation and terminology, bizarre units, and seemingly counter-intuitive behavior can impede the appreciation of noise necessary to design high-performance communication receivers. This talk will attempt to demystify electronic noise in communication receivers by approaching fundamental concepts from an intuitive standpoint and by showing how probability theory and system design must interact to effectively deal with the impact of noise. Several examples will be presented that demonstrate how an understanding of noise can be exploited to improve the performance of communication receivers.