Effective Power/Ground Plane Decoupling for PCB

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Power/Ground-Reference Plane Noise

• Must consider TWO Major Factors
  – Functionality -- Provide IC with sufficient charge
  – EMC -- Reduce noise along edge of board from IC somewhere else

• Decoupling strategies are FULL of Myths
Source of Power/Ground-Reference Plane Noise

- Power requirements from IC during switching
- Critical Net currents routed through via
Power Bus Spectrum
Clock Driver I DT74FCT807
Noise Injected between Planes Due to Critical Net Through Via

Edge voltage test point 1 (150,33.3)

Edge voltage test point 2

signal via

I/O line via

signal line

I/O line

V_{\text{edge}}

PWR

GND

Z_{s} = 50 \, \Omega

60 \, \Omega

Z_{\text{ant}} = 100 \, \Omega

Vs

t

10 mils

10 mils

60 \, \Omega

10 mils
Transfer function from Via to I/O Pin

The diagram shows the transfer function from Via to I/O Pin, plotting Voltage Ratios (dB) against Frequency (MHz) across different thickness configurations: 10 mils, 20 mils, 30 mils, and 45 mils. The frequencies range from 100 MHz to 3000 MHz, and the voltage ratios are measured in decibels (dB). The graph highlights specific modes such as TM10, TM11, TM01, TM02, TM31, and TM40, demonstrating the attenuation and resonance characteristics across the specified frequency range.
Decoupling Must be Analyzed in Different Ways for Different Functions

- EMC
  - Resonance big concern
  - Requires STEADY-STATE analysis
    - Frequency Domain
  - Transfer function analysis
    - Eliminate noise along edge of board due to ASIC/IC located far away
Decoupling Must be Analyzed in Different Ways for Different Functions

• Provide Charge to ASIC/IC
  – Requires TRANSIENT analysis
  – Charge will NOT travel from far corners of the board fast enough
  – Local decoupling capacitors dominate
  – Impedance at ASIC/IS pins important
Steady-State Analysis

- Measurements and Simulations
- Test Board with Decoupling capacitors every 1” square
Figure 1

Test Board Ports

12"
11"
10"
9"
5"
9"
6"
3"
1"
3"
6"
9"

#1 #2 #3 #4 #5
#6 #7 #8 #9 #10
#11 #12 #13 #14 #15

Figure 1
S21 Used for Decoupling “Goodness”

- Ratio of Power ‘out’ to power ‘in’
- Better Indicator of EMI noise transmission across board
- Also used to validate simulations
Measured $S_{21}$ for 12" x 10" PC Board Between Power/Ground Planes with No Decoupling Capacitors (Measured Center to Corner)

- Board Capacitance Dominates
- Physical Board Size Resonances Dominate
Test Board Decoupling Capacitor Placement for 25 .01 uf Caps
Test Board Decoupling Capacitor Placement for 51.01 uf Caps

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Possible Cap Location

Populated Cap Locations
S21 Between Port #8 and Port #1 on Test Board
With Various Amounts of .01 uf Decoupling Capacitors

![S21 Graph](image-url)

- Frequency (Hz): 0.0E+00 2.0E+08 4.0E+08 6.0E+08 8.0E+08 1.0E+09 1.2E+09 1.4E+09 1.6E+09 1.8E+09
- S21 (dB): -120 -100 -80 -60 -40 -20 0

Legend:
- No Caps
- 25 Caps
- 51 Caps
- 99 Caps
S21 Between Port #8 and Port #1 on Test Board
With Various Amounts of .01 uf Decoupling Capacitors

Frequency (Hz)

S21 (dB)

No Caps
25 Caps
51 Caps
99 Caps
Cap Impedance

- 0.01uF
- 22pF
- 0.01uF in parallel with 22pF
Test Board Decoupling Capacitor Placement for 41 22pf Caps
(In Addition to 99 .01uf Caps)
S21 Between Port #8 and Port #1 on Test Board
With 99 .01 uf Decoupling Capacitors and Various Amounts of 22pf Capacitors Added

-60
-50
-40
-30
-20
-10
0
0.0E+00 2.0E+08 4.0E+08 6.0E+08 8.0E+08 1.0E+09 1.2E+09 1.4E+09 1.6E+09 1.8E+09
Frequency (Hz)

S21 (dB)

9 22pf Caps
17 22pf Caps
21 22pf Caps
33 22pf Caps
41 22pf Caps
99 22pf Caps
99 Caps
Comparison of Model and Measured Data
for 10" x 12" Board

99 caps -- alternating .01uF and 330pF

S21 (dB)

Frequency (Hz)
S21 Transfer Function for Different Value Capacitors

Center-to-Corner

10" x 12" Board
Voltage Distribution @ 350 MHz
0.01uF and 330pF Case (Source in Center)
Voltage Distribution @ 750 MHz
.01uF and 330pF Case (Source in Center)
Voltage Distribution @ 950 MHz
.01uF and 330pF Case (Source in Center)
Voltage and Gradient
99 caps @ 800 MHz
.01 uF Capacitor Impedance with 5/8” Trace
1000 pF Capacitor Impedance with 5/8” Trace

1000pF with 5/8” extra trace inductance

16dB difference

1000pF with nominal trace, via ind.

Frequency

1.0MHz  3.0MHz  10MHz  30MHz  100MHz  300MHz  1.0GHz

$V(U1:+) / I(U1)$
22 pF Capacitor Impedance with 5/8” Trace

- 22pF, 5/8” extra trace inductance
- 22pF, nominal trace & via inductance

Frequency

1.0MHz 3.0MHz 10MHz 30MHz 100MHz 300MHz 1.0GHz
Other Design Possibilities

• So-called Buried Capacitance
  – Reduces high frequency transfer function
  – Allows less capacitors to be used
  – Really should be called ‘increased distributed capacitance’

• Lossy decoupling
  – Reduces high frequency transfer function
  – Allows less capacitors to be used
Buried Capacitance

- Planes very close together (2 mils)
- Only effective for the power/ground plane pair !!!
- Other sets of Planes must still be decoupled the traditional way
Buried Capacitance **ONLY**
Applies to Plane Pairs

Still Needs Decoupling

Buried Capacitance Plane Pairs
Transfer function for Decoupling Board 10" x 12"
with Various Power/Ground Plane Separation and No Capacitors

Transfer function (dB)

Frequency (Ghz)
Transfer function for Decoupling Board 10" x 12"
with Various Power/Ground Plane Separation

Transfer function (dB)

Frequency (GHz)

2 mil - No Caps
10 mil - No Caps
20 mil - No Caps
35 mil - No Caps
35 mil w/99 caps
Lossy Decoupling

• New technique
• Series resistance and capacitance in same SMT package
• Need to use both low ESR capacitors and lossy capacitors
  – fewer total parts
Cause of Failure above 400 - 500 MHz?

- Inductance is limiting factor for capacitors
- Board size cause resonances which causes problems
- Need to reduce resonance effects by lowering Q-factor
  - add resistive loss
Transfer Function with Resistive Caps
Port 8 to Port 1
(Resistive Caps with ~10 ohms and 0.01 uF)
Comparison of Impedance of SMT Capacitors
Lossy and Normal Capacitor (0805 size)

![Graph showing comparison of impedance magnitudes for standard and resistive 0.01uF capacitors across different frequencies.](image-url)
Transient Analysis

• Provide charge to ASIC/IC
• Inductance dominates impedance
  – Loop area 1\textsuperscript{st} order effect
• Traditional analysis not accurate enough
Traditional Analysis #1

- Use impedance of capacitors in parallel

Impedance to IC power/gnd pins

No Effect of Distance to IC Included!
Traditional Impedance Calculation for Four Decoupling Capacitor Values

<table>
<thead>
<tr>
<th>Capacitor Value</th>
<th>Impedance (ohms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1uF</td>
<td></td>
</tr>
<tr>
<td>0.01uF</td>
<td></td>
</tr>
<tr>
<td>0.001uF</td>
<td></td>
</tr>
<tr>
<td>0.0001uF</td>
<td></td>
</tr>
</tbody>
</table>

All in Parallel

Frequency (Hz)

Impedance (ohms)
Traditional Analysis #2

- Calculate loop area – Traditional loop inductance formulas
  - Which loop area? Which size conductor

Over Estimates L and Ignores Distributed Capacitance
More Accurate Model Includes Distributed Capacitance
Distributed Capacitance Schematic

- Intentional Capacitor
- Distributed Capacitance
- ESR
- Loop L
- Capacitance

Note: L increases as distance from source increases
Effect of Distributed Capacitance

- Can NOT be calculated/estimated using traditional capacitance equation
- Displacement current amplitude changes with position and distance from the source
Displacement Current
500 MHz via @40 mils from Source
Displacement Current
500 MHz via @40 mils from Source
Displacement Current
500 MHz via @450 mils from Source
Displacement Current
500 MHz via @450 mils from Source
Displacement Current
800 MHz via @40 mils from Source
Displacement Current
800 MHz via @40 mils from Source
Displacement Current
800 MHz via @450 mils from Source
Displacement Current
800 MHz via @450 mils from Source
Need to Find the Real Effect of Decoupling Capacitor Distance

• Perfect decoupling capacitor is a via between planes
• FDTD simulation to find the effect of shorting via distance from source
• Vary spacing between planes, distance to via, frequency, etc
Impedance of Shorting Via vs. Frequency
Four Via Case (20 mil Separation Between Plates)
Impedance Result

- Linear with frequency (on log scale)
- Looks like an inductance only!
- Consider this inductance an **Apparent Inductance**
- Apparent inductance is constant with frequency
Apparent Inductance for One Shorting Via Case
20 mil Plate Separation

Frequency (Hz)

Inductance (nH)

50mils
110mils
120mils
200mils
250mils
350mils
450mils
Formulas to Predict Apparent Inductance

\[
L_{\text{one-via}} = (0.1336s - 0.0654)\ln(dist) + (-0.2609s + 0.2675)
\]

\[
L_{\text{two-via}} = (0.1307s - 0.0492)\ln(dist) + (-0.2948s + 0.1943)
\]

\[
L_{\text{three-via}} = (0.1242s - 0.0447)\ln(dist) + (-0.2848s + 0.1763)
\]

\[
L_{\text{four-via}} = (0.1192s - 0.0403)\ln(dist) + (-0.2774s + 0.1592)
\]

\[s = \text{separation between plates (mils/10)}\]

\[dist = \text{distance to via}\]
True Impedance for Decoupling Capacitor

Source

IC

Capacitor

Power

Gnd

L_{IC}

L_{apparent}

L_{cap}

ESR

L_{cap} + L_{IC}

Nominal Capacitance
## Impedance Calculation with Apparent Inductance for Four Decoupling Capacitor Values

### Table: Distance to Cap from IC

<table>
<thead>
<tr>
<th>Cap Value</th>
<th>Case 1</th>
<th>Case 2</th>
<th>Case 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1 uF</td>
<td>800mils</td>
<td>1200mils</td>
<td>1500mils</td>
</tr>
<tr>
<td>0.01 uF</td>
<td>600mils</td>
<td>900mils</td>
<td>1100mils</td>
</tr>
<tr>
<td>0.001uF</td>
<td>400mils</td>
<td>700mils</td>
<td>800mils</td>
</tr>
<tr>
<td>0.0001uF</td>
<td>200mils</td>
<td>400mils</td>
<td>400mils</td>
</tr>
</tbody>
</table>

### Graph: Impedance Calculation with Apparent Inductance

- **Cap Value**: 0.1 uF, 0.01 uF, 0.001 uF, 0.0001 uF
- **Distance to Cap from IC**: Case 1, Case 2, Case 3
- **Frequency (Hz)**: 1E+07 to 1E+09
- **Impedance (ohms)**: 10 to 0.001
- **Lines**:
  - Case 1
  - Case 2
  - Case 3
  - Traditional Calculation
Two Major Questions

- How will structure respond?
- What is the source of the noise?
  - CURRENT!
Predicting the Source of Decoupling Noise

• What is the source?
• ICs need two types of current
  – Current for the I/O drivers
  – “core” current
    • current that does not go out the I/O drivers
• On-going research with Prof Jim Drewniak at UMR
Modeling the Power Current Waveform

- $I_{p2} = \text{shoot through current}$
- $I_{p1} = \text{I/O current} + \text{core current}$
Core Current

\[ I_{p2} = \frac{C_{pd} \times m \times V_{cc}}{\Delta t_2} \]

- \(C_{pd}\) is specified for Clock drivers/buffers
- \(m\) is number of I/O drivers
- \(\Delta t_2 = t_r + t_f\)
I/O Driver Current

• Simple Capacitive Load method
• $C_L = 10$ pF is typical
• $n =$ number of loads
• $\Delta t = t_r$

\[ I_L = \frac{C_L n V_{cc}}{\Delta t / 2} \]
More Accurate I/O Driver Current

• Use Signal Integrity tools to find current waveform
  – Hyperlynx
  – Spectraquest
  – SPICE
Example for Clock Buffers
(Operating at 100 MHz)

<table>
<thead>
<tr>
<th></th>
<th>MPC905</th>
<th>MPC946</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{PD}$</td>
<td>19.5</td>
<td>25</td>
<td>pF</td>
</tr>
<tr>
<td>$V_{CC}$</td>
<td>3.3</td>
<td>3.3</td>
<td>V</td>
</tr>
<tr>
<td>$m$ (number of outputs)</td>
<td>6</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>$n$ (number of loads)</td>
<td>6</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>$t_r$(MAX)</td>
<td>4 V/nS</td>
<td>1.0 nS</td>
<td></td>
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</table>
Motorola MPC905 Results

The theoretical and measured results are plotted against frequency (GHz) and spectrum (dBm) for the Motorola MPC905.
Motorola MPC946 Results

The graph shows the measured and theoretical results for the spectrum of the Motorola MPC946 across different frequencies. The x-axis represents the frequency (GHz) ranging from 0.5 to 3.0, while the y-axis represents the spectrum in dBm, ranging from -90 to 0 dBm. The green circles represent the theoretical results, and the red line represents the measured results.
Sources on Active Board

- Large ASICs do not specify $C_{pd}$
- Measured power/ground plane noise for large ASIC with and without decoupling capacitors installed
- Circuits operating with exerciser software
- Examples for 1.5 volt and 2.5 volt supplies
Power Noise Measured Across C534 (1.5 volt Supply)
With Decoupling Capacitors Installed

Time (seconds)

Amplitude (volts)
Power Noise Measured Across C534 (1.5 volt Supply)
With Decoupling Capacitors Removed
Voltage Histogram
Power Noise Measured Across C534 (1.5 volt Supply)
Power Noise Measured Across C534 (Tvcc 1.5v Supply)
With Decoupling Capacitors Installed
Power Noise Measured Across C534 (Tvcc 1.5v Supply)
With Decoupling Capacitors Removed

Amplitude (dBuv) vs. Frequency (Hz) graph.
Illinois Power Noise Measured Across C533 (2.5 volt Supply)
With Decoupling Capacitors Installed

Amplitude (volts)

Time (seconds)
Illinois Power Noise Measured Across C533 (2.5 volt Supply)
With Decoupling Capacitors Removed
Voltage Histogram
Power Noise Measured Across C533 (2.5 volt Supply)

Voltage
Percentage %

Voltage

Caps
Caps gone
Power Noise Measured Across C533 (2.5 volt Supply)  
With Decoupling Capacitors Installed
Power Noise Measured Across C533 (2.5 volt Supply)
With Decoupling Capacitors Removed

Amplitude (dBuv) vs Frequency (Hz)
To prevent/Reduce Unintentional Signal -- Power Plane Bounce

✓ Distribute Decoupling Capacitors evenly Across entire Board

✓ Capacitor Value not Especially Important!
  – .01 uF or .1 uF the same!
  – Use the largest value of capacitor in the selected SMT Package

✓ Adding ‘high frequency’ capacitors does NOT help, and may HURT at low frequencies!
To prevent/Reduce Unintentional Signal Power Plane Bounce

✓ Provide capacitors near ALL IC power pins for functionality
✓ Avoid routing critical nets through vias
  – This effect requires decoupling between all planes
✓ Consider Alternative Solutions
  – Lossy Decoupling
  – Closely spaced Planes (Increased distributed capacitance)
Summary

- Two different types of decoupling analysis required
  - Transient analysis for functionality
    - Apparent inductance must be included
  - Steady state analysis for EMC
    - Resoance effects important

- Source of power/ground-reference plane noise
  - Current