Low Temperature Integration of Hybrid CMOS Devices on Plastic Substrates

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OUTLINE

- Processing Details
- CMOS Performance
  - NAND, NOR Gates
  - Inverters
- CMOS Reliability
  - Electron and hole Mobility
  - Vt stability
  - Electrical Stress induced degradation
- Summary

Process Details

- Substrates evaluated
  - Thermally stabilized PEN
  - Stainless steel
- Maximum processing temperature: 180^{o}C (nMOS) and 120^{o}C (PMOS)
- Fabrication of a:Si:H-based nMOS devices first, followed by the pentacene-based pMOS devices.
  - a:Si:H TFTs,
    - molybdenum as the gate metal
    - Si_3N_4 as the gate dielectric
    - Aluminum as the source-drain contacts
  - Pentacene- OTFT
    - Aluminum gate the metal
    - Parylene as gate insulator and inter-level dielectric
    - Gold electrodes as source-drain contacts
- The circuits are encapsulated using parylene for passivation with vias opened for device testing.

Why Parylene Gate Dielectric?

Authors	Dielectric	Mean Vt (V)	VTt Std.Dev (± V)	% Std.Dev of V_T
K.P. Pernstich [1]	SiO_2 / OTS	-3.7	1.0	27
I. Kymissis [2]	Parylene	-3.5	1.0	29
K. Diallo [3]	Parylene	-3.5	Not reported	Not reported
J. Puidgollers [4]	PMMA	-15	Not reported	Not reported
This work	**Parylene**	**-2.3**	**0.27**	**12**

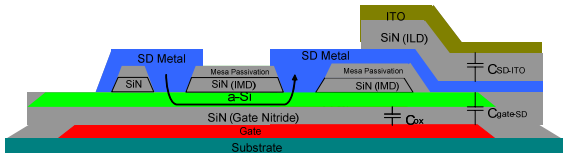
SiO_2 / HMDS / Pentacene	Parylene / Pentacene
• Water contact angle = 60-90°	• Water contact angle = 100-105°
• Unreacted OH on SiO_2 with HMDS/OTS shifts V_T	• OH free surface provides less V_T variation
• Complex, time consuming and batch-batch variation in preparing solution	• Simple CVD process
• V_T variation > 35%	• V_T variation <15% (easier to design circuits with stable gate overdrive)

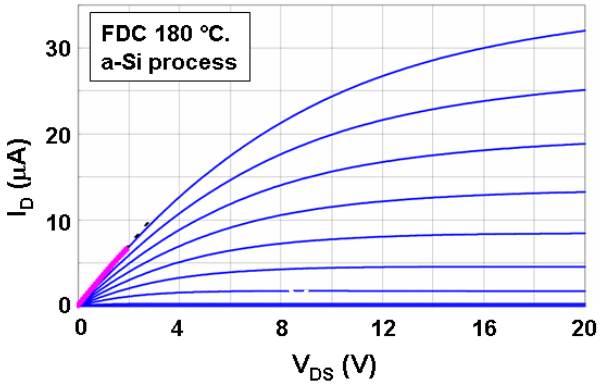
- Using parylene as the gate dielectric allows Vt variation to <15%
- Low Vt variation critical for circuit design..

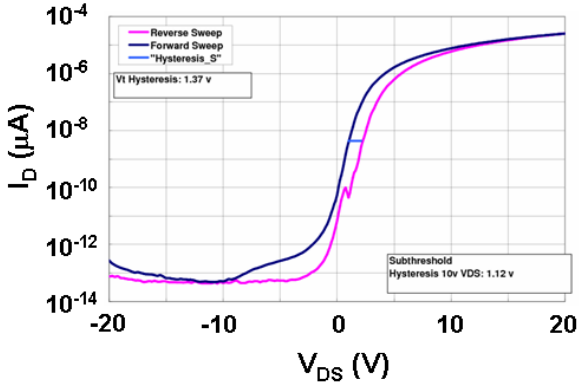
[1] J. Appl. Phys. **96,** 11 (2004), [2] Journal of Display Technology **1,** 2 (2005), [3] Appl. Phys. Lett. **91,** 183508 (2007), [4] Organic Electronics **5,** 67 (2004).

nMOS and pMOS Performance

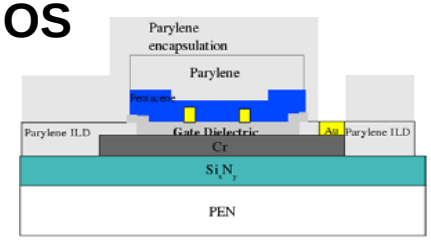
NMOS

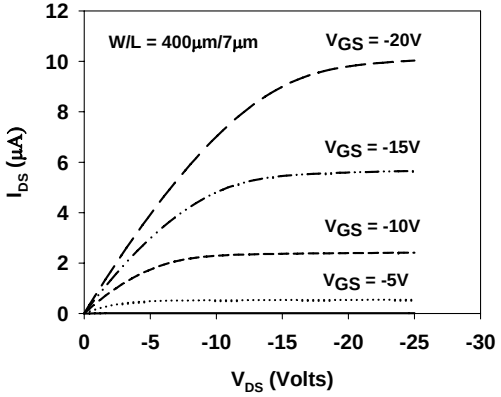


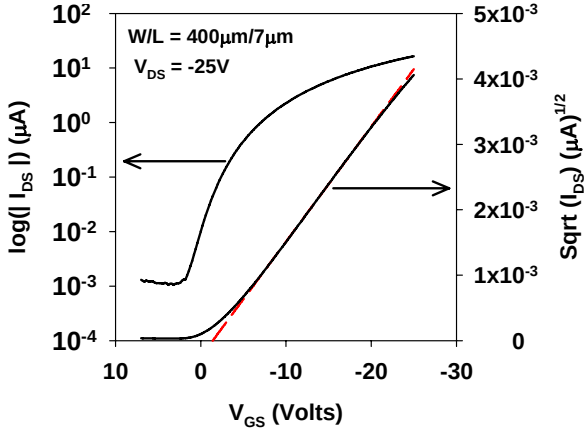




PMOS

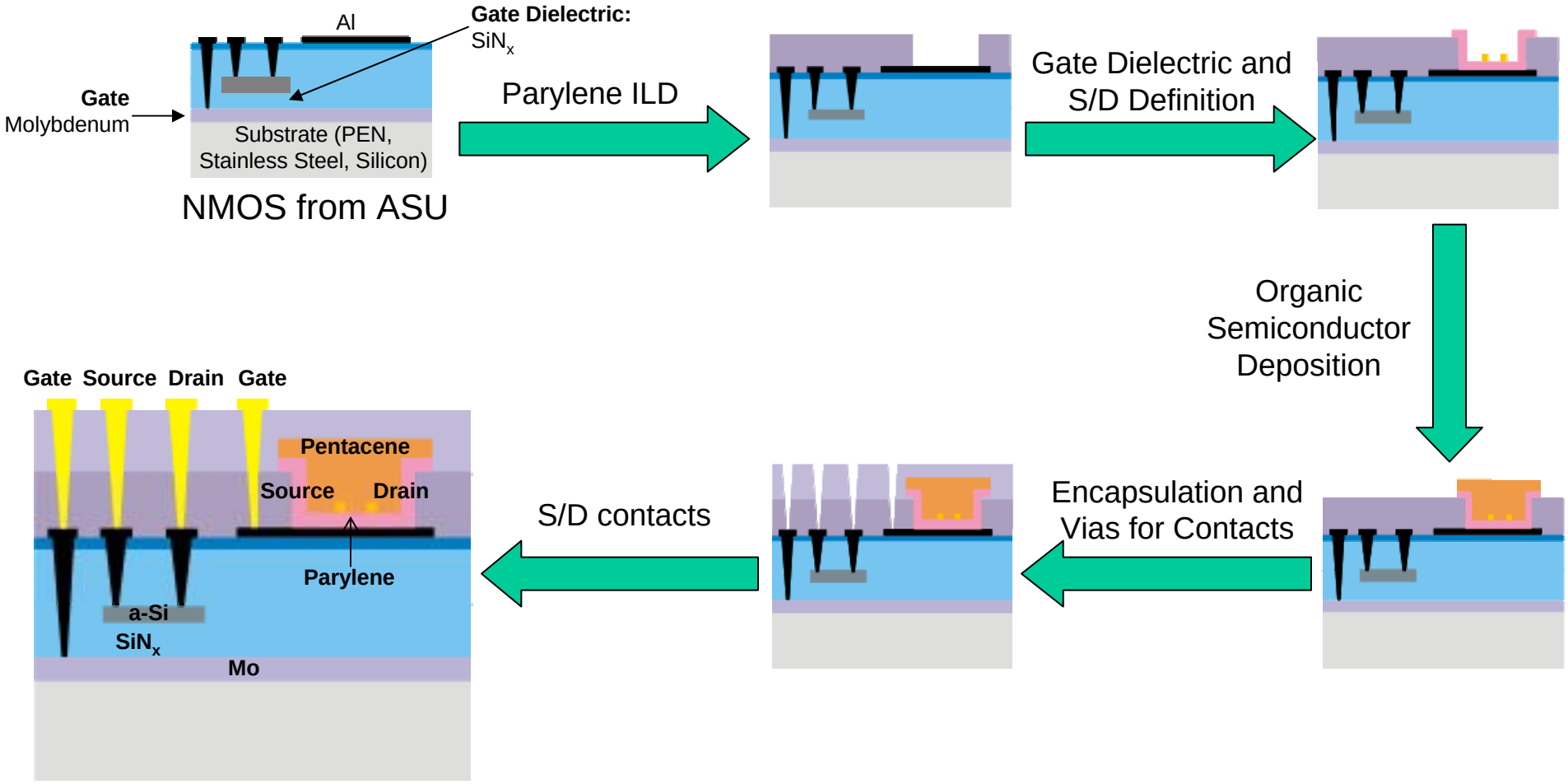




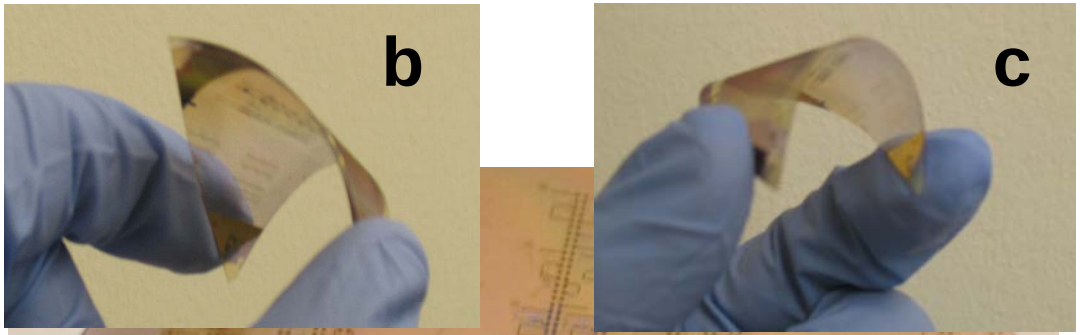


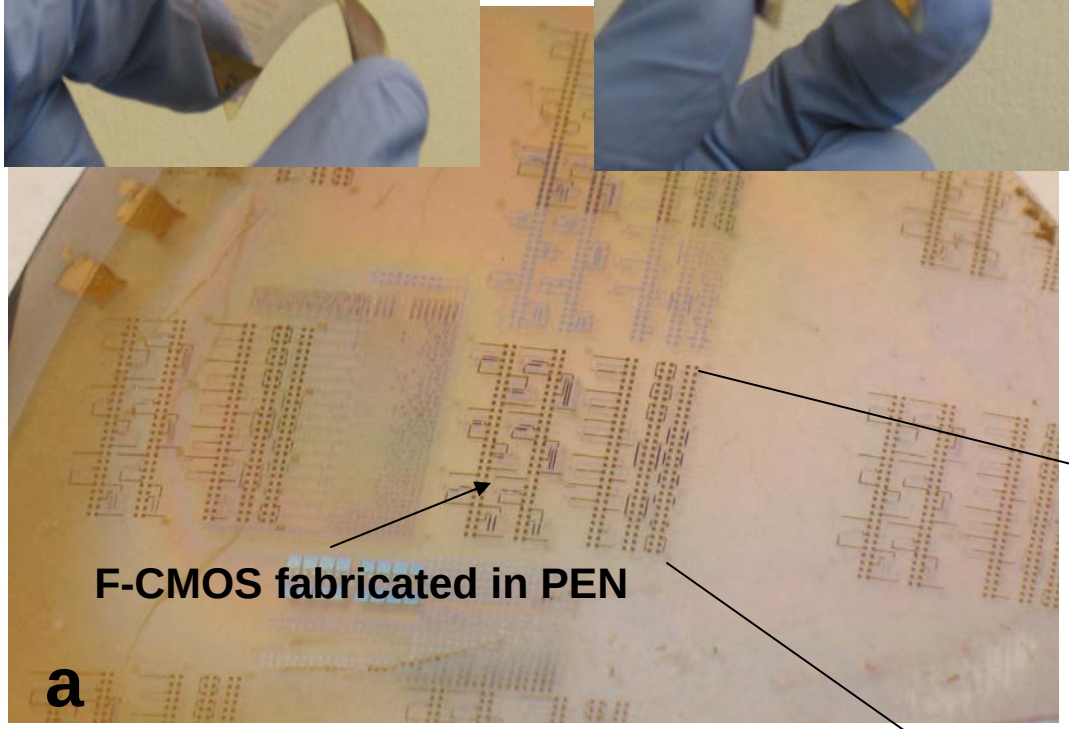
- **Why CMOS**
  - –Dramatically reduced power consumption
  - –Analog circuitry possible with CMOS operational amplifiers
- **Flexible CMOS**
  - – N-Type a-Si:H TFTs (FDC)
  - – P-type OTFT based (UTD)
  - – OTFTs fabricated after a-Si:H TFTs
  - – Standard Cell Approach

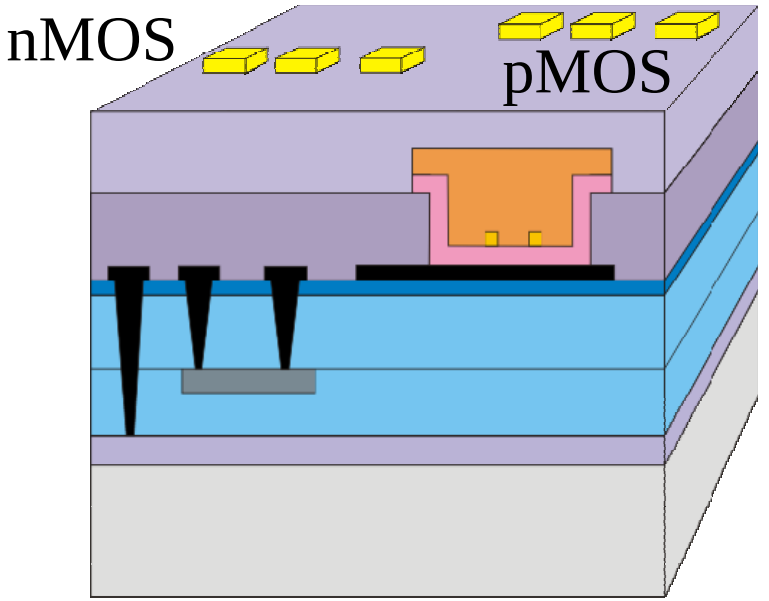
Process Integration

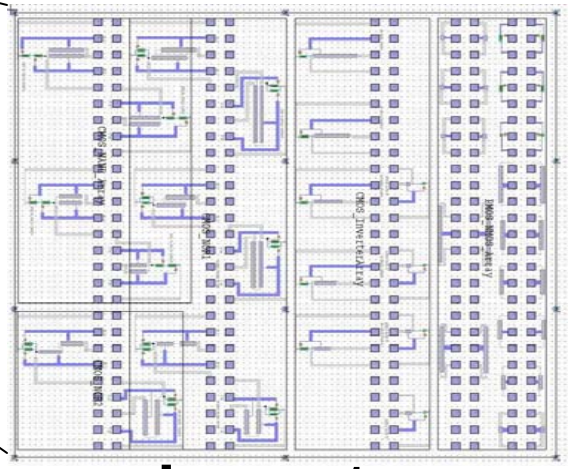


Flexible CMOS





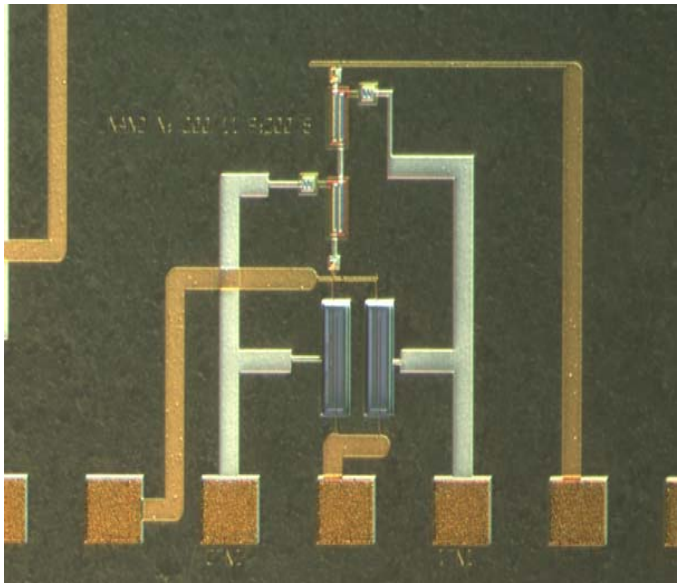




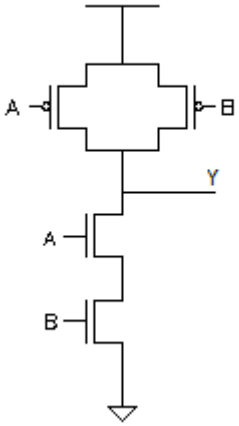
Layout

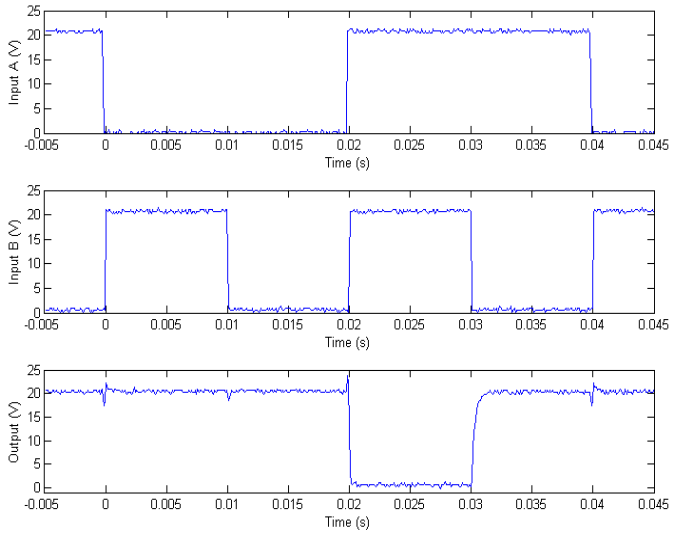
- Die consists of logic gates, inverters and ring oscillators
- All processing Temperature < 180C
- Die size ~ 0.75 cm2

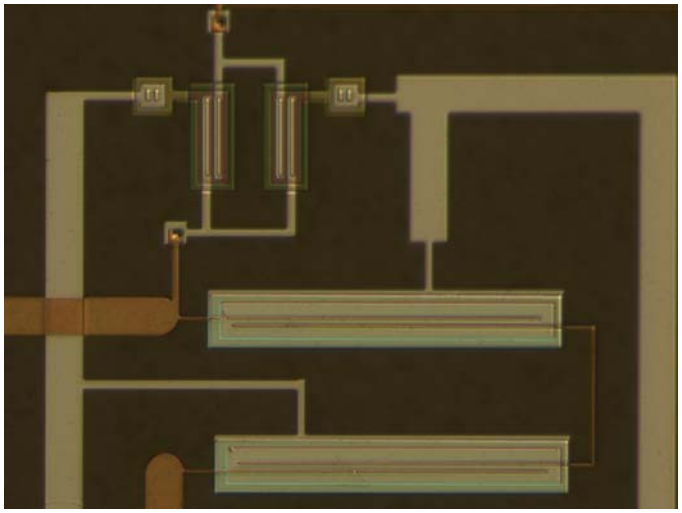
CMOS NAND and NOR Gates



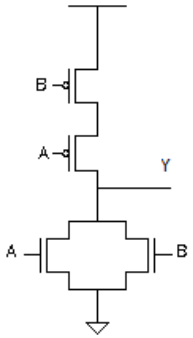
NAND Gate

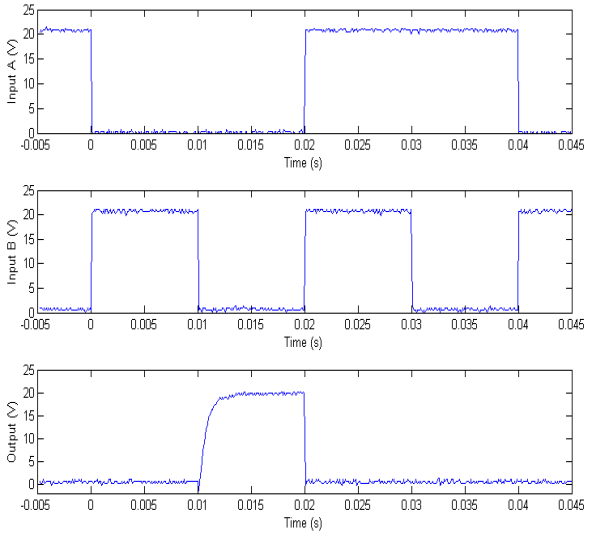




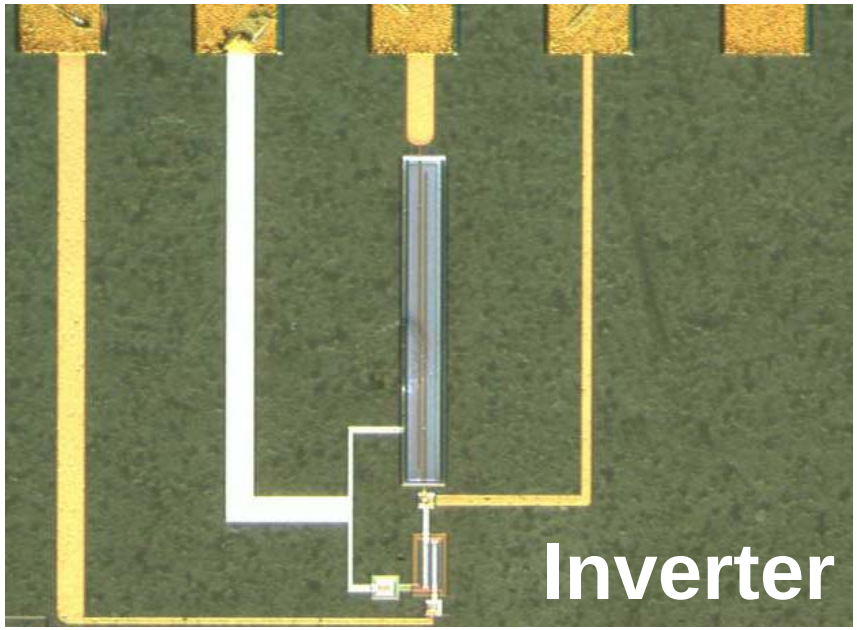


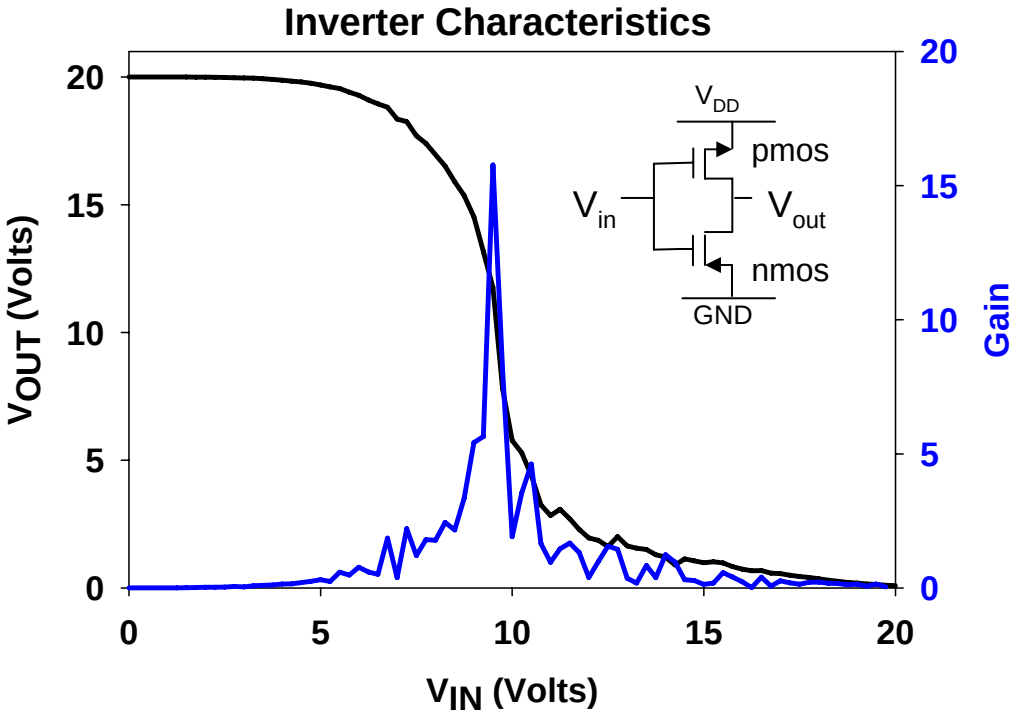
NOR Gate

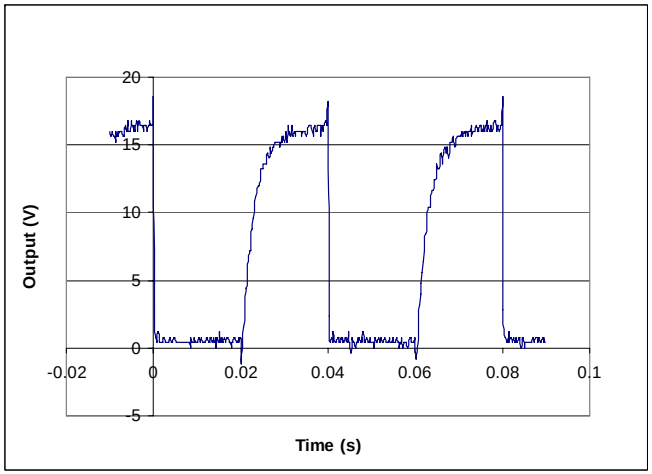




CMOS Circuits on PEN - Inverter







- **Inverter swings rail-rail**
- **Inverter Gain ~ 16 at $V_{DD}/2$**
  - **V_{DD} = 20V**

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  - Inverters
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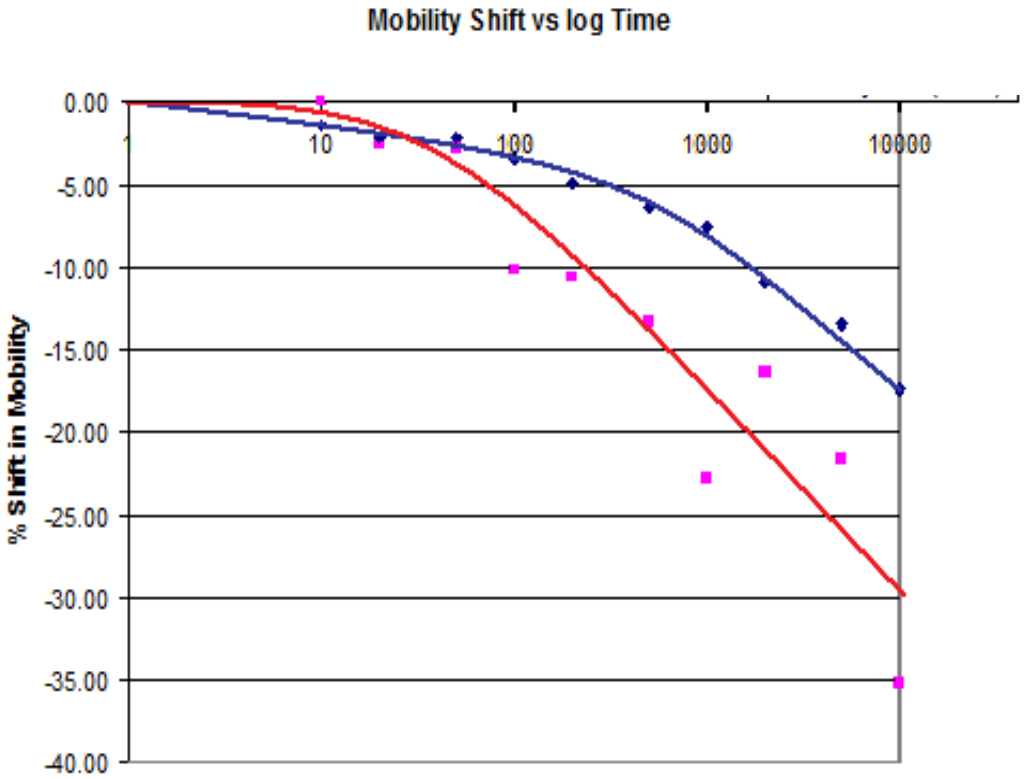
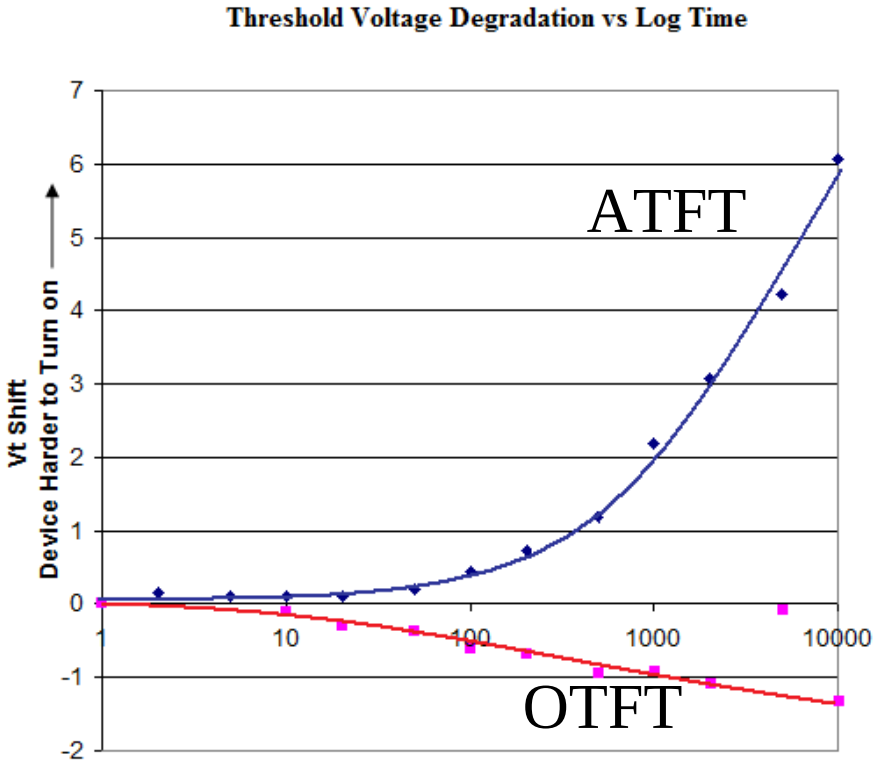
  - Vt stability
  - Electrical Stress induced degradation
- Summary

Mobility and VT Stability

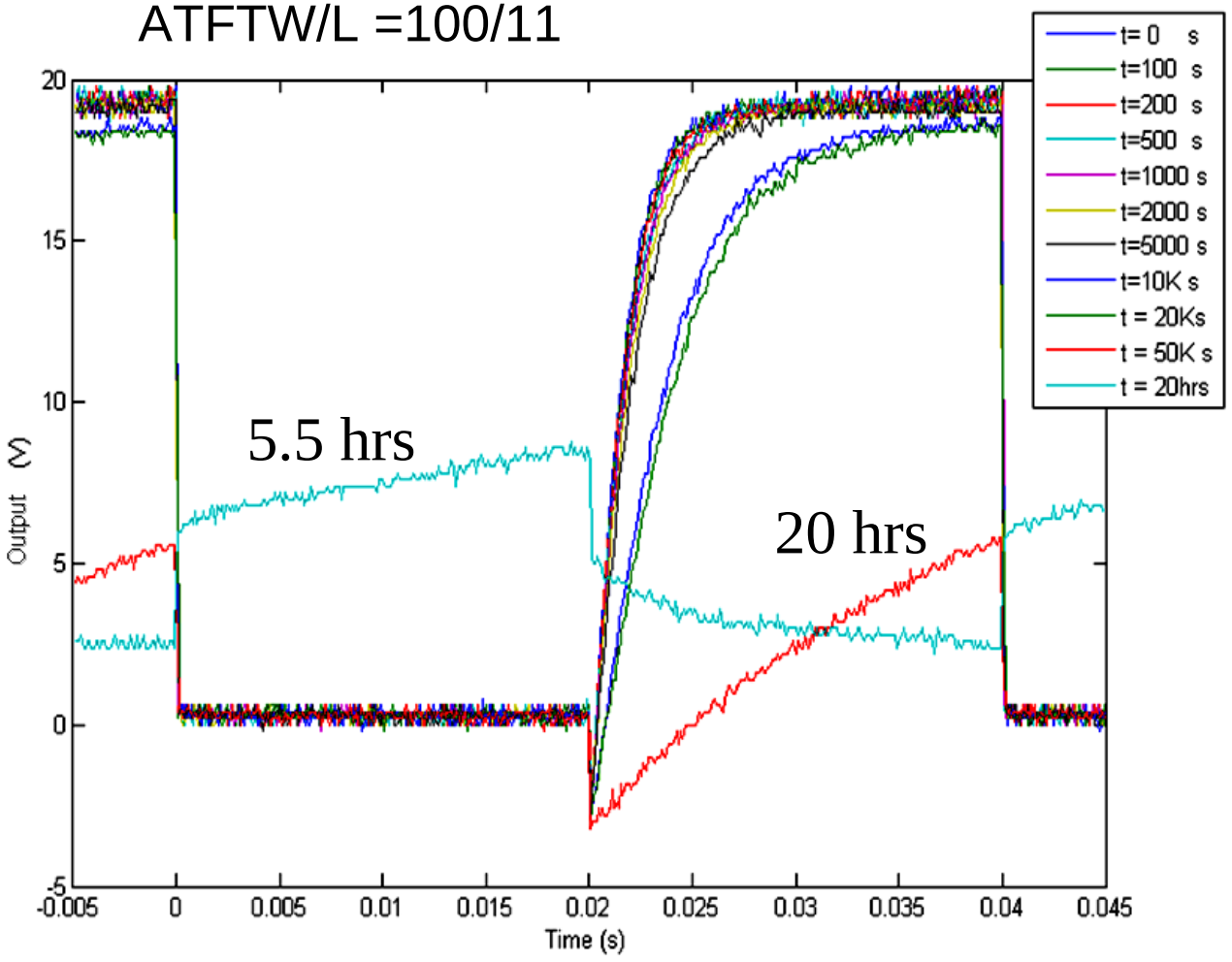




- OTFT mobility decreases from 0.083 cm^2/V-s to 0.053 cm^2/V-s (**35%)**
- ATFT mobility decreases from 0.354 cm^2/Vs to 0.298 cm^2/V-s (**15%)**
- OTFT V_T shifts in the positive direction → Easier to turn on
- ATFTs V_T shifts in the positive direction → Harder to turn on.

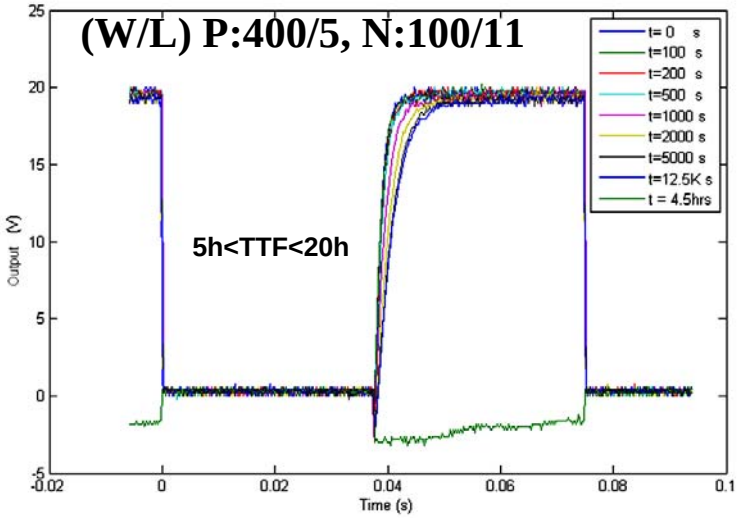
Transient Stress Measurements: inverters

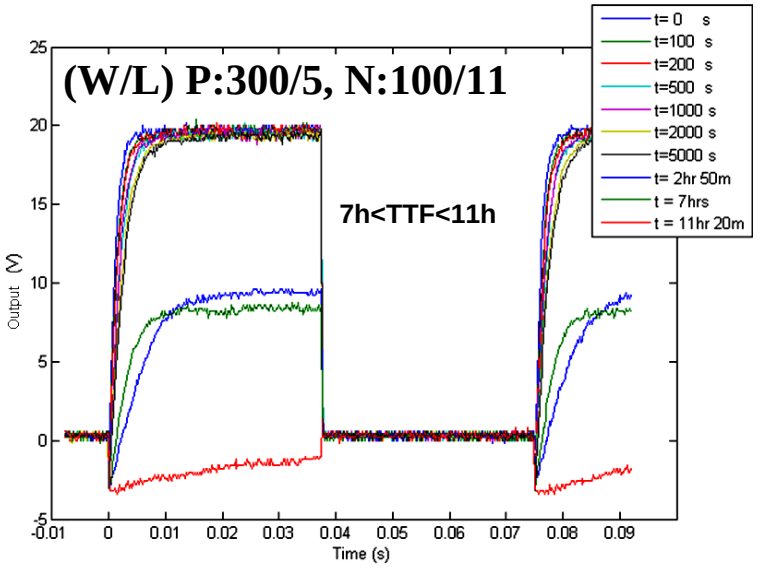
OTFT WL= 200/5
ATFTW/L =100/11

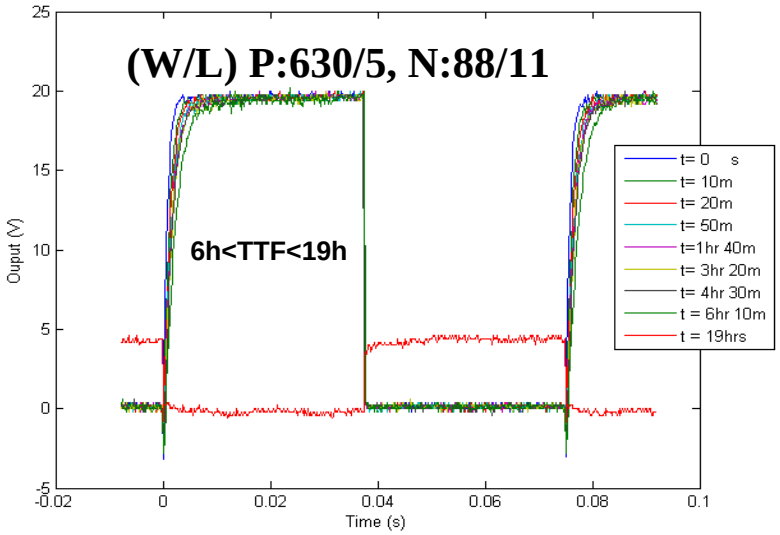


- Inverter subjected to 50% duty cycle
  - 40 ms period, 20V p-p pulse waveform, at V_{DD}=20V
- failure of the device happens in between 5.5-20hrs

Inverter Stress Results as Function of nMOS/PMOS W/L Ratio

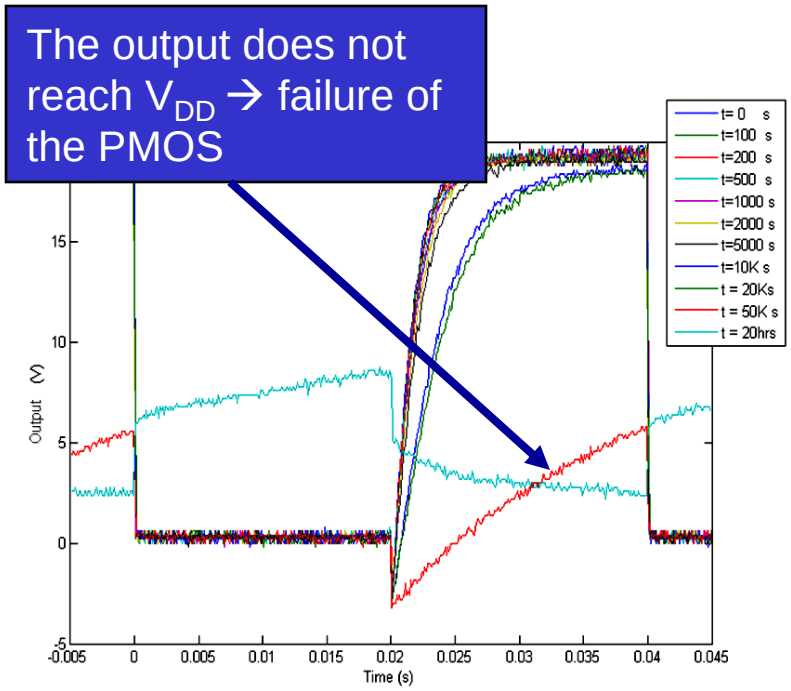




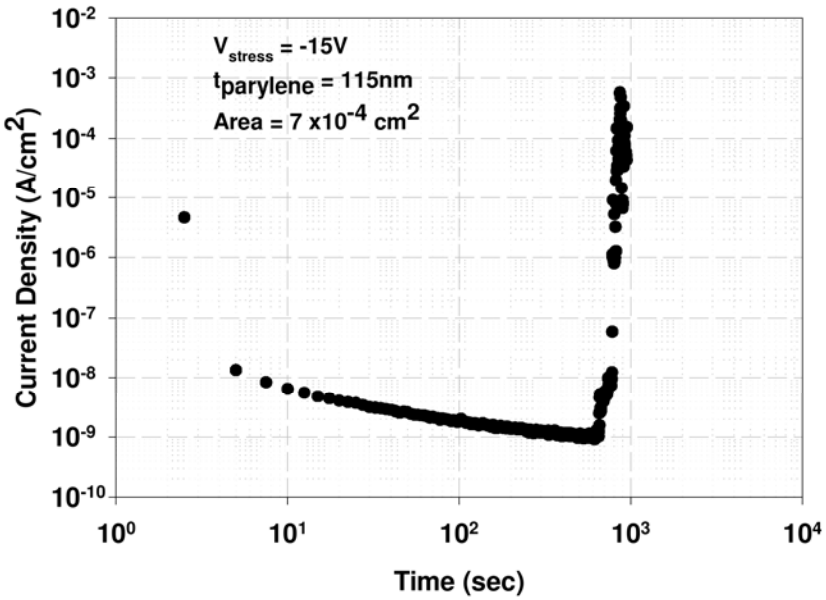


- Transient output of several CMOS on Flexible substrates
- All devices failed between 7-20hrs

pMOS Failure Mechanism



TDDB for Parylene Gate Dielectric



- Gate dielectric (OTFT) likely breaking down after stress

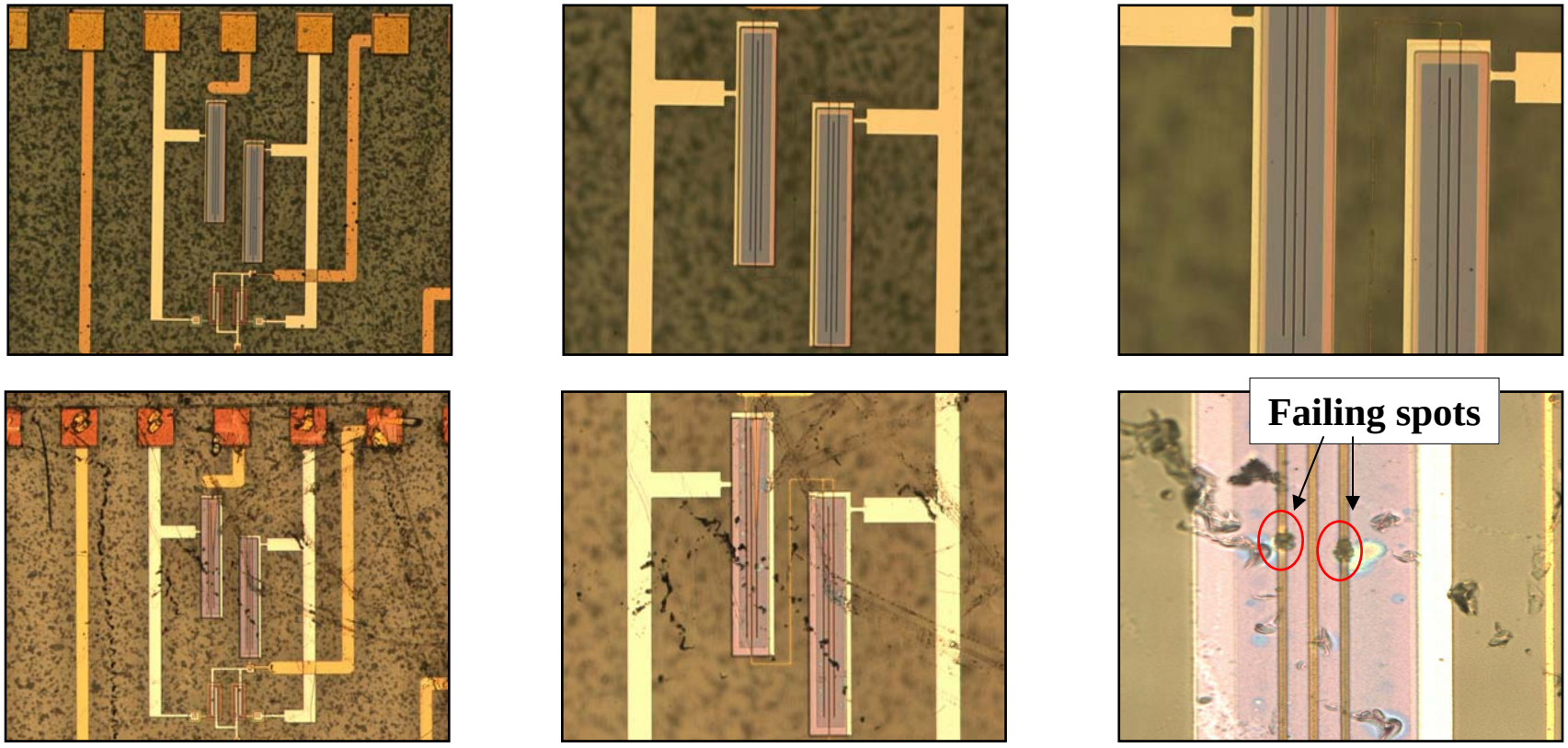
Evidence of pMOS Gate Dielectric Breakdown

NAND Gates

Increasing Magnification

Not Stressed

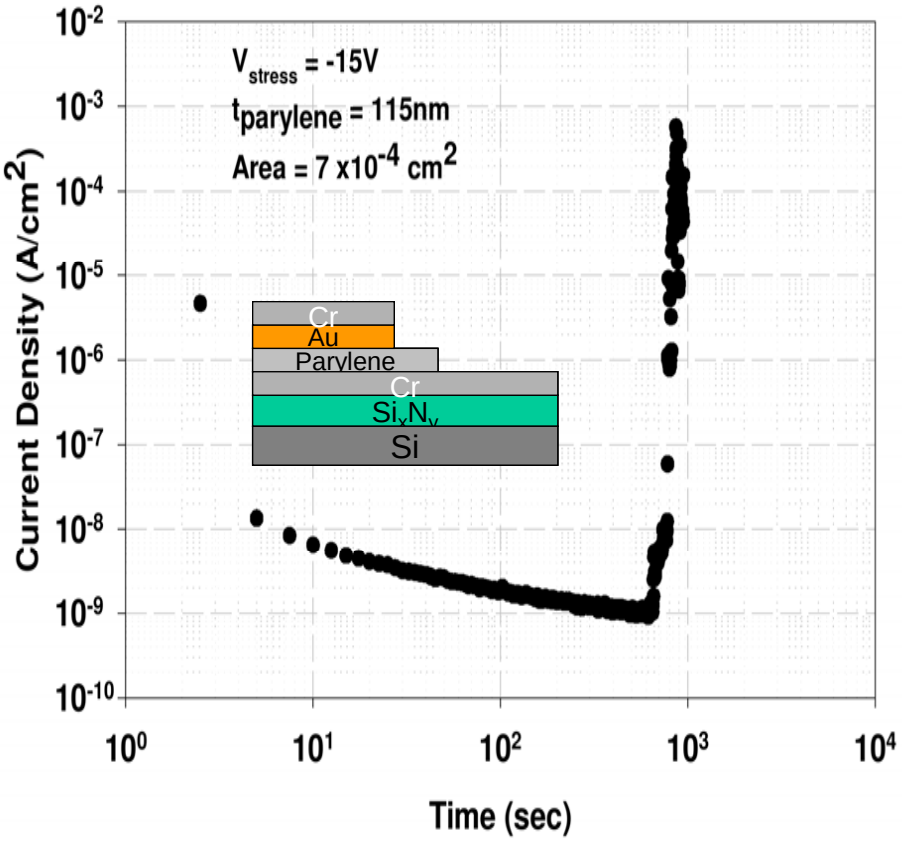
Stressed



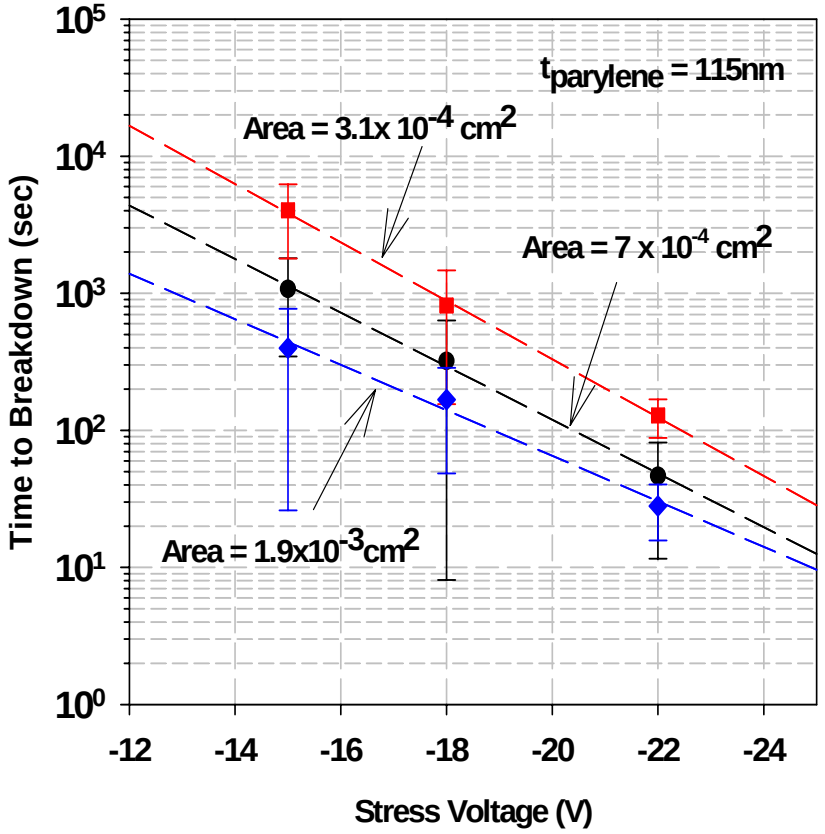
- Source of gate dielectric breakdown likely due to defects in the dielectric
- Currently evaluating alternate organic, inorganic and hybrid dielectrics to improve gate dielectric reliability

Reliability - TDDB of Parylene

Typical Results



TDDB as Function of Device Area



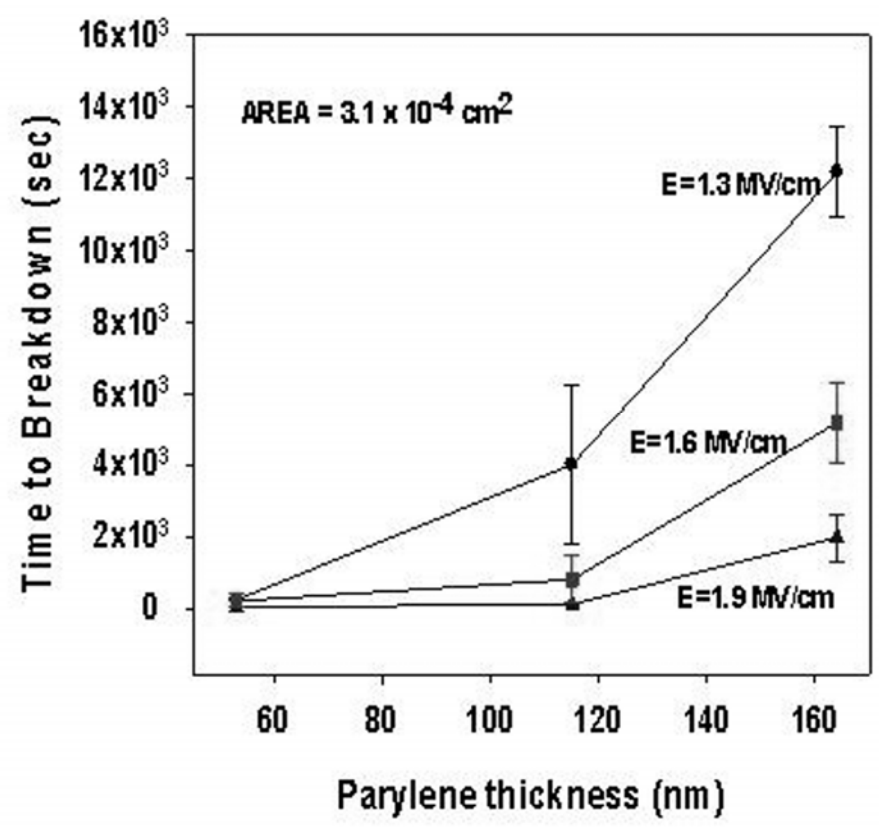
- Time to breakdown ~ 10x initial current
- Area dependence ➡ defects dominated

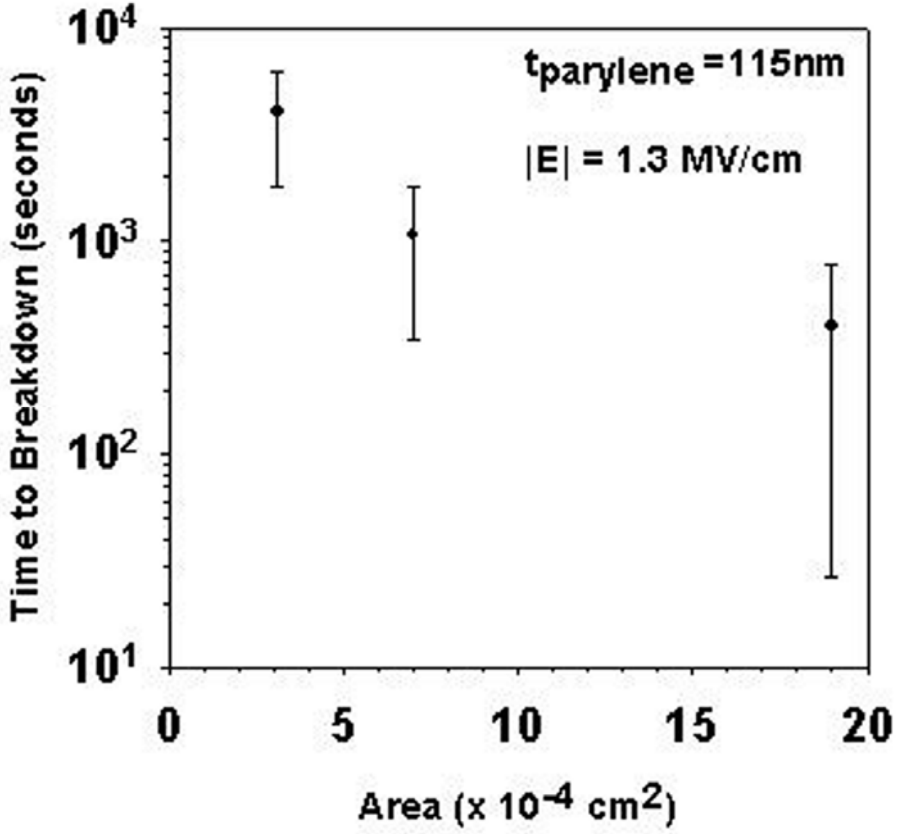
$t_f \propto V^{-n}$

n~ 5-9

n- strongly depends on area and thickness

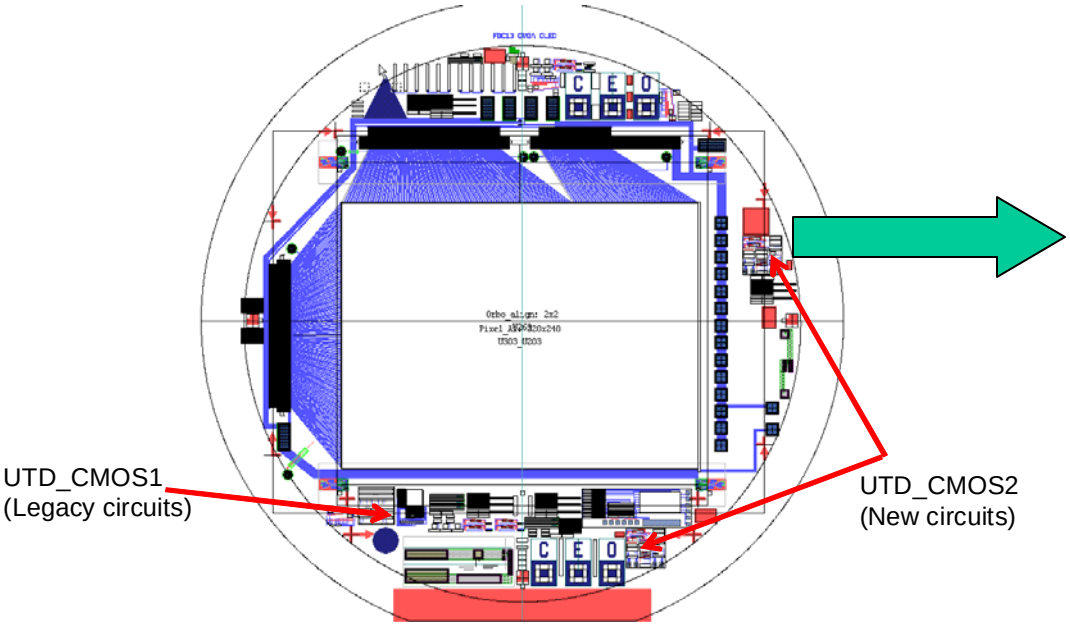
Reliability - TDDB of Parylene

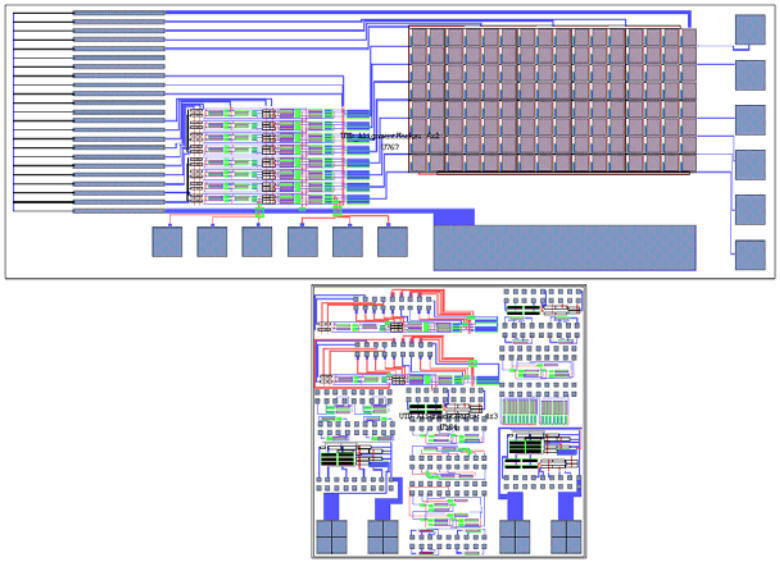




- TDDB of thin parylene show field dependence
  - Predominantly determined by the number of defects
- Lifetime extracted from power law dependence > 1000hrs operating under stress conditions (W/L of 1000µm/6µm and fixed gate bias of -10V)

Devices Under Fabrication





- Legacy circuits
  - nMOS, pMOS TFTs
  - Inverters
  - NANDs
  - NORs
- New Circuits
  - Opamp
  - Integrated column drivers
  - Column drivers with 16x8 display
  - Ring oscillators
  - Latches and FlipFlops

Summary

- CMOS circuits on flexible substrate have been demonstrated
  - **nMOS a-Si:H** (maximum processing temperature <180C)
  - **pMOS Pentacene** (maximum processing temperature <120C)
- Inverters (gain of 16) and two input NAND and NOR gates with logic function demonstrated
- Electrical stress degradation of the CMOS circuits indicates that gate dielectric (pMOS) causes device failure
  - Currently evaluating alternate gate dielectrics for pMOS
- CMOS devices currently under fabrication include:
  - Op-amp, Bias circuit, Integrated column drivers, column drivers, ring oscillators, latches and flipflops