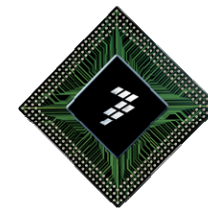


Through Silicon Via Stress Characterization



May 19th , 2009

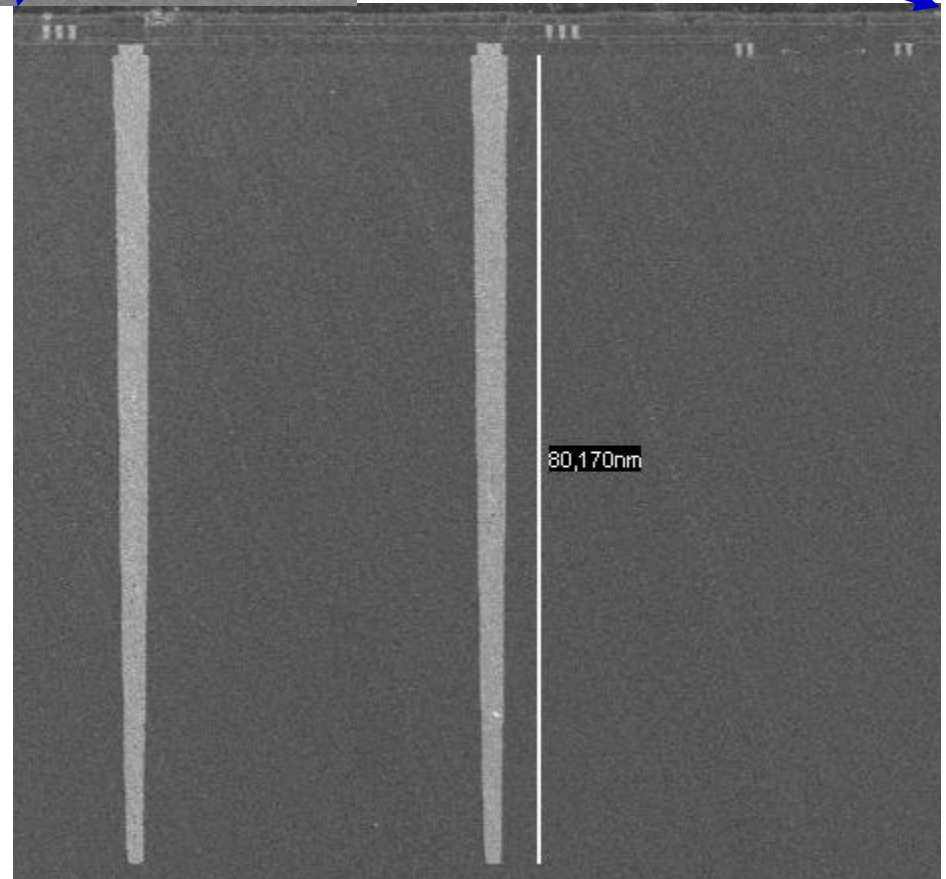
Thuy Dao, Dina Triyoso, Mike Petras, Michael Canonico

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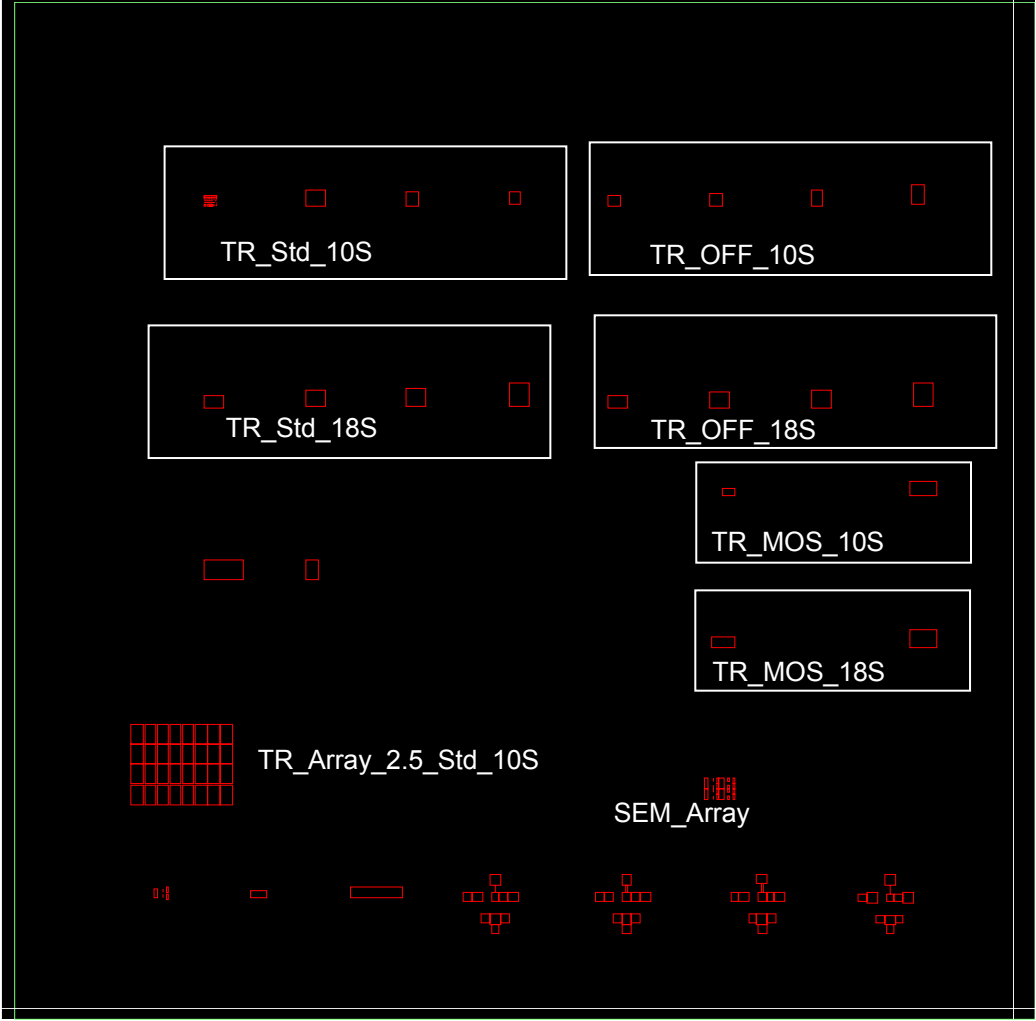
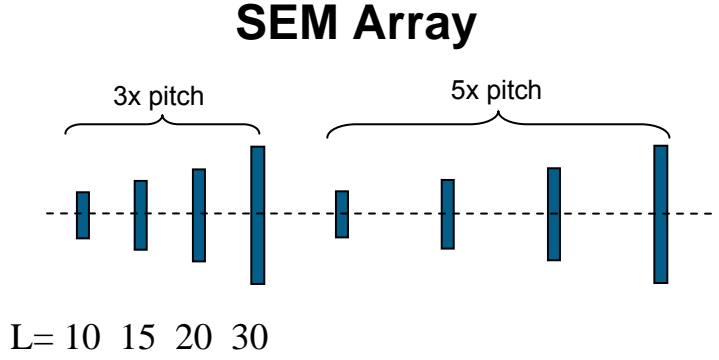
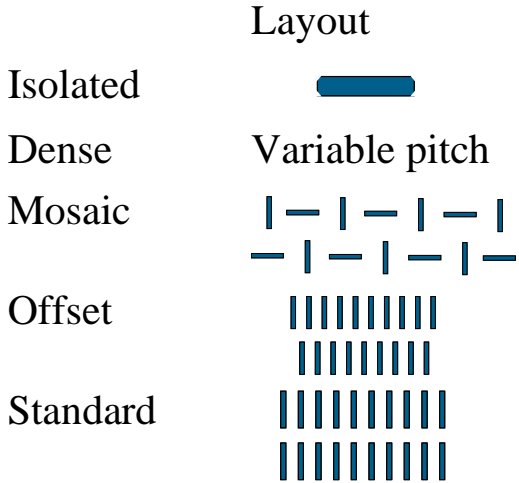


Through Silicon Via

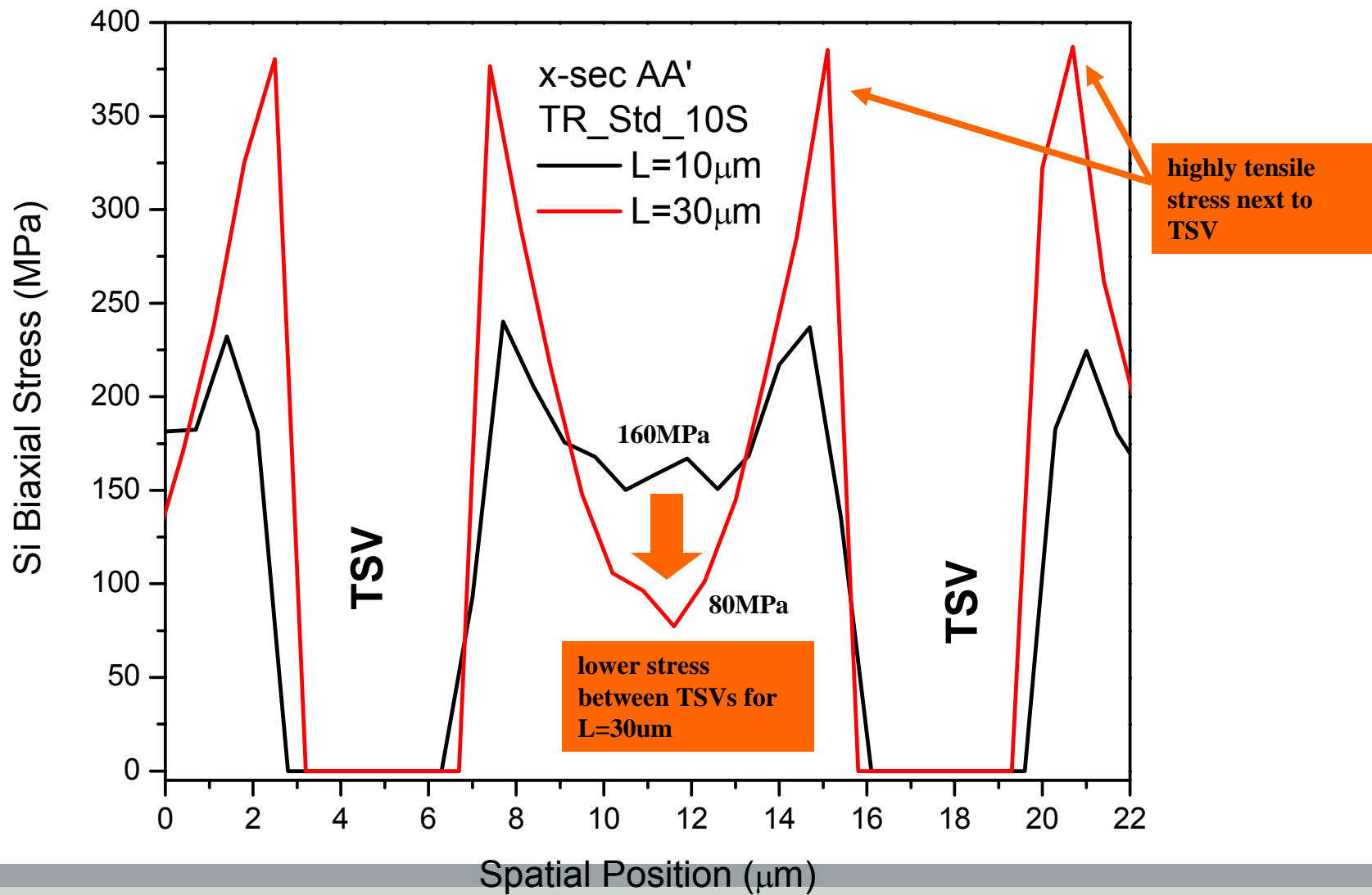
- Through Silicon Via (TSV) has been shown to deliver reduced inductance compared to traditional wire bond.
- W is chosen as filling material.
- The coefficient of linear expansion (CTE) mismatch between W and Si is rather large at ~3ppm and therefore CTE induced stress is expected.
- The induced stress can have an impact on the performance of any structures which might be located near the TSV.
- Understand the stress introduced by the TSV for purposes of selecting the appropriate materials and layout.
- UV-Raman spectroscopy was used to map the spatial distribution of stress in the Si surrounding the TSV structures as a function of TSV length and spacing & type of arrays.
- Spectrometer: UV-upgraded Dilor XY800 in additive configuration; Laser line: 364nm Ar-Ion, 10mW, 100x obj.; Detector: LN2 cooled and UV-enhanced (2048x512) CCD

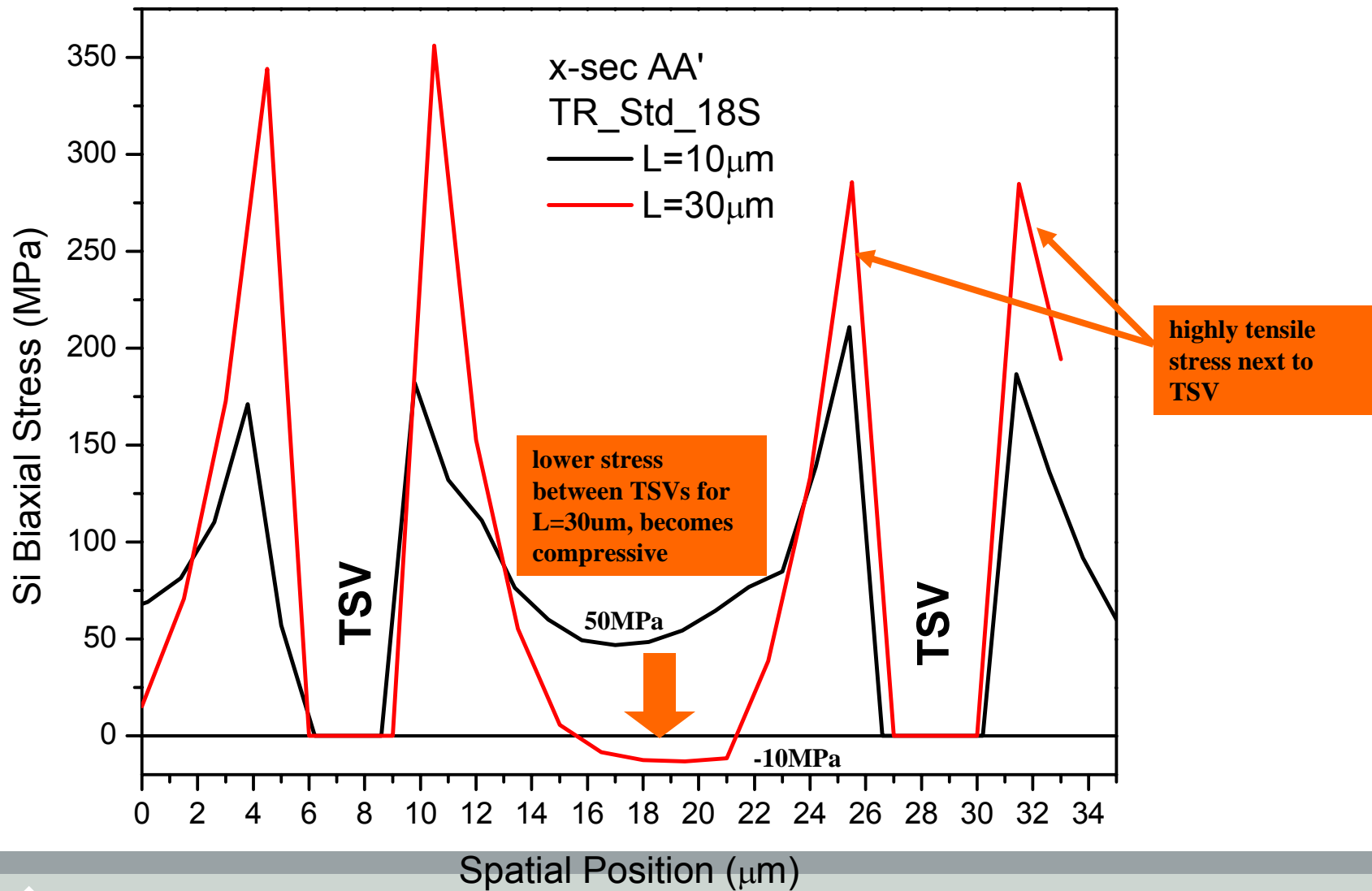


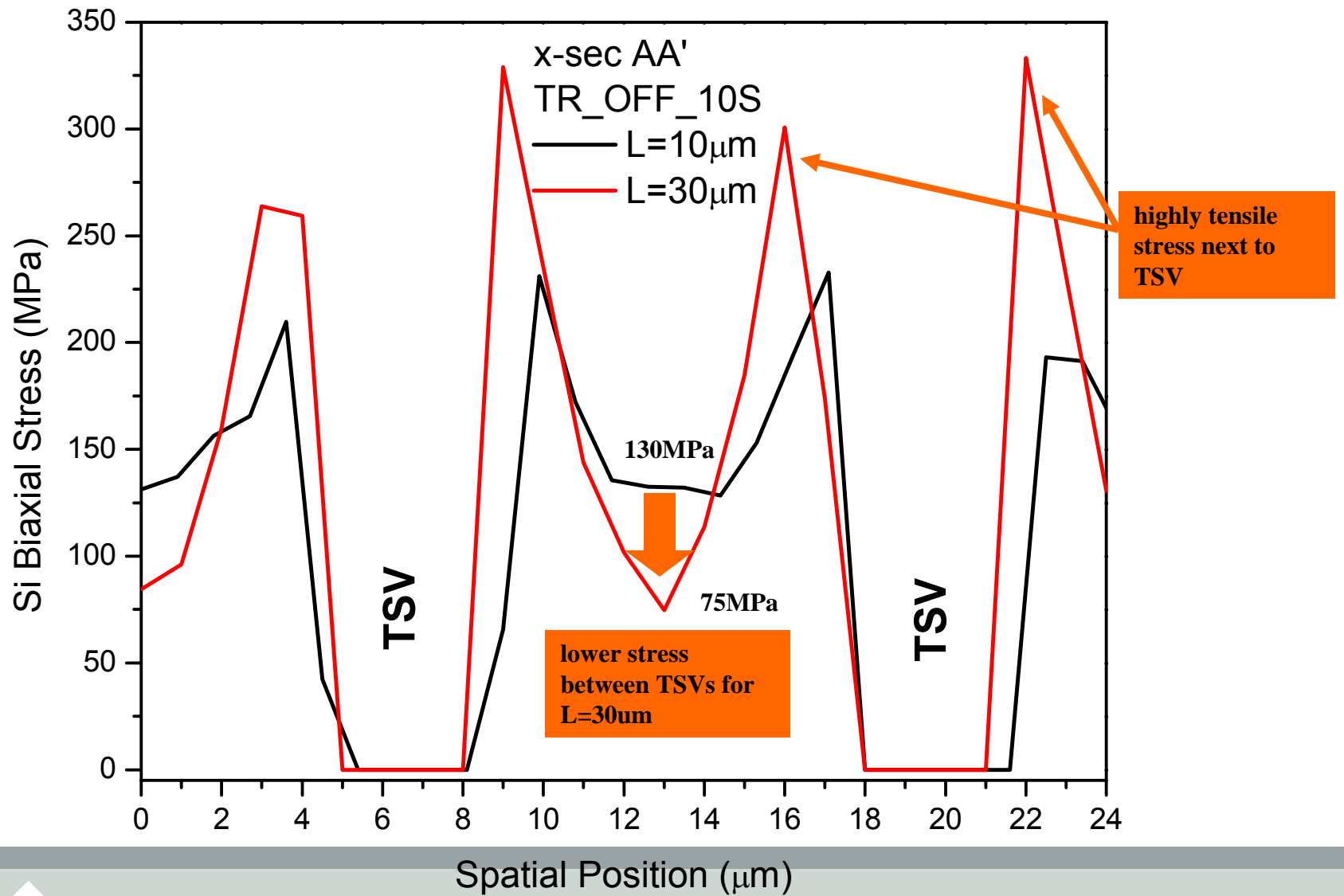
Through Silicon Via Structures

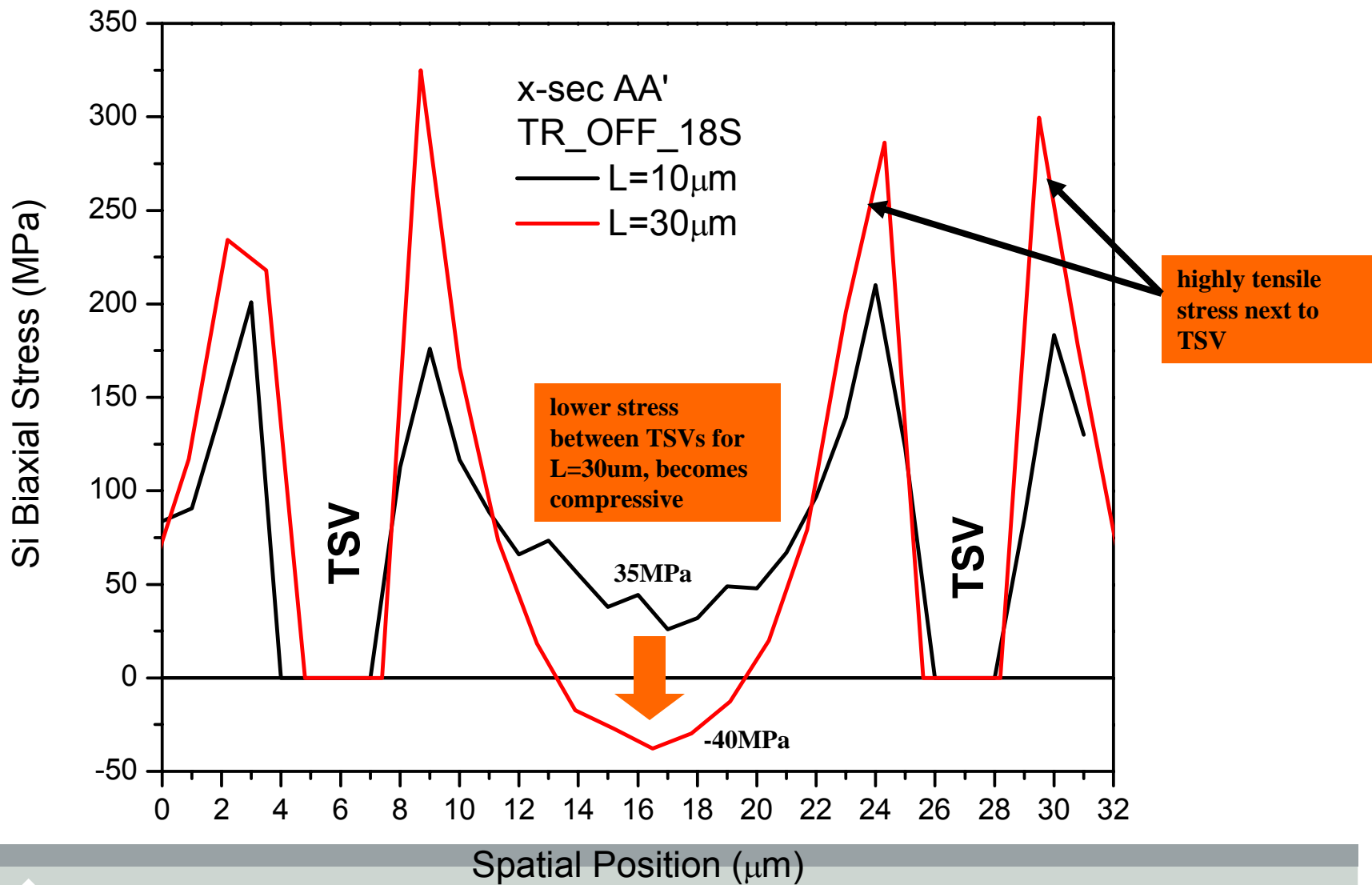


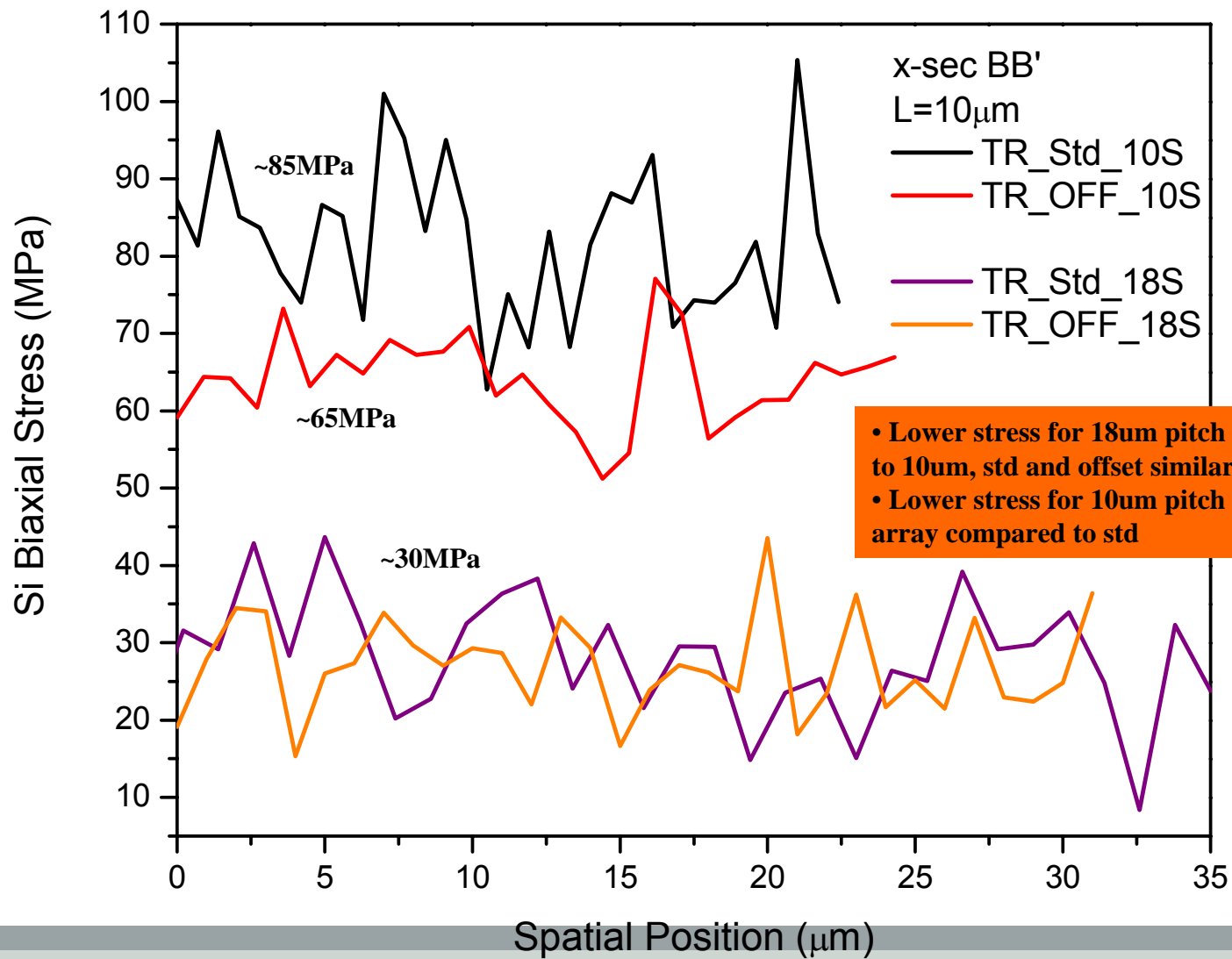
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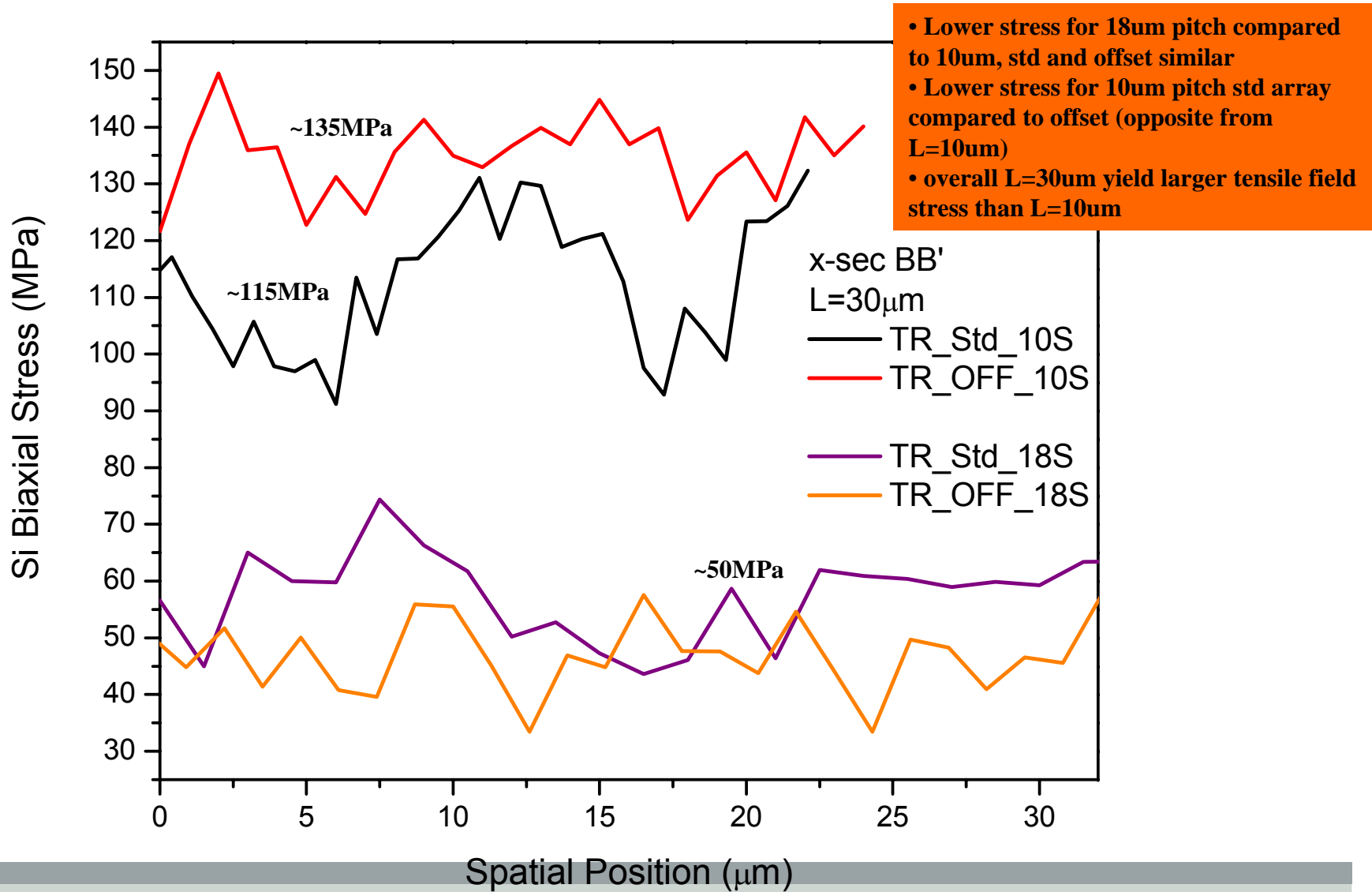




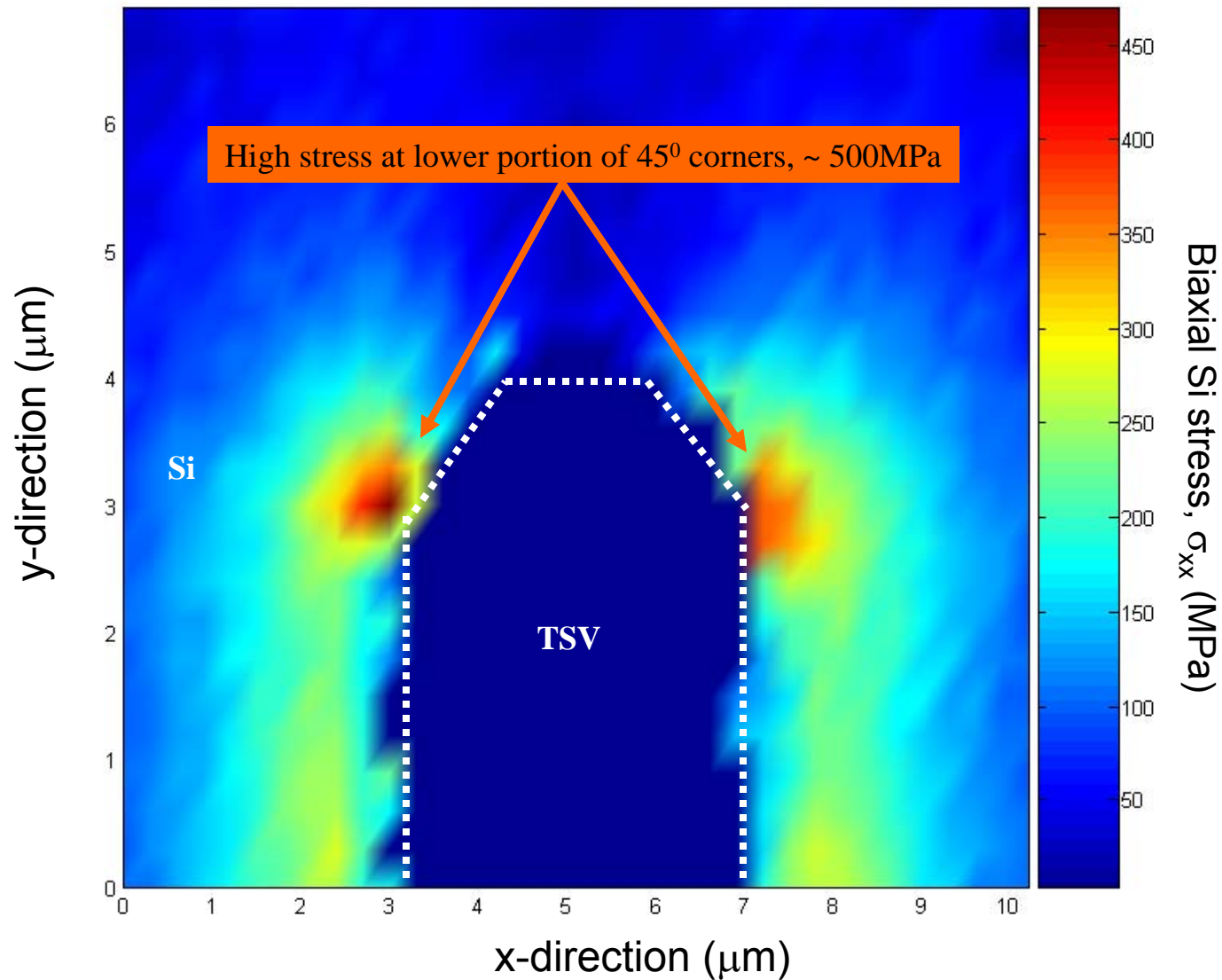








Map 17 – SEM(10,20,30), L=30



Summary

- ▶ Raman Stress Measurements for standard and offset arrays with TSV lengths of 10 & 30um at 10 & 18um pitch.
- ▶ Tensile biaxial stress typically extends perpendicular to trench shape TSVs for tens of microns but not along the length of the trench.
- ▶ Longer trench TSVs generate higher tensile stress in neighboring Si than shorter trench TSV.
- ▶ Long TSVs generate lower tensile stress in the field perpendicular to TSV which becomes compressive for the standard and offset geometries with 18um space .
- ▶ Offset geometry reduces tensile field stress compared to standard geometry.
- ▶ Highest stress points on linear TSVs are located at the two ends of the via.

