# Where the Noise Starts
# – PWB Design –

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# REFERENCES


[1] Personal Communications (Michael King):
- •August 1987 –Discussions concerning PWB Board Resonance phenomenon with respect to its effect on Common-mode (CM) currents, as well as CM current minimization via appropriate PWB-to-chassis grounding and connector placement.
- •August 1991 –Discussions on CM current generation effects due to reference planes cuts located under signal traces along with an explanation of PWB inductance, also the effect of vias and traces on decoupling capacitor resonance as well as signal trace "Reference Flipping".

[2] Ott, *Noise Reduction Techniques in Electronic Systems,* Pages 296 and 297, Wiley and Sons 1988, ISBN 0-471-85068-3.

[3] Dockey, "Asymmetrical Mode Radiation from Multi-layer Printed Circuit Boards", pages 247 – 251, *Conference Proceedings of EMC/ESD International Symposium*, Denver Colorado, April 22-24, 1992, published by Cardiff Publishing Company.

[4] Dockey & German, "New Techniques for Reducing Printed Circuit Board Common-mode Radiation", pages 334 – 339, *Proceedings 1993 IEEE Symposium on Electromagnetic Compatibility*, Dallas, Texas August 9-13, 1993.

[5] Leferink & Van Doorn, "Inductance of Printed Circuit Board Ground Planes", pages 327 – 329, *Proceedings 1993 IEEE Symposium on Electromagnetic Compatibility*, Dallas, Texas August 9-13, 1993.

[6] Ott, "Ground Plane Inductance", Paper presented to Rocky Mountain Chapter, EMC Society 1994

[7] Leferink, "Reducing Radiation Emissions by the Application of SNT", page 469, *Proceedings 1994 IEEE Symposium on Electromagnetic Compatibility*, Chicago, Illinois August 22-26, 1994.

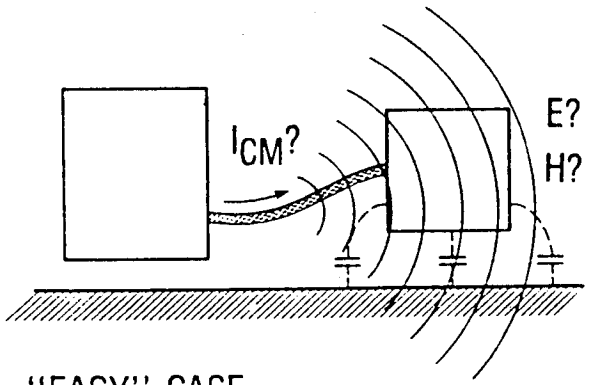
[8] Holloway and Kuester, "Net and Partial Inductance of a Microstrip ground Plane", *IEEE Transactions on Electromagnetic Compatibility*, volume 40, number 1, pages 33-45, 1998.

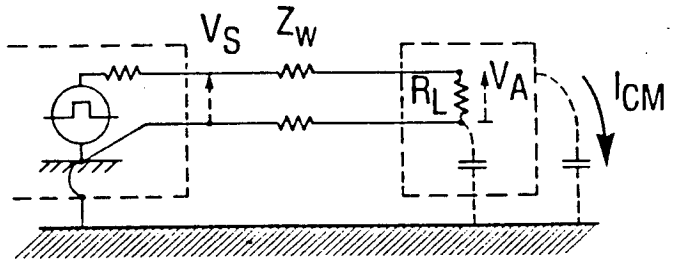
[9] Ott, "Ground Plane Inductance [update]", Paper presented at: *EMC '99 – ARIZONA A Colloquium and Exhibition on Pre-Compliance EMC Testing problems and Solutions* sponsored by Phoenix chapter of the IEEE EMC, May 1999.

# PWB TOPICS

- Board and Board plus Cable Resonance
- Ground Plane Inductance
- Ground Plane Inductance "Drivers"
  (The Noise Makers)
- Mitigation Techniques (as time and interest permits)

# CM RADIATION FROM I/O CABLES




I. "EASY" CASE

RADIATION CAUSED BY THE I/O SIGNAL ITSELF

*Extracted from Interference Control Technology lecture notes (created approximately 1987). Author was* Michel Mardiguian.

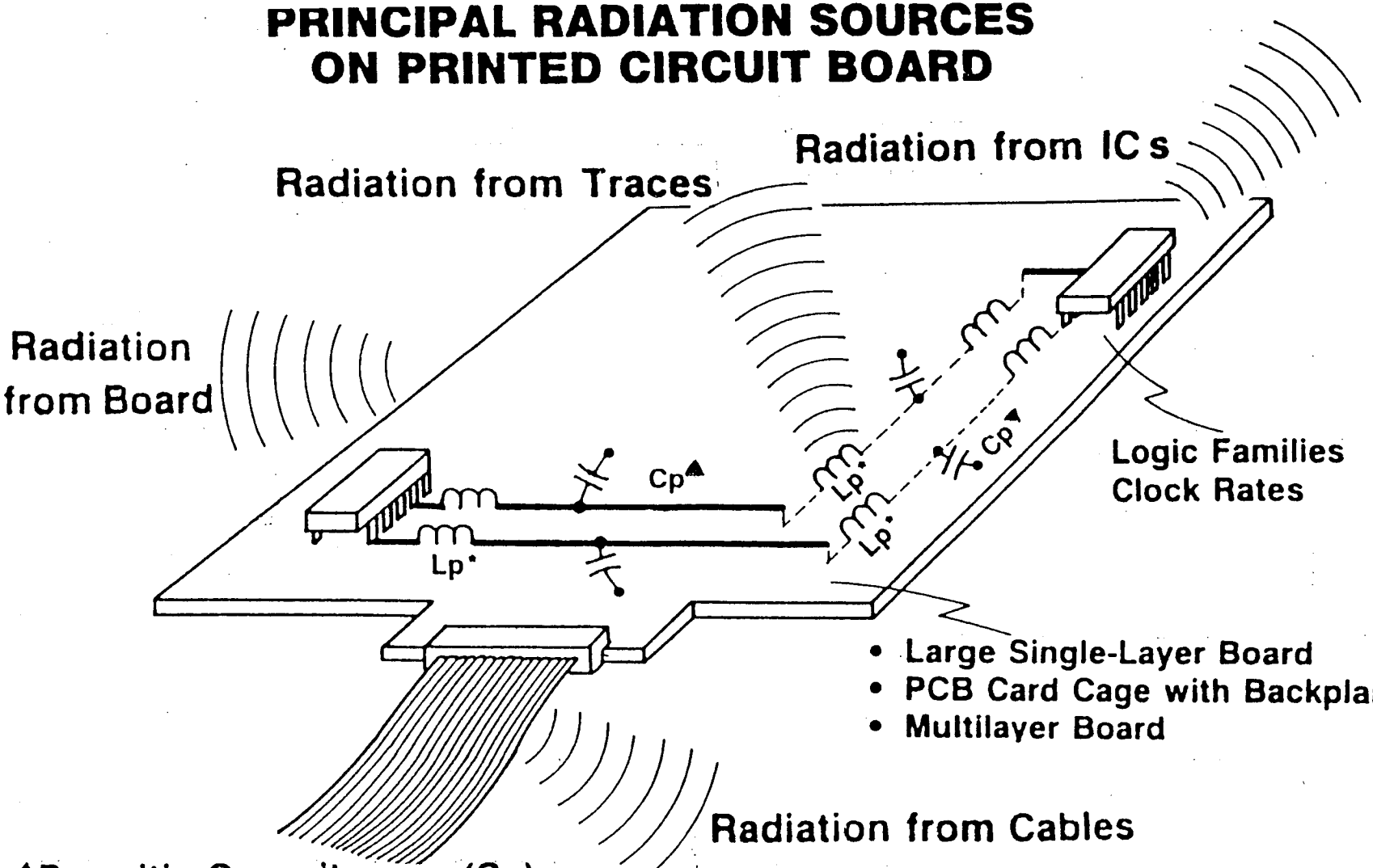
- THE LARGEST UNBALANCED CURRENT COMES FROM THE "HOT" SIDE OF $R_L$ (UNLESS THE WHOLE SYSTEM IS PERFECTLY BALANCED)
- THEREFORE A GOOD APPROXIMATION OF $I_{CM}$ IS:

$$I_{CM} \cong \frac{V_A}{Z_{Loop}} = \frac{V_S}{Z_W + Z_{float}}$$

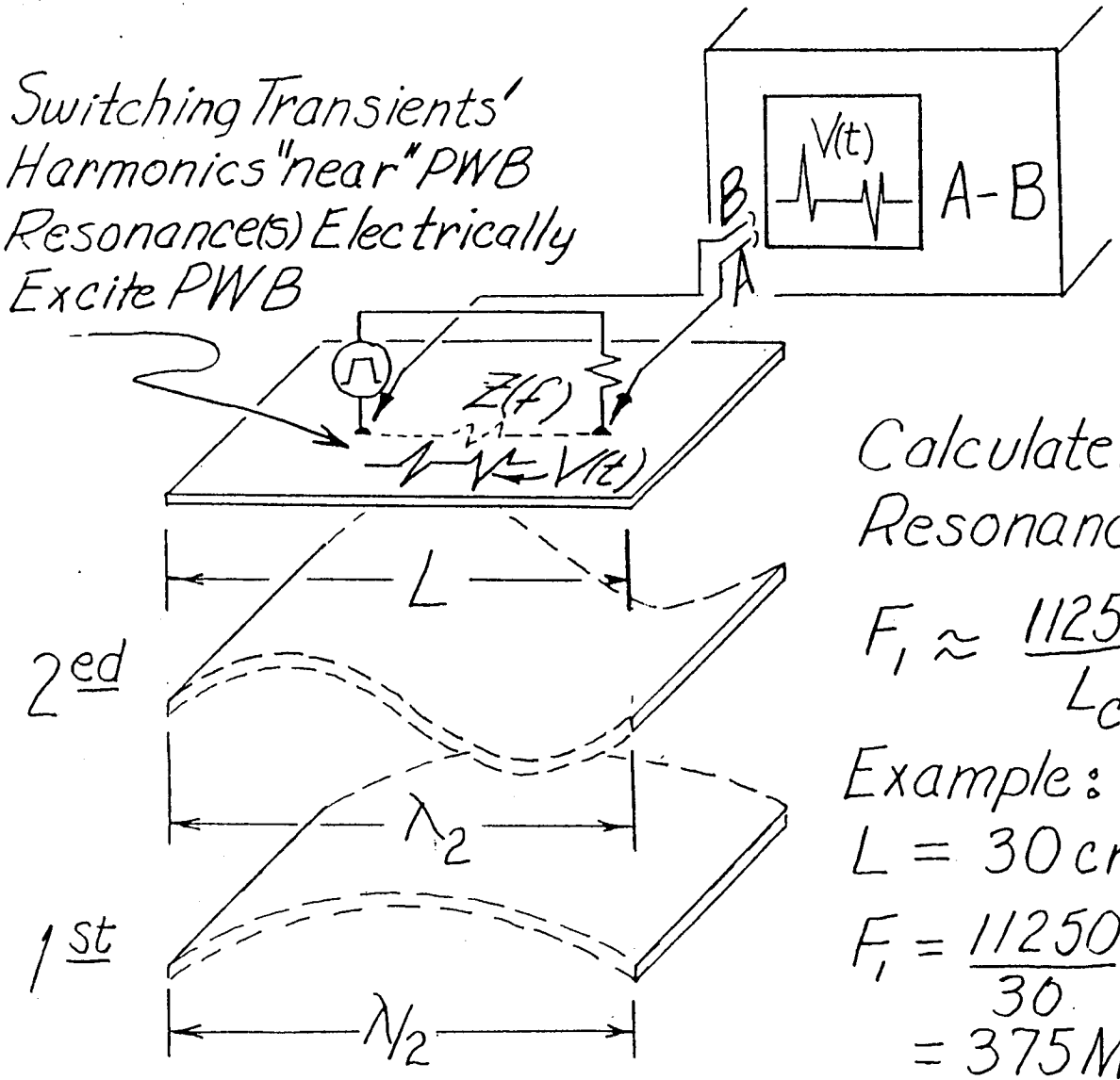
WHERE $Z_{float}$ IS THE CIRCUIT TO GROUND IMPEDANCE OF LOAD SIDE; IF THE LOAD IS GROUNDED, THE LOOP IMPEDANCE IS MINIMAL

- RADIATION IS COMPUTED USING $V_S$, $Z_{Loop}$ AND LOOP AREA AS INPUTS

# PRINCIPAL RADIATION SOURCES ON PRINTED CIRCUIT BOARD




▲Parasitic Capacitances (Cp) and Inductances (Lp) Result in Resonances that Enhance Radiations at Certain Harmonics.




Calculate PWB Resonance:

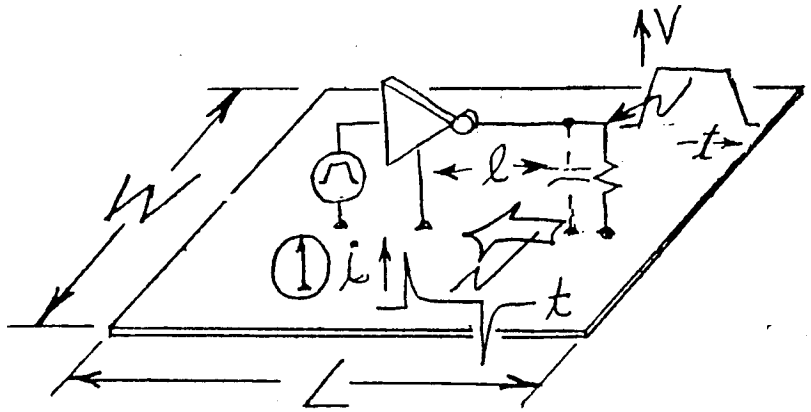
$$F_1 \approx \frac{11250}{L_{cm}}$$

Example:

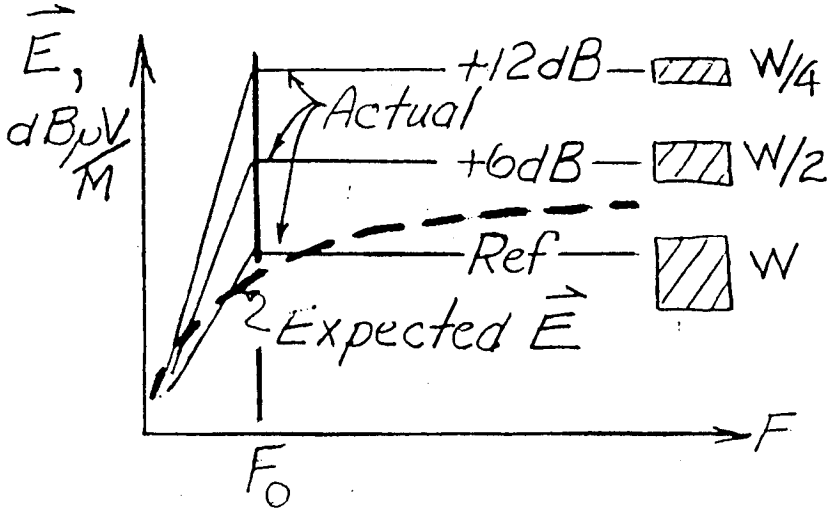
$L = 30\,cm$

$$F_1 = \frac{11250}{30} = 375\,MHz$$

PWB RESONANCE



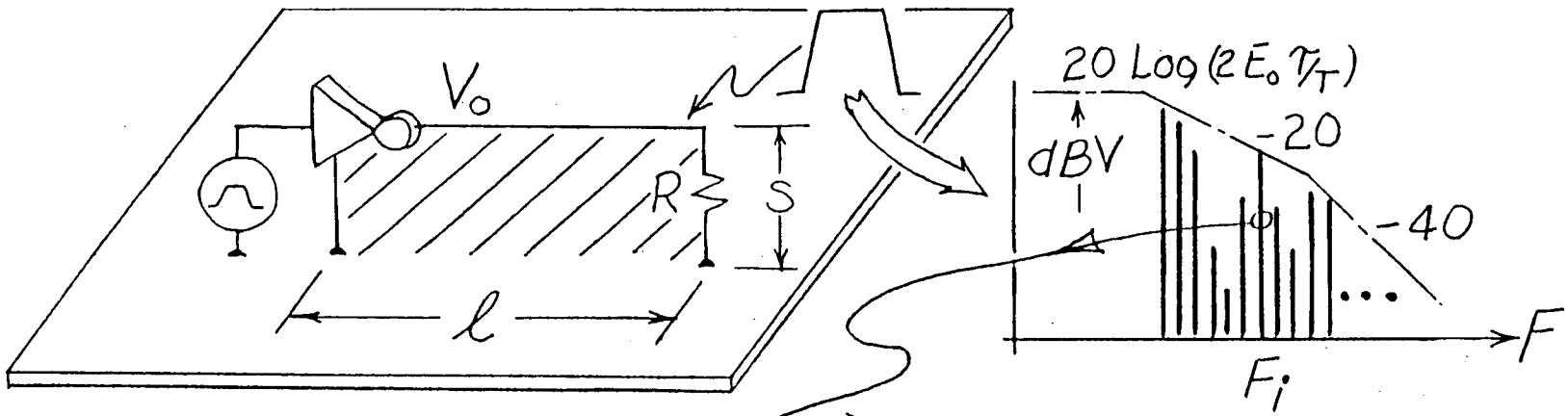

WIDTH(W) – As W decreases, Radiated Emissions Climb. Can Express as Function of ratio of L/W: Gain over Square Board $\approx 20 \log(L/W)$




LENGTH(L) – Board Length Sets Resonance. Signal Traces Excite Total Board Via Harmonically Rich Current Pulses ①. Board Resonance($F_0$) is:

$$F_{0,MHz} \approx \frac{11250}{L_{CM}}$$

PWB Emission Model




$$\Delta\ |\vec{E}| = \frac{1.3A}{r}\left(\frac{V_o}{Z}\right)\left(F_i\right)^2$$

$|\vec{E}|$ - Far Field at Distance r, $\mu V/m$

A - Area of Loop, S x ℓ, $cm^2$

r - Distance to Antenna, m

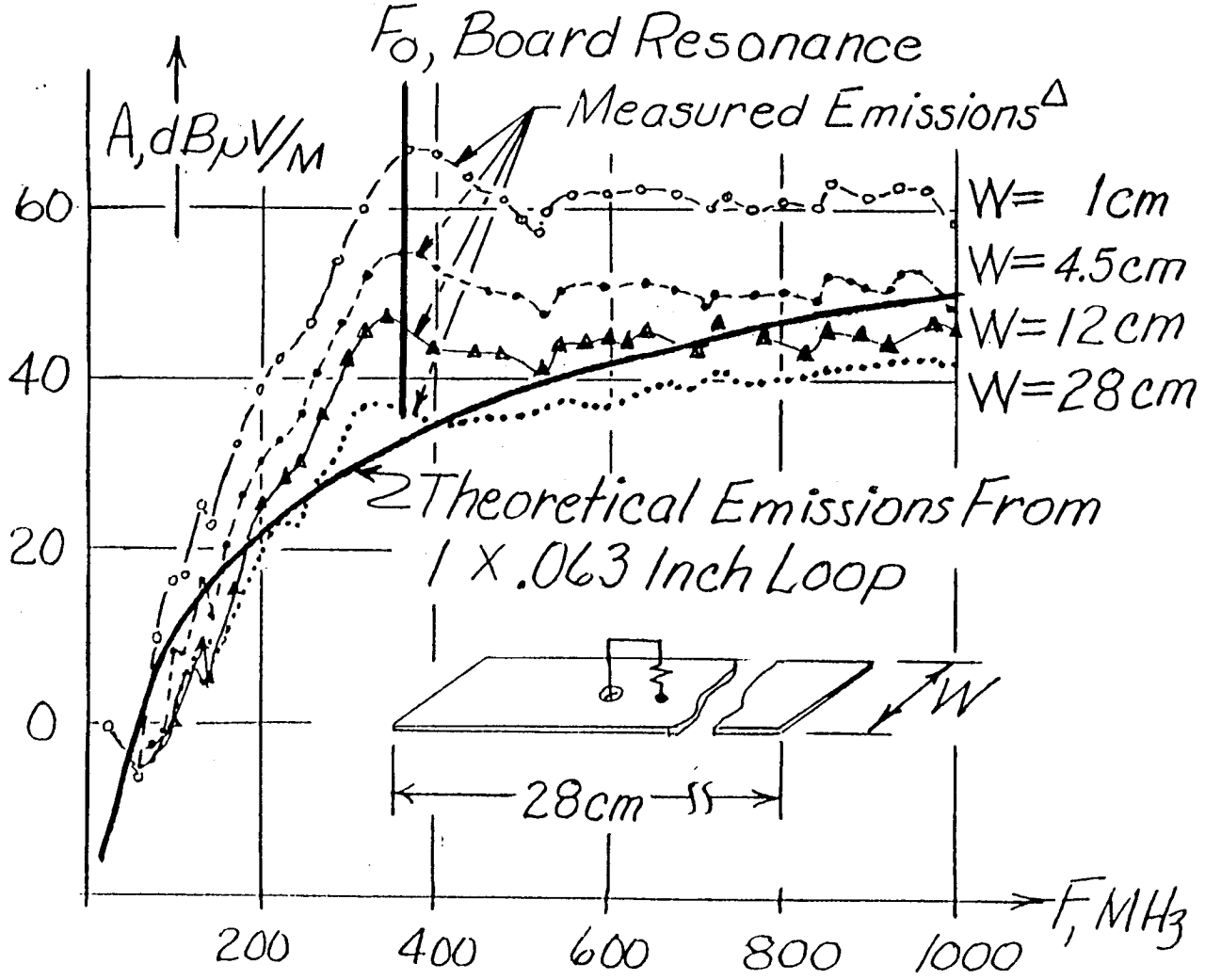
$V_o$ - Driving Voltage, Volts

Z - Loop Impedance, Ω

$F_i$ - Clock Harmonic, $MH_3$

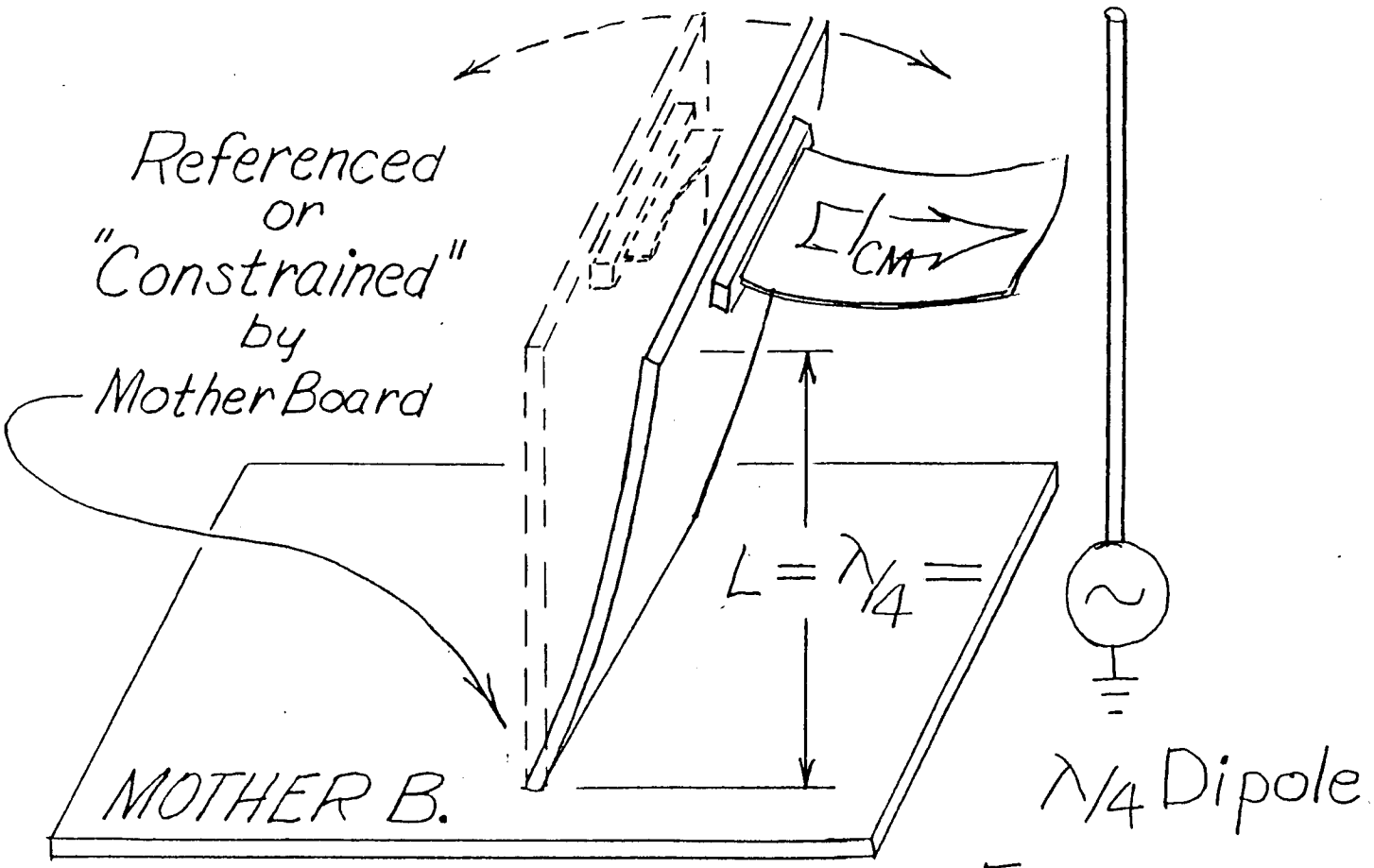
# LOOP Radiation Concept

Δ "Electromagnetic Shielding", Page 9.14; VOL 3, ICT EMC Series, 1988




PWB Length-to-Width Effects on Emissions

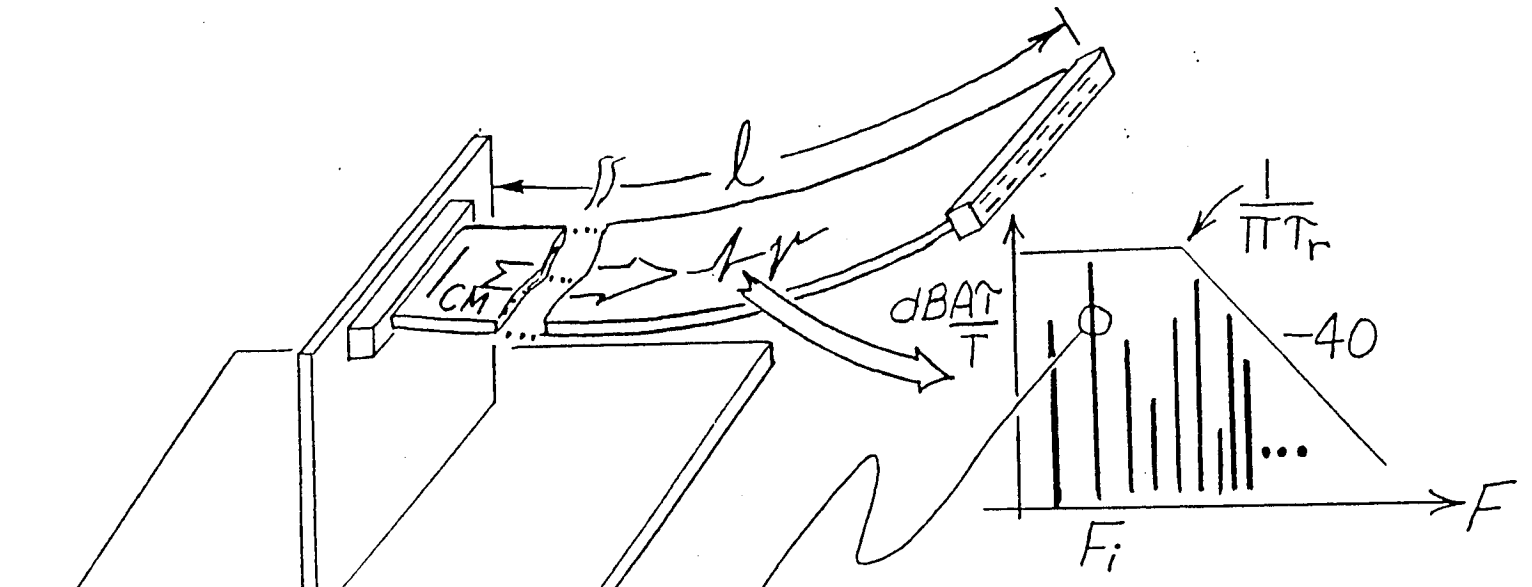
△"Asymetrical Mode Radiation From Multi-Layer Printed Circuit Boards"
R. Dockey, 1991 EMC-ESD Conference Proceedings, Cardiff Publishing




$\lambda/4$ Dipole

$F_r \approx \frac{5630}{L_{cm}}$

# Daughter Board Resonance




$$\Delta\ |E_{CM}|_{MAX} \simeq \frac{6.28 \times 10^{-7} l (I_{CM})(F_i)}{r}$$

$|E_{CM}|_{MAX}$ – Far Field due to $I_{CM}$ at Distance r, $\mu V/m$

$l$ – Length of Cable, m

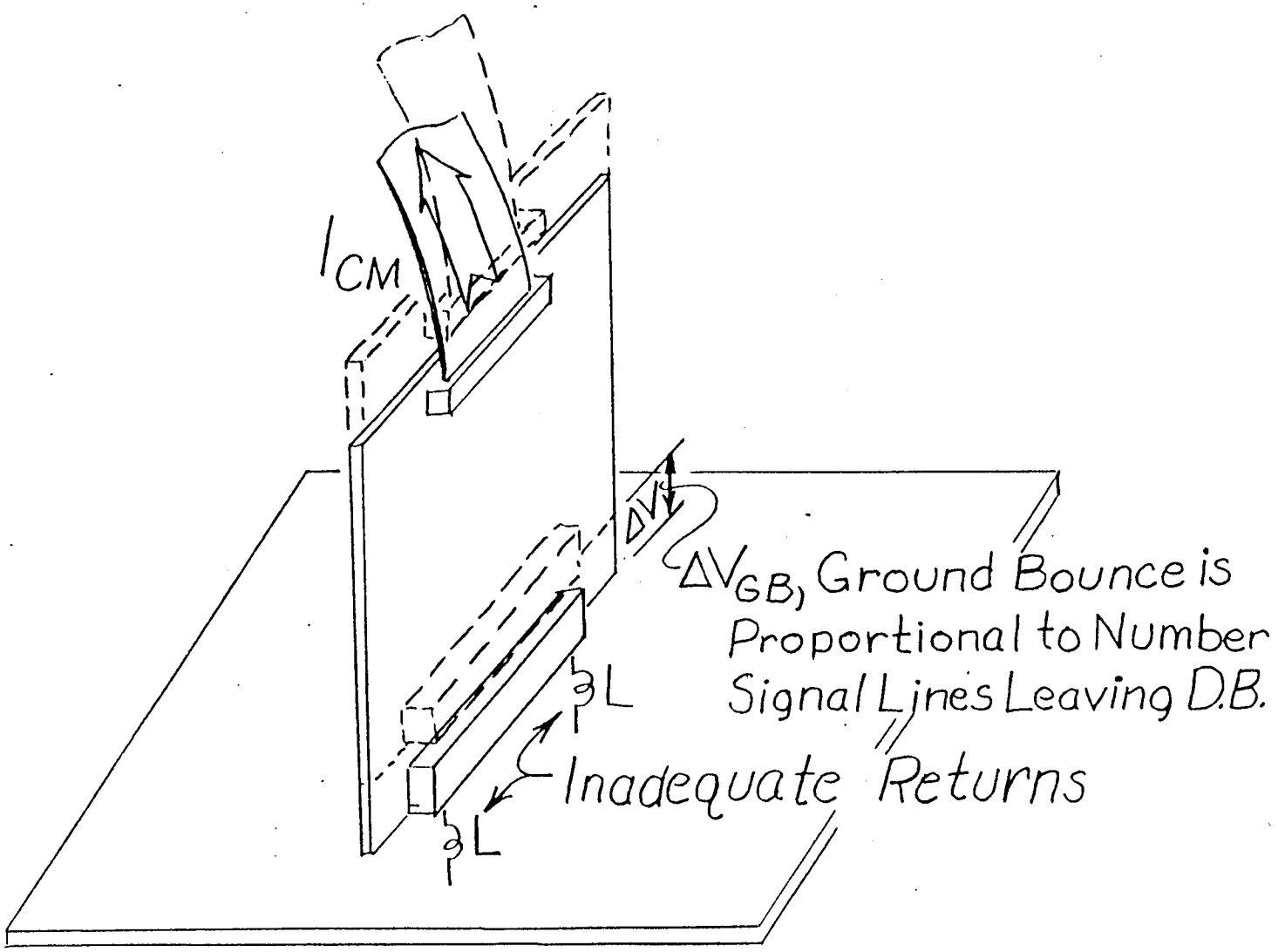
$r$ – Distance to Antenna, m

$I_{CM}$ – Common Mode Current, $\mu A$

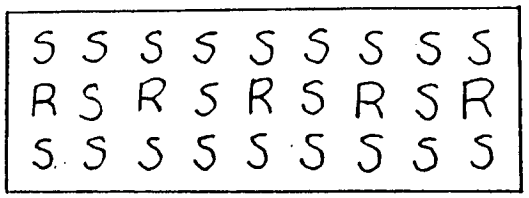
$F_i$ – Clock Harmonic, MHz

Δ Formula adapted from *Introduction To Electromagnetic Compatibility*, CR. Paul, page 447, Wiley 1992

# CABLE Radiation Concept



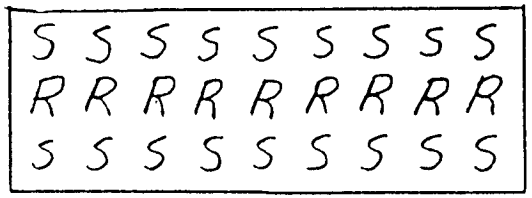

Daughter Board Ground Bounce




One Ret. to 5 Sig.

Slow Signals – More than 15 nS Rise Time

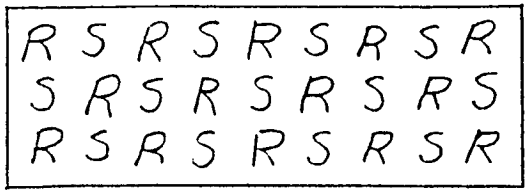
$\Delta V_{GB} \leq 200mV$ @ 15 nS




One Ret. to 2 Sig.

Medium Signals – More Than 5 nS Rise Time, Less Than 15 nS

$\Delta V_{GB} \leq 250mV$ @ 5 nS




One Ret. to 1 Sig.

Fast Signals – Less Than 5 nS Rise Time, More Than 2 nS

$\Delta V_{GB} \leq 300mV$ @ 2 nS

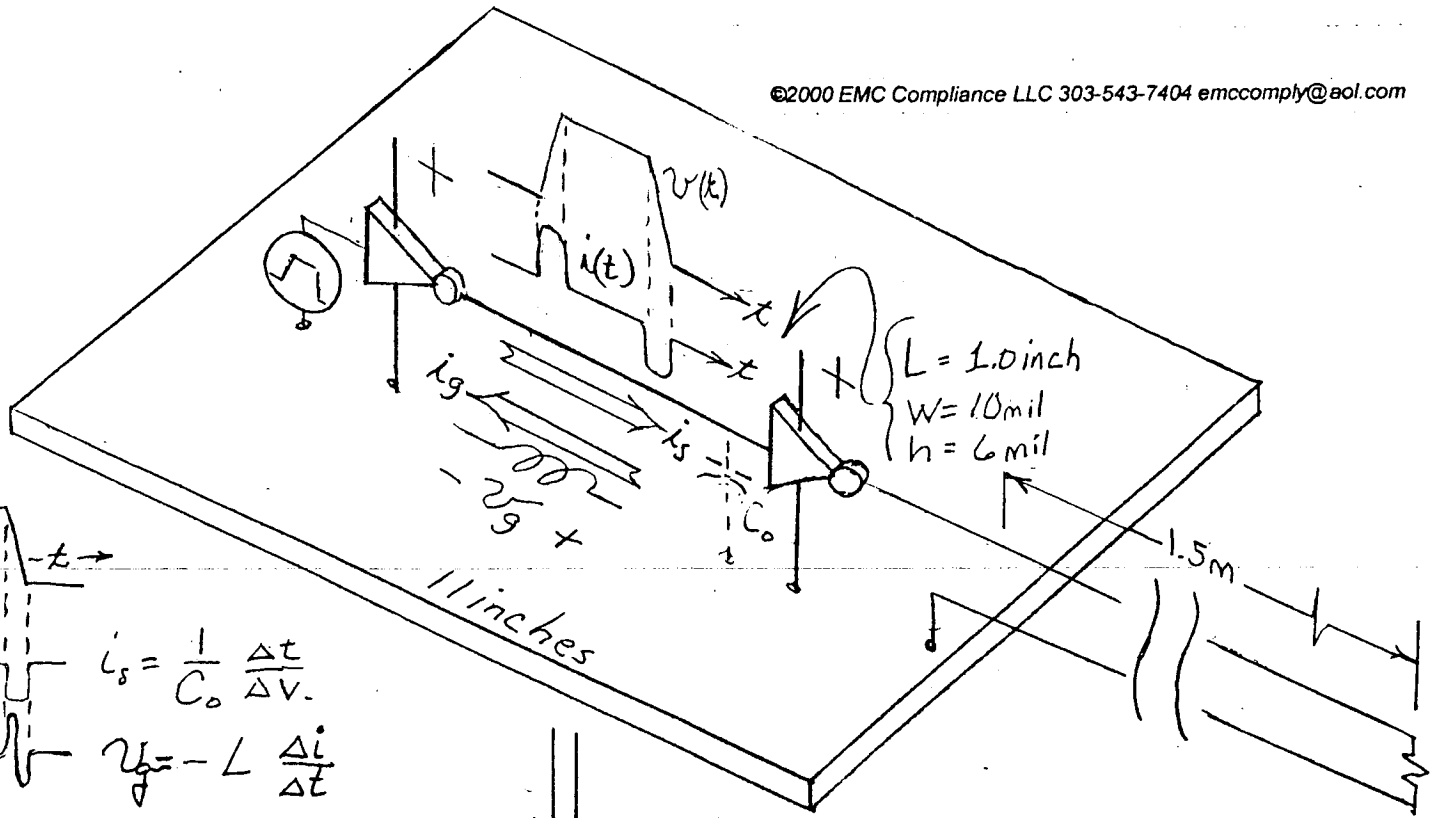
# Selecting Connector Returns (Grounds)

# Common-Mode (CM) Current

- IC Switching Induced CM Current
- Capacitor Decoupling Induced CM Current
- Transmission line Induced CM Current
- Connector Induced CM Current

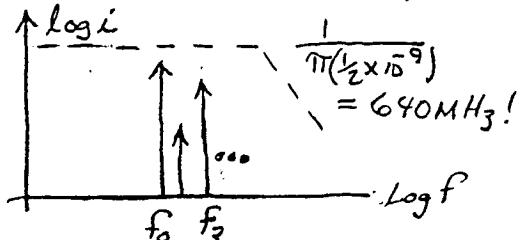
# Simple Illustrative Model of Ground Plane plus Digital Signal Radiation Model











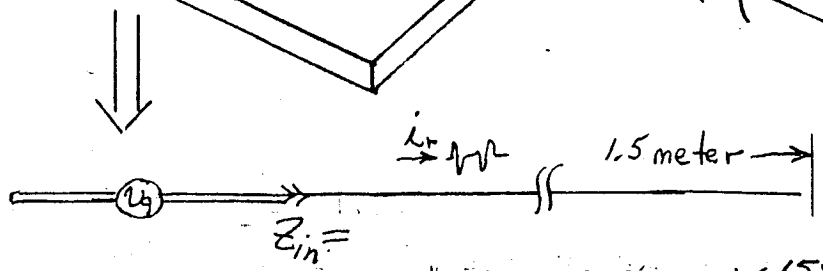

$F_o = 50\,MHz$, $F_3 = 150\,MHz$ etc

Assume: $F_3$ is 6dB down from $i_p$

$i_p = 30\,mA$

$i_{150} = 15\,mA$

$L = 0.08\,nH$ (from Figure 11 of Reference [8])

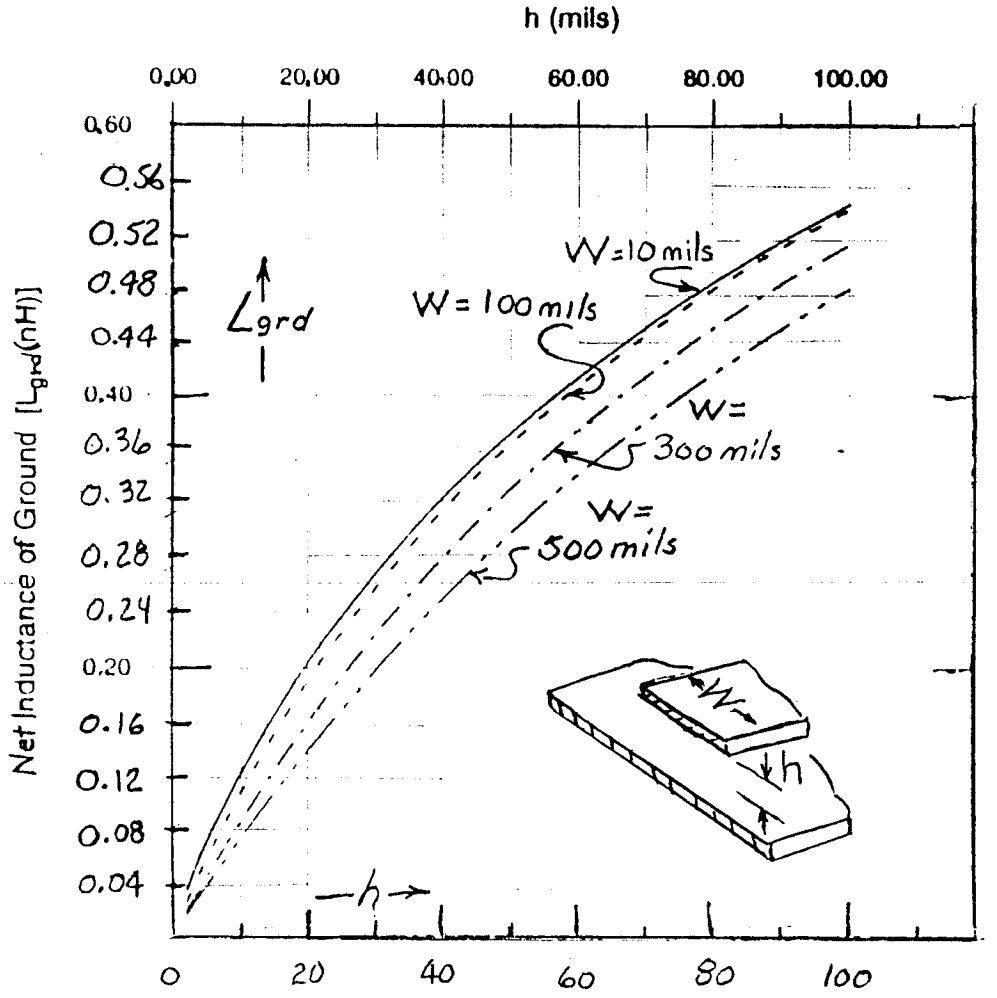



For 150 MHz $i_r = \frac{|v_g|}{Z_{cable}} \cong \frac{(8\times10^{-10}H)(1.5\times10^{-2}/5\times10^{-10})}{300\,\Omega}$ (See figure 11 of [7])

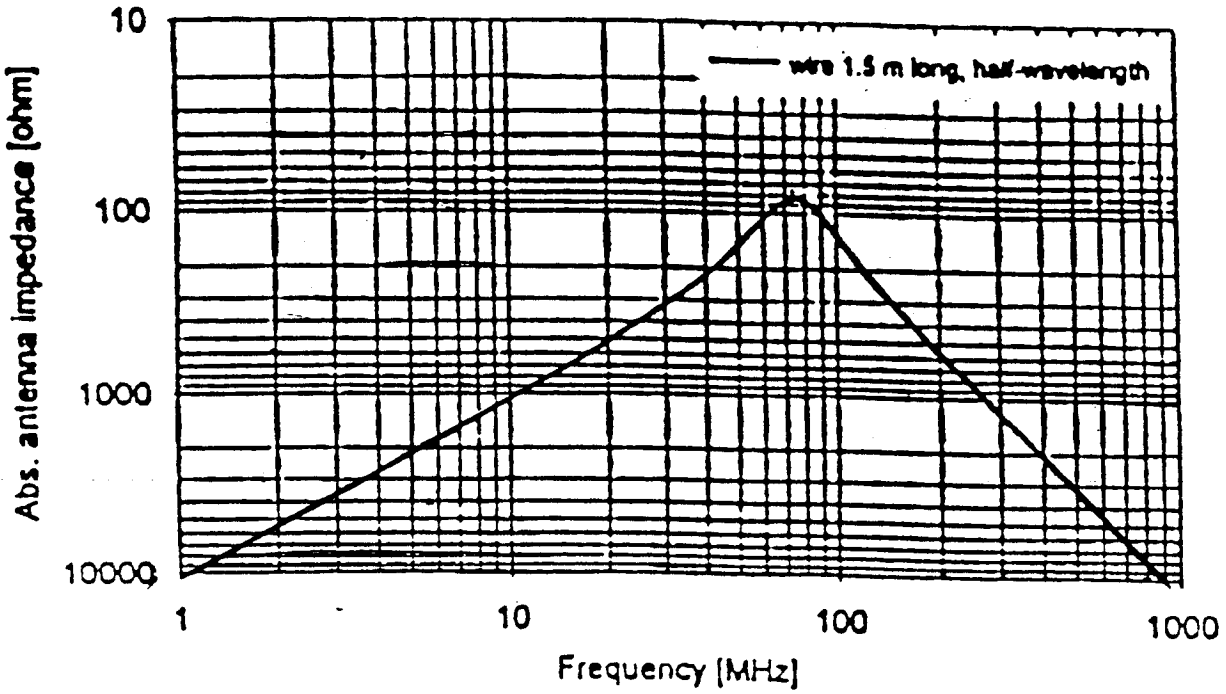
$\cong 2.4\times10^{-2}/300$

$\cong 60\,\mu A$ (36dBμA)

This implies will exceed Class B by ≈ 27dB per Figure A




**Net Ground Plane Inductance as a Function of Signal Trace Width (w) and Height (h) above the Ground Plane for a 1 inch Trace [ref 8]**




**Antenna Input Impedance of a 1.5 meter Long Cable at Half Wave Resonance [ref 7]**

# Figure A—Table of EN55022 Class B Maximum Allowable Common Mode Cable Currents for Information Technology Equipments

The table below shows the maximum *common mode current* that–flowing along the various lengths of cable shown and at the stated frequencies–will cause far field emissions[1] *equal to* EN55022 Class B limits[2]

| cable length, meters | Quarter Wave Resonance Frequency, MHz | Max. Non-Fail Current At 30 MHz, dBuA | Max. Non-Fail Current At 60 MHz, dBuA | Max. Non-Fail Current At 120 MHz, dBuA | Max. Non-Fail Current At 240 MHz[2], dBuA | Max. Non-Fail Current At 480 MHz[2], dBuA |
|---|---|---|---|---|---|---|
| 0.1 | 750 | 44 | 38 | 32 | 33 | 27 |
| 0.2 | 375 | 38 | 32 | 26 | 27 | 21 |
| 0.5 | 150 | 30 | 24 | 18 | 19 | 13 |
| 1.0 | 75 | 24 | 18 | 12 | 13 | 7 |
| 2.0 | 38 | 18 | 12 | 6 | 7 | 1 |

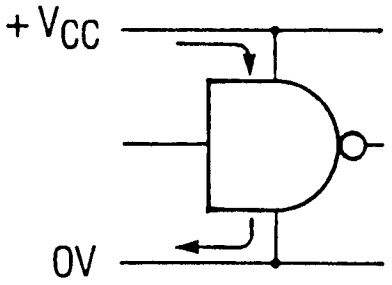
1) $E=(2\pi\ 10^{-7} \times F \times L \times I) / D$ (see C. Paul, Introduction to Electromagnetic Compatibility , page 417, equation 8.21), where:
E–absolute value of field strength in volts/meter maximized with respect to antenna polarity and cable aspect
F–frequency in Hz
L–length of cable in meters
I –common mode current flowing along cable in Amperes
D–distance from cable to antenna in meters

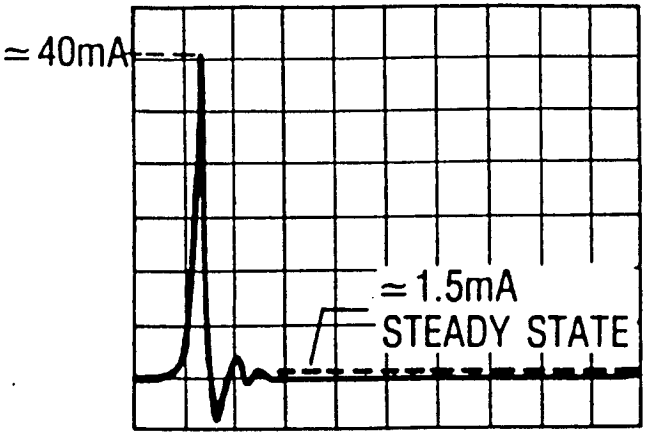
2) EN55022 emission limits at 10 meters are 30 dBuV/m from 30 MHz to 230 MHz and increase by 7 dB for frequencies above 230 MHz

# Decoupling Capacitors

- Chip Cross-Over Current
- Rise Time
- Capacitor Lead Inductance,
- Parasitic Inductance
- Series Resonance
- Dynamic Impedance, $\Delta e/\Delta i$

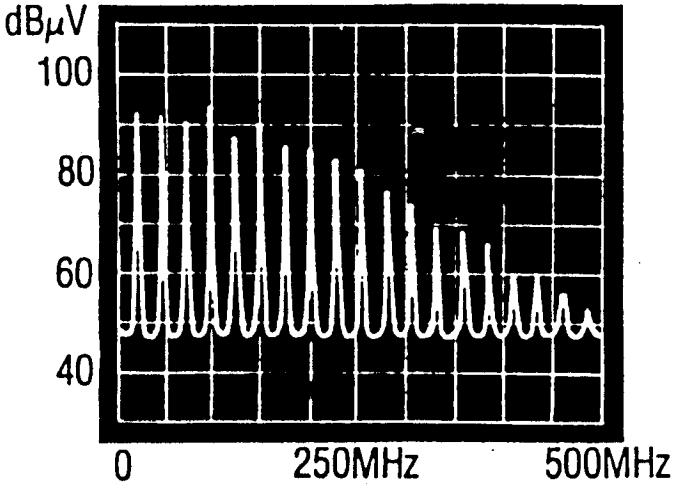
# POWER SUPPLY TRANSITION CURRENT
# 74LS GATE



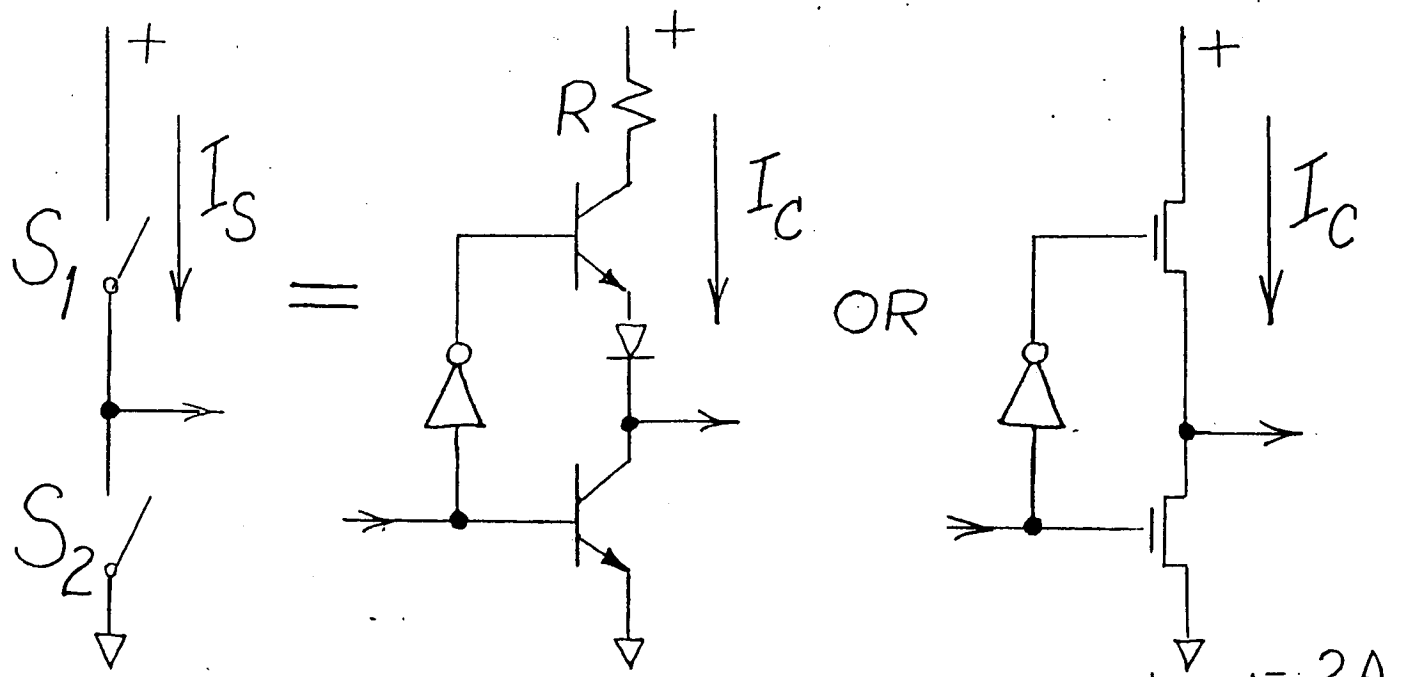




SCALE: HORIZONTAL—5ns/div; VERTICAL—7mA/div

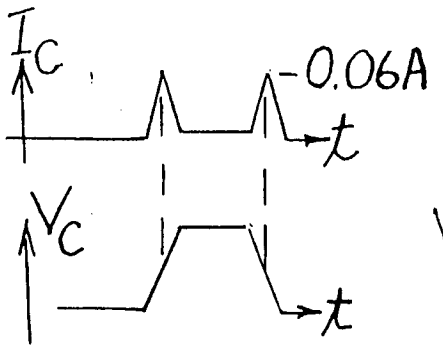
SPECTRUM MEASURED WITH
TEKTRONIX PROBE
(TRANSFER IMPEDANCE 5Ω)

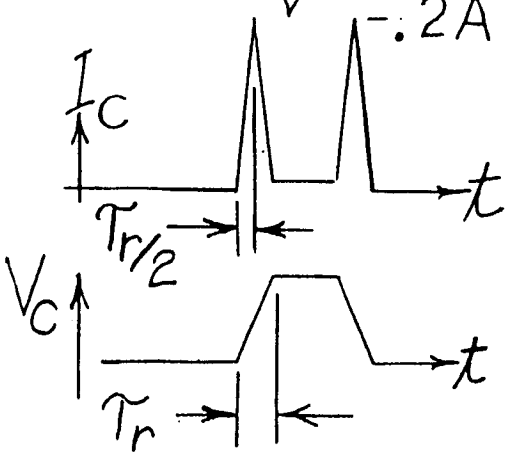


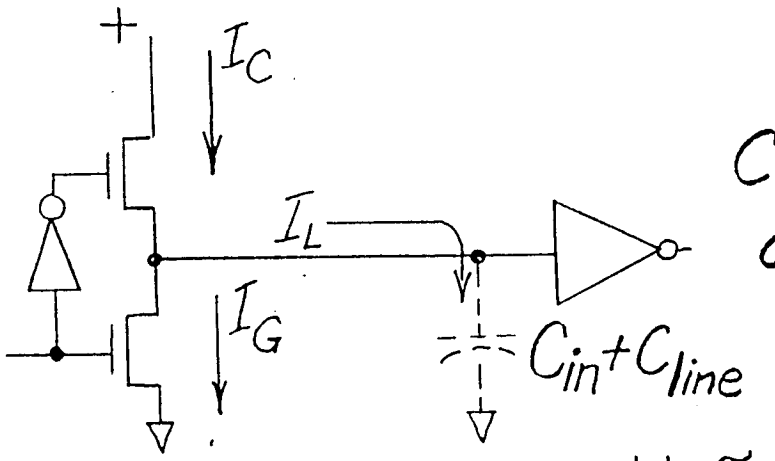
# Cross-Over Current




$S_1$ is still On When $S_2$ Closes – (and Visa Versa)

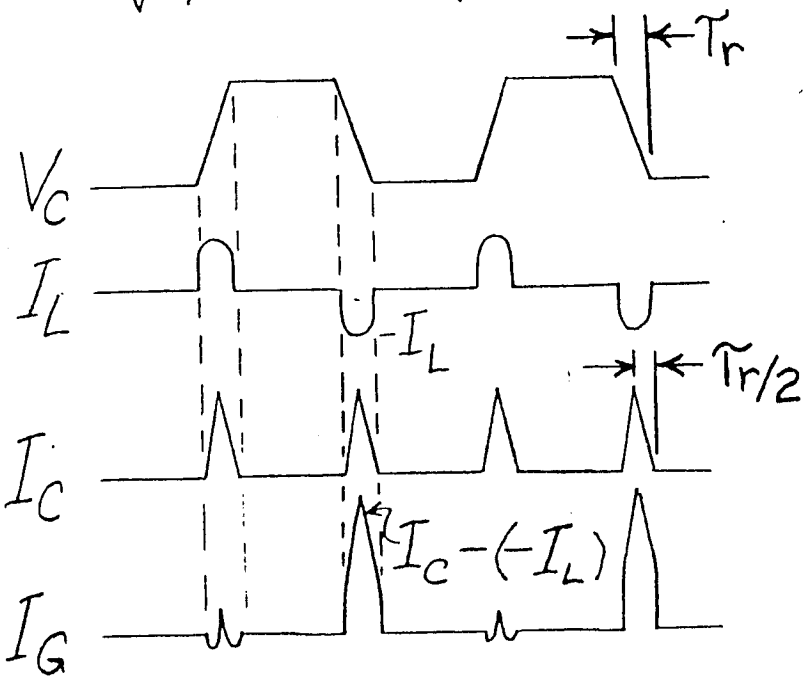




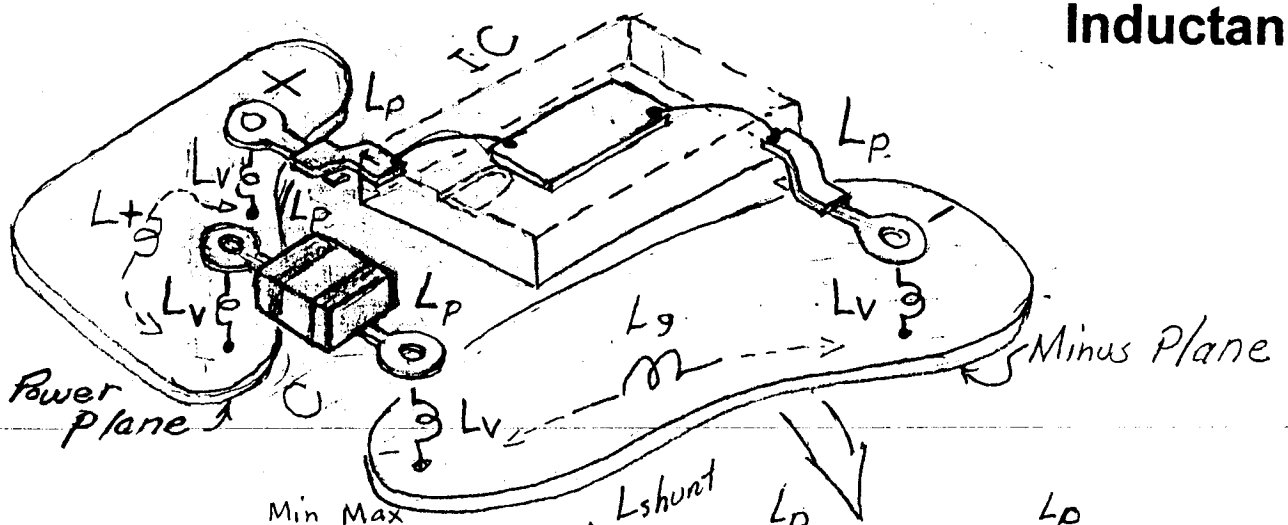

# Ground Current ($I_G$) Combined Cross-Over and Load Currents

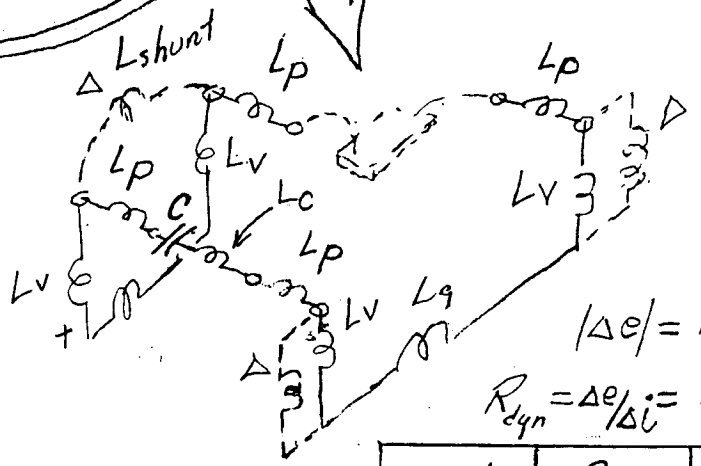
$$I_G = I_C - I_L$$




| Family | $I_p$, ma | $\tau_{r/2}$, nS |
|---|---|---|
| TTL | 30-50 | 5 |
| LS | 30-50 | 2.5-5 |
| FAST | 30-50 | 0.5-1 |
| HC | 40-80 | 1.5-2.5 |
| AC | >150 | .25-.5 |

# Visualization Sketch of Typical Decoupling Capacitor Circuit Showing Parasitic Inductance Effects




| | Min | Max |
|---|---|---|
| $L_c$ - 1-2 nH | 1 | 2 |
| $L_v$ - 1-1.5 nH | 4 | 6 |
| $L_p$ - $\Sigma \approx$ 1nH | 1 | 1 |
| $L_g$ - $\approx$ .1nH | .1 | .1 |
| $L_+$ - $\approx$ .1nH | .1 | .1 |
| | 6.2 | 9.2 |

Minimized "L" (see Δ's)

$L_c$ = 0.1 nH (AVX "IDC")

$L_v$ = 1. nH (bridged and shunted)

$L_p \simeq .8$ nH

$L_g \simeq .1$ nH

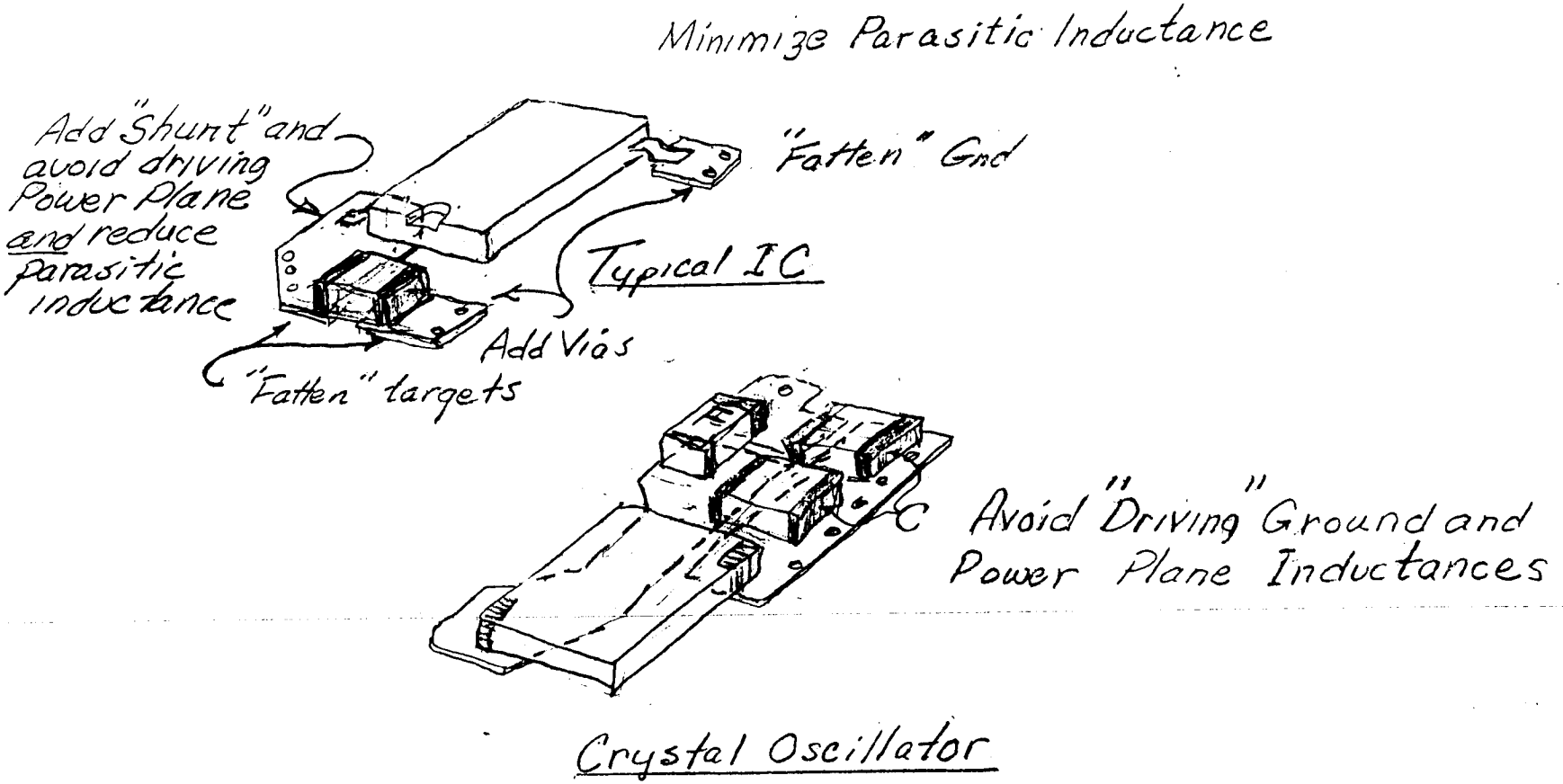
$L_+ \simeq .1$ nH

$L_{Total} \simeq 2.1$ nH

$|\Delta e| = L \frac{\Delta i}{\Delta t}$

$R_{dyn} = \Delta e / \Delta i = L / \Delta t$

| $L_T$, nH | $R_{dyn}$ | $F_0$ resonance |
|---|---|---|
| 9.2 | 18 Ω | 3 MHz |
| 6.2 | 12 Ω | 6 MHz |
| 2.1 | 4 Ω | 11 MHz |




# Alternate Methods of Minimizing Decoupling Parasitic Inductance and Reducing "Board Bounce"

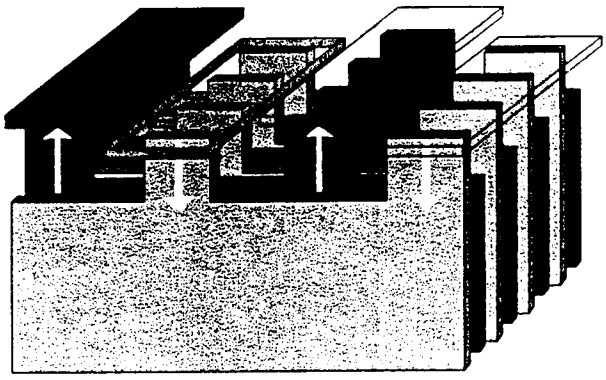


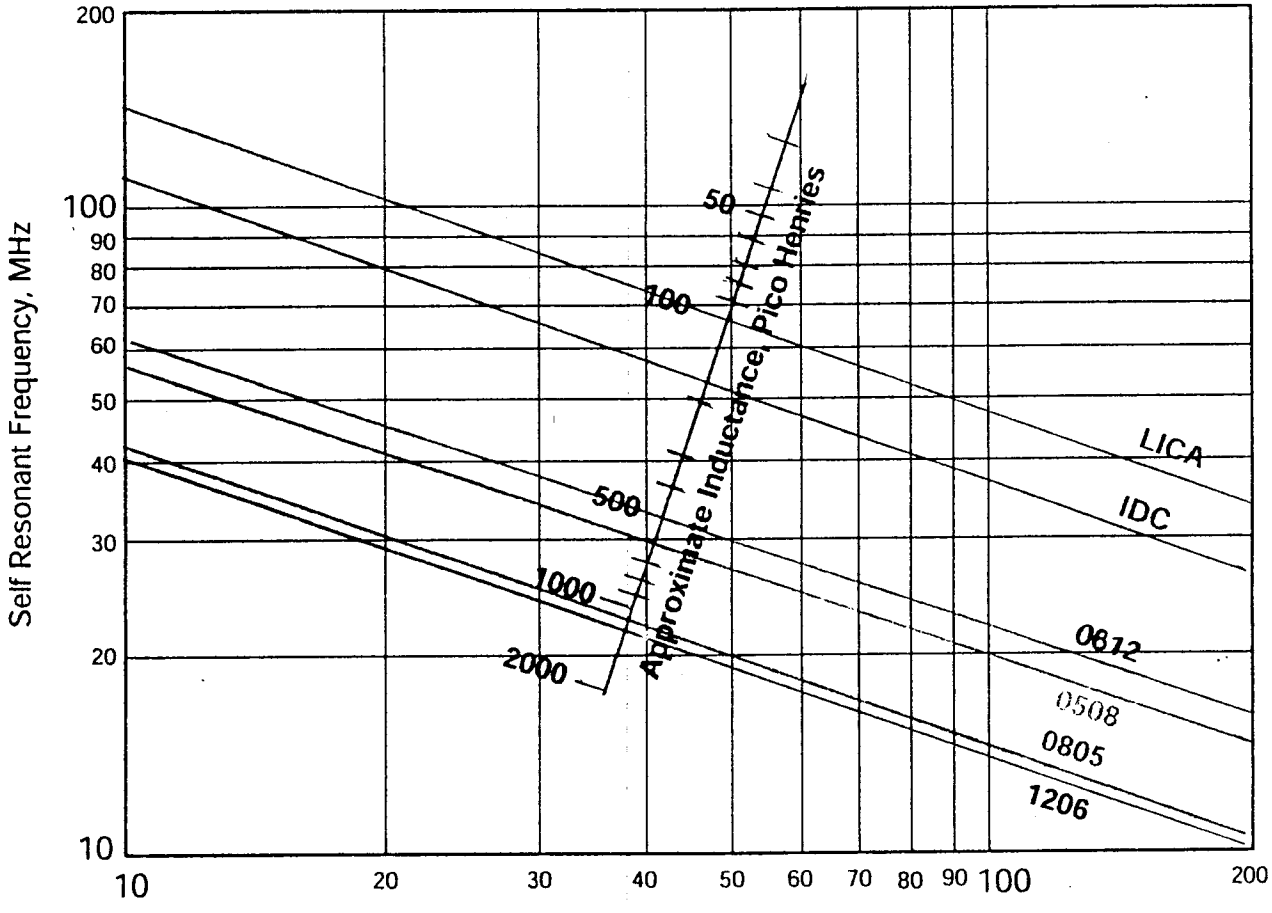
*Figure 4. LICA's Electrode/Termination Construction. The current path is minimized – this reduces self-inductance. Current flowing out of the positive plate, returns in the opposite direction along the adjacent negative plate – this reduces the mutual inductance.*

Also the effective current path length is minimized because the current does not have to travel the entire length of both electrodes to complete the circuit. This reduces the self inductance of the electrodes. The self inductance is also minimized by the fact that the charging current is supplied by both sets of terminals reducing the path length even further!

The inductance of this arrangement is less than 100 pH, causing the self-resonance to be above 50 MHz for the same popular 100 nF capacitance. Parts available in the LICA design are shown on pages 6 and 7.

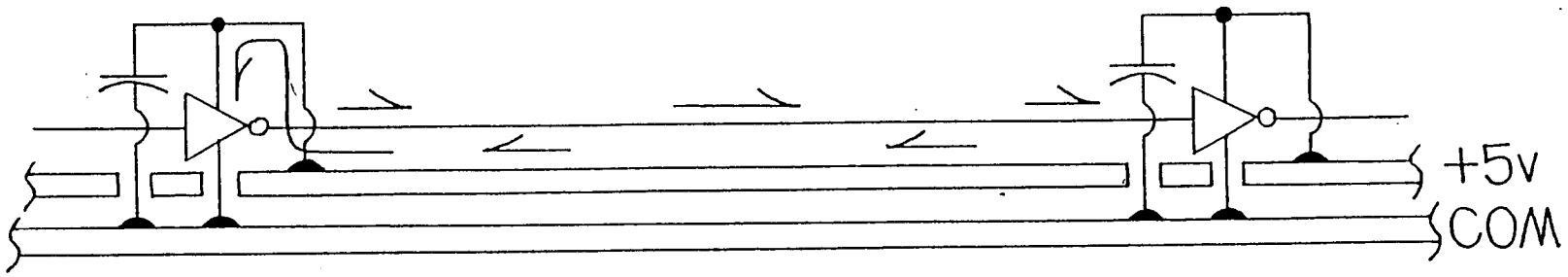
Figure 5 compares the self resonant frequencies of various capacitor designs versus capacitance values. The approximate inductance of each style is also shown.

*Active development continues on low inductance capacitors. C4 termination with low temperature solder is now available for plastic packages. Consult AVX for details.*

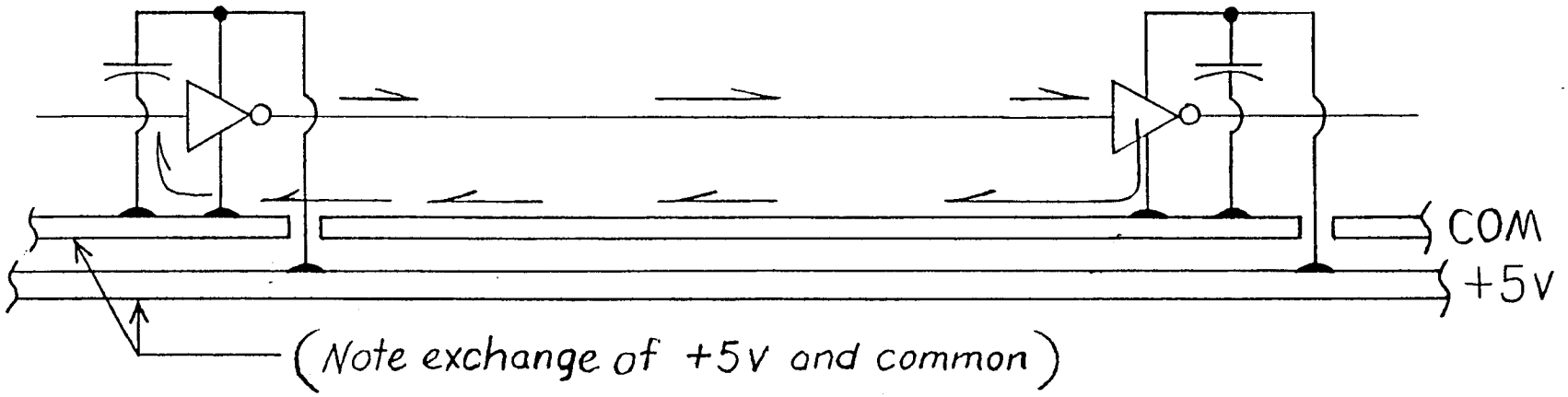



Self Resonant Frequencies vs. Capacitance and Capacitor Design

*Figure 5*

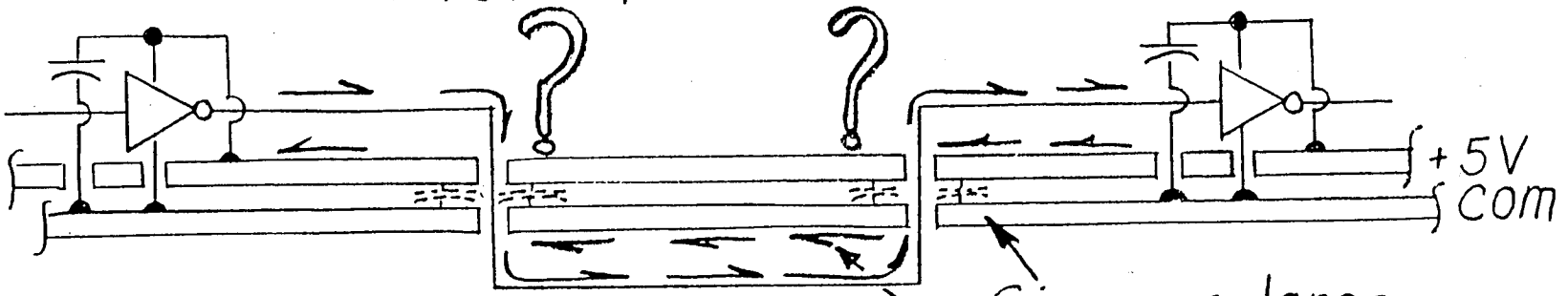



# Case 1 - Signal Referenced to Power Plane (+5v)




# Case 2 - Signal Referenced to Common Plane

# Case 3 - Signal References BOTH 5 Volts & Common

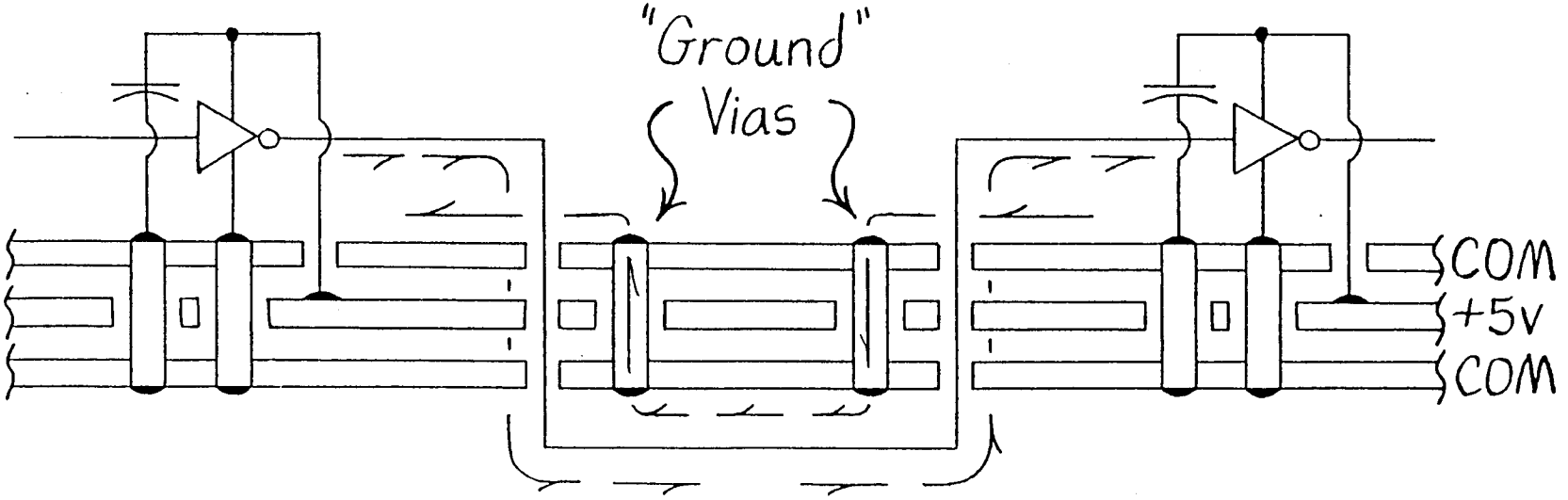



How does Return Current follow the source?

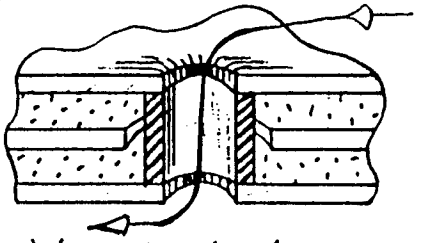
C is never large enough - causes Signal Delay and NOISE

This question becomes important ONLY if signal rise time falls below 5 ns

# Fix For Case 3 - Add Extra Common



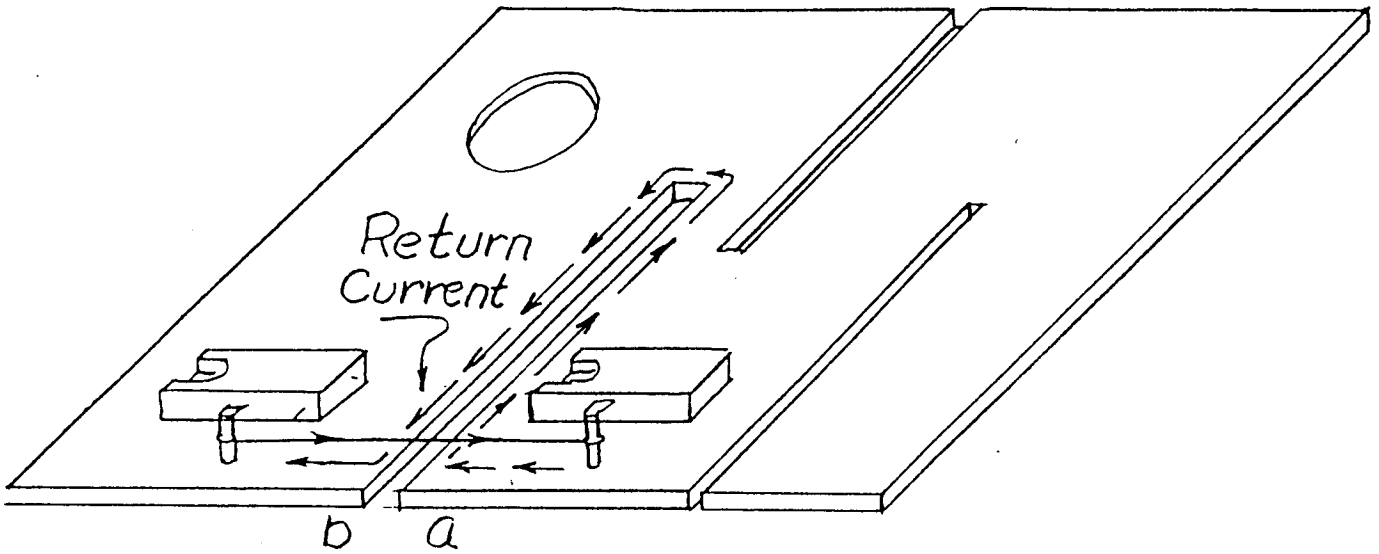

Return Current
Follows Signal Current



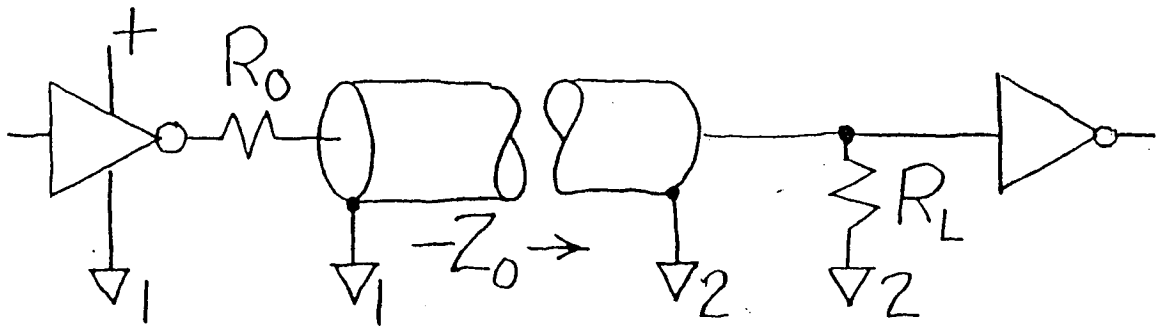
Via Cut-Away

"Detours" in Ground Plane Cause:

- Inductive Hits on $Z_o$
- High Frequency Emissions

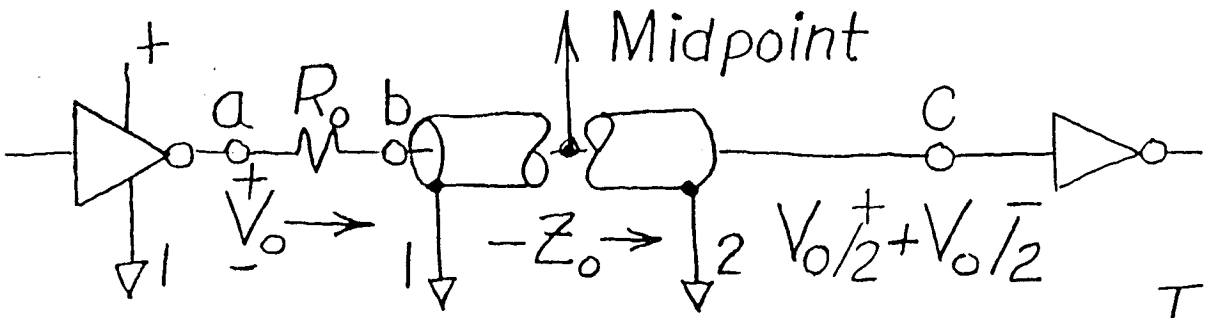



Beware of Chopped Ground Plane




- For Bipolar Logic, Goal is to "Match" $R_L$ to $Z_0$ so that Reflection = 0
- For CMOS Logic, Goal is to Match $R_0$ to $Z_0$ and Set $R_L = \infty$ so that Reflection = +1

Concept of Transmission Line Matching

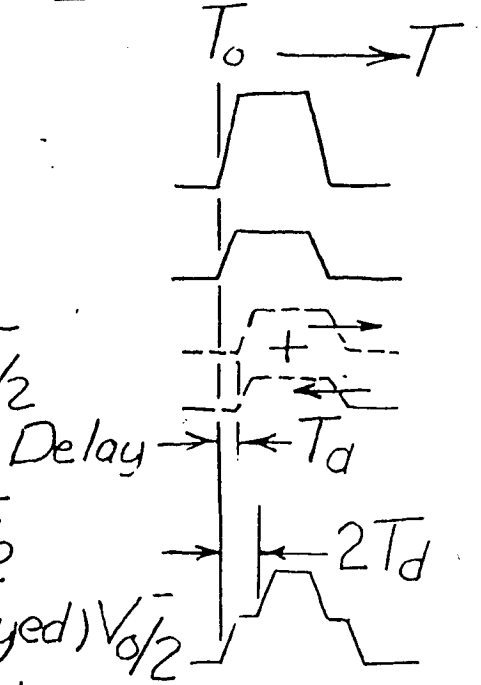



Left-to-Right (Forward Wave)

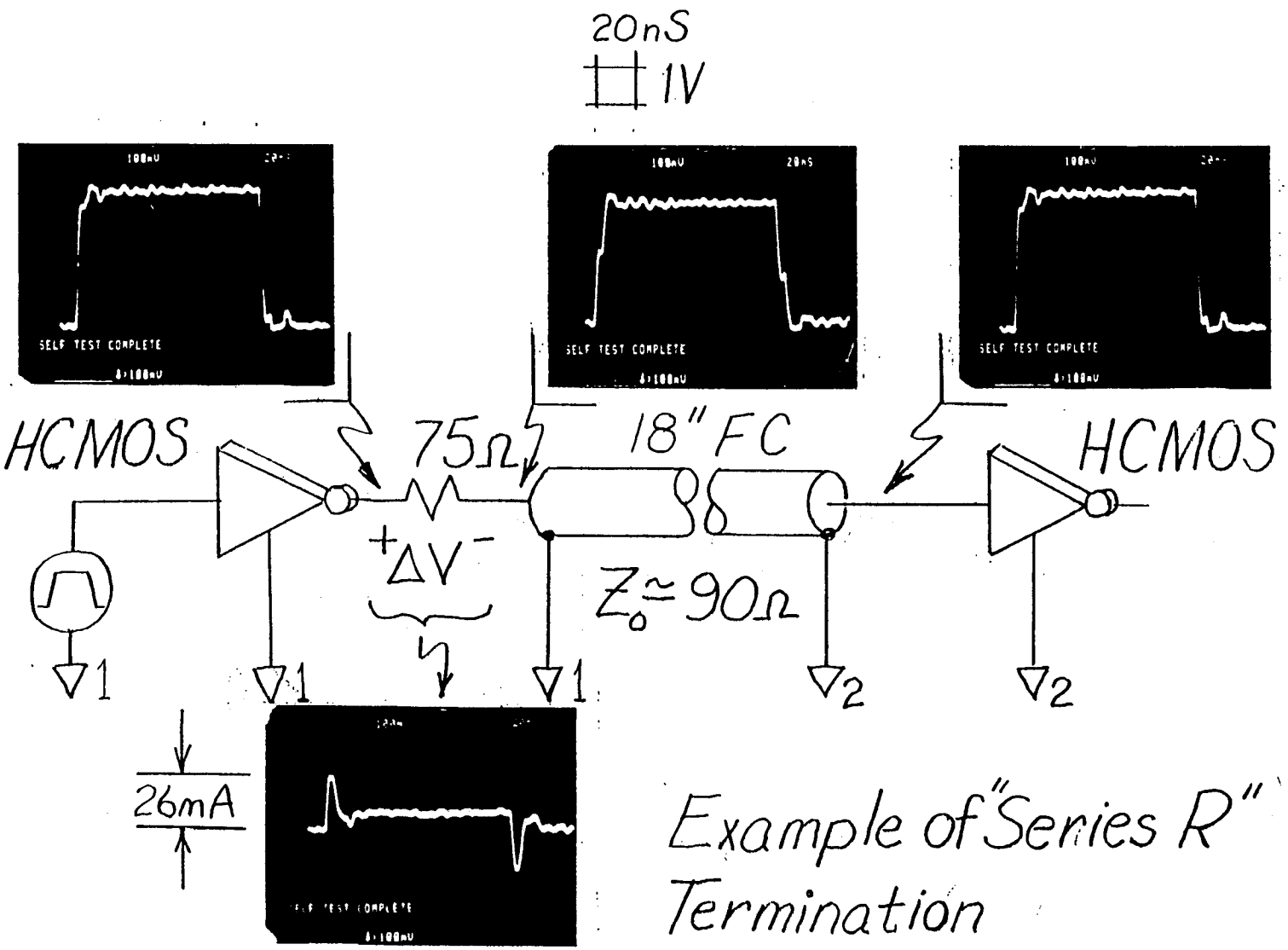
- Voltage at Point "a" = $V_o$
- Voltage at point "b" = $V_o/2$
- Voltage at point "c" = $V_o/2^+ + V_o/2^-$

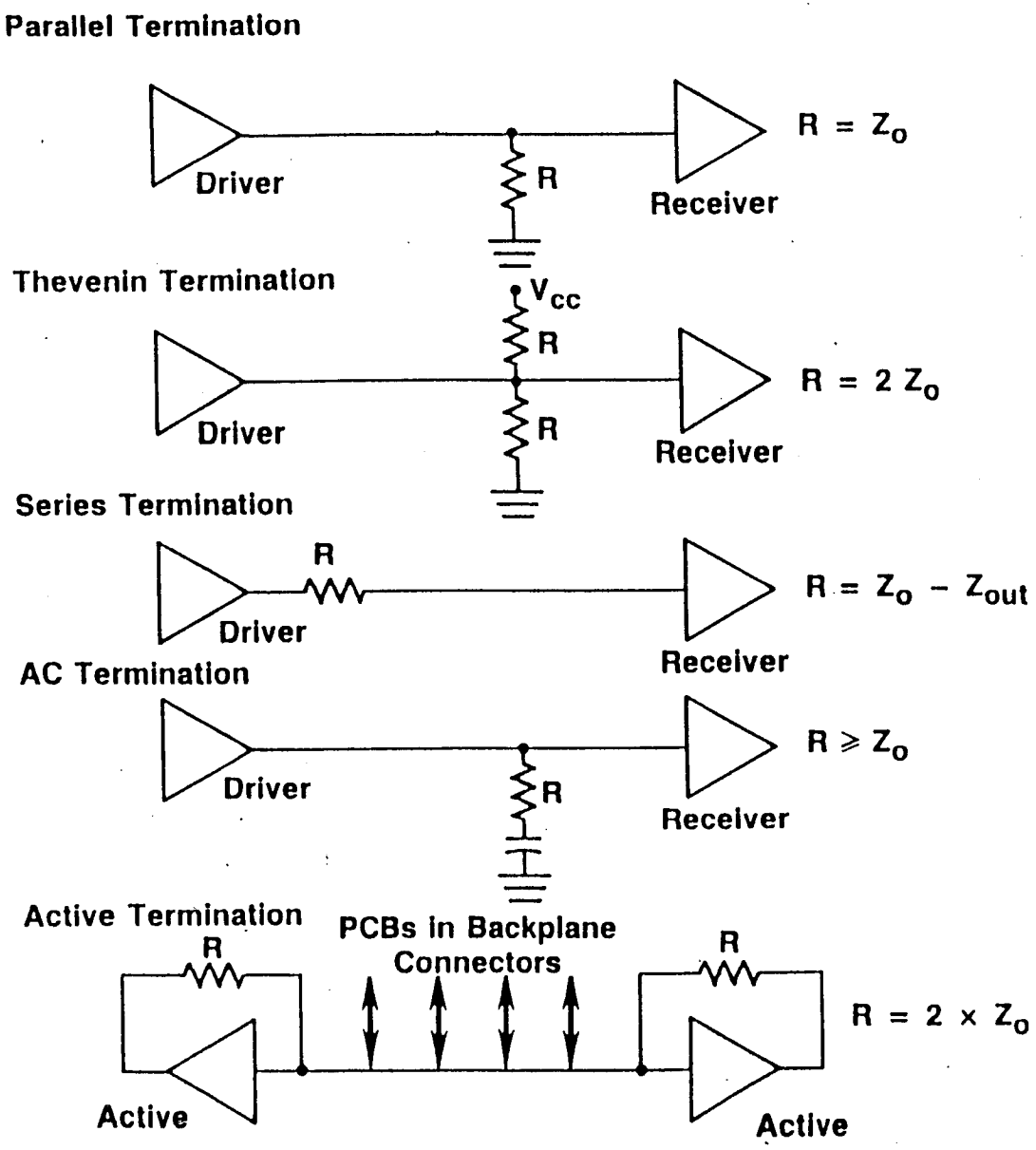
Right-to-Left (Reflected Wave)

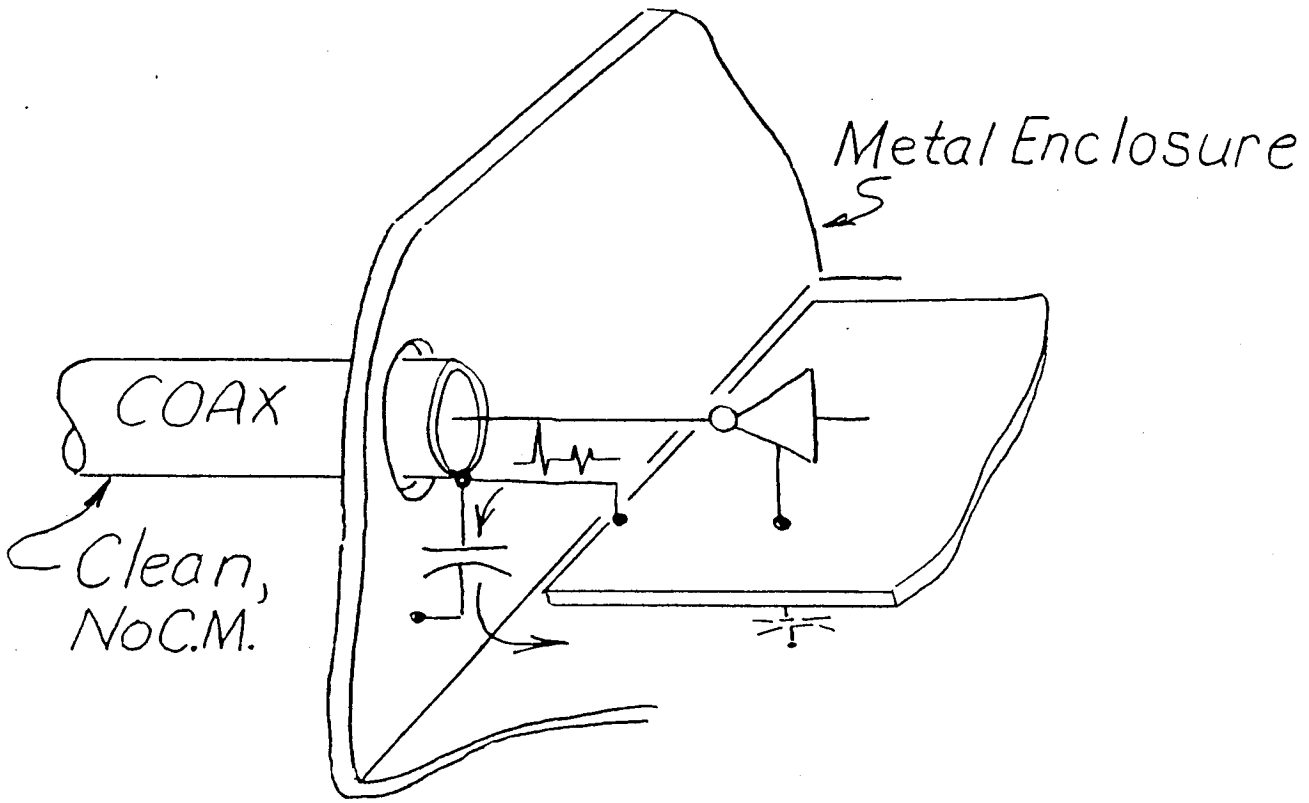
- Voltage at point "c" = $V_o/2^+ + V_o/2^-$
- Voltage at point "b" = $V_o/2^+$ + (delayed) $V_o/2^-$
- Voltage at point "a" = 0 (matched Load)



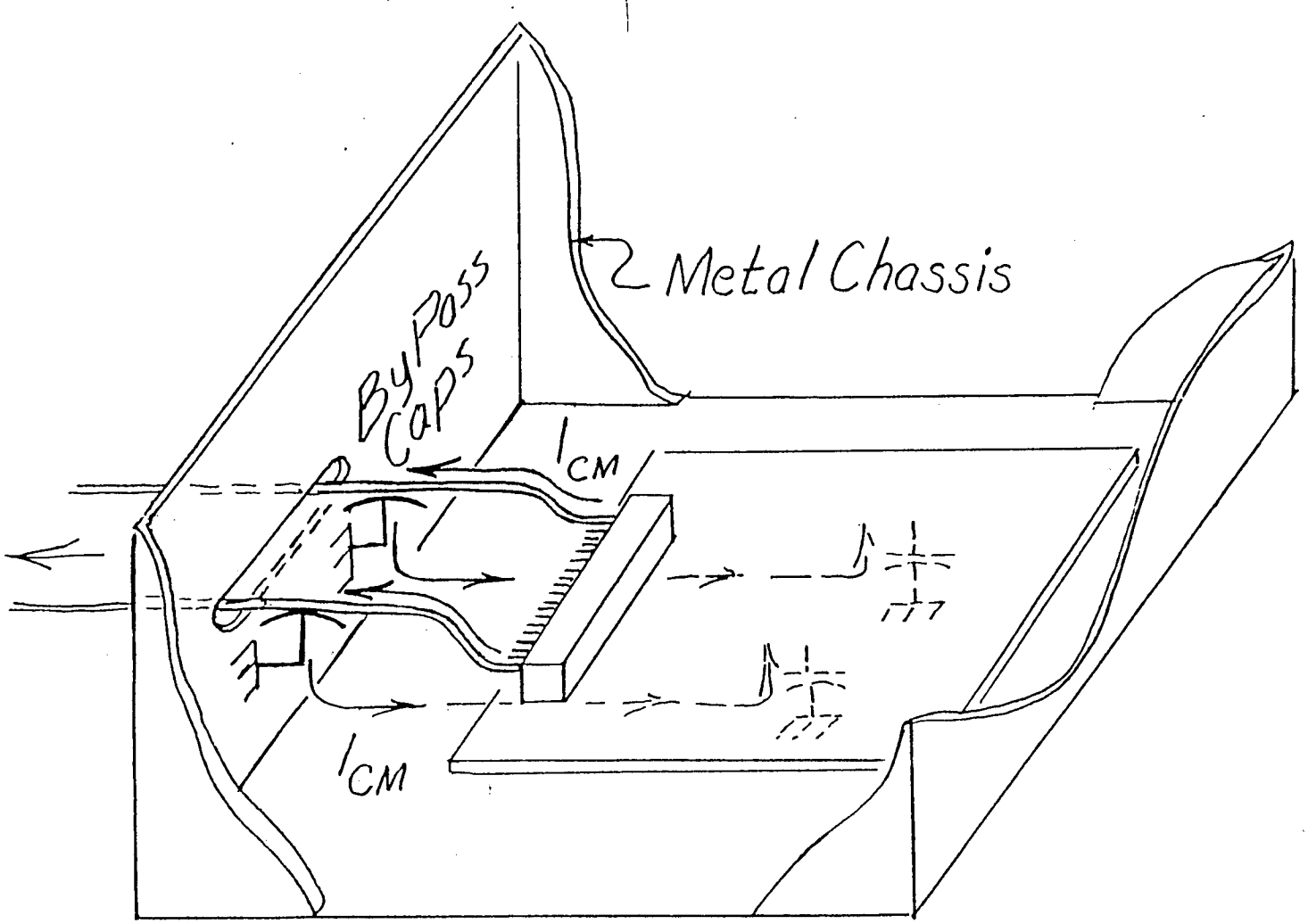

# CMOS Transmission Line Details



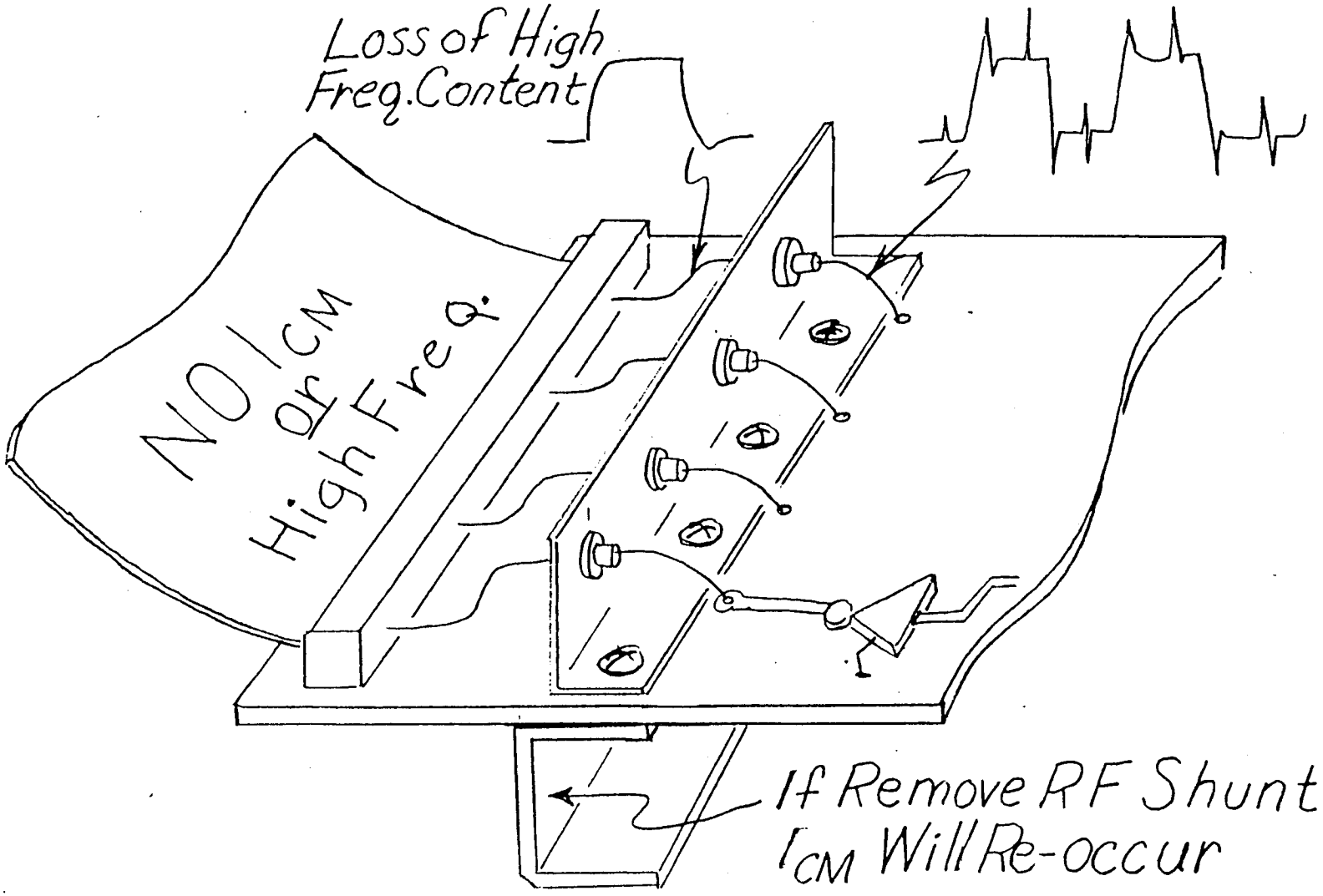




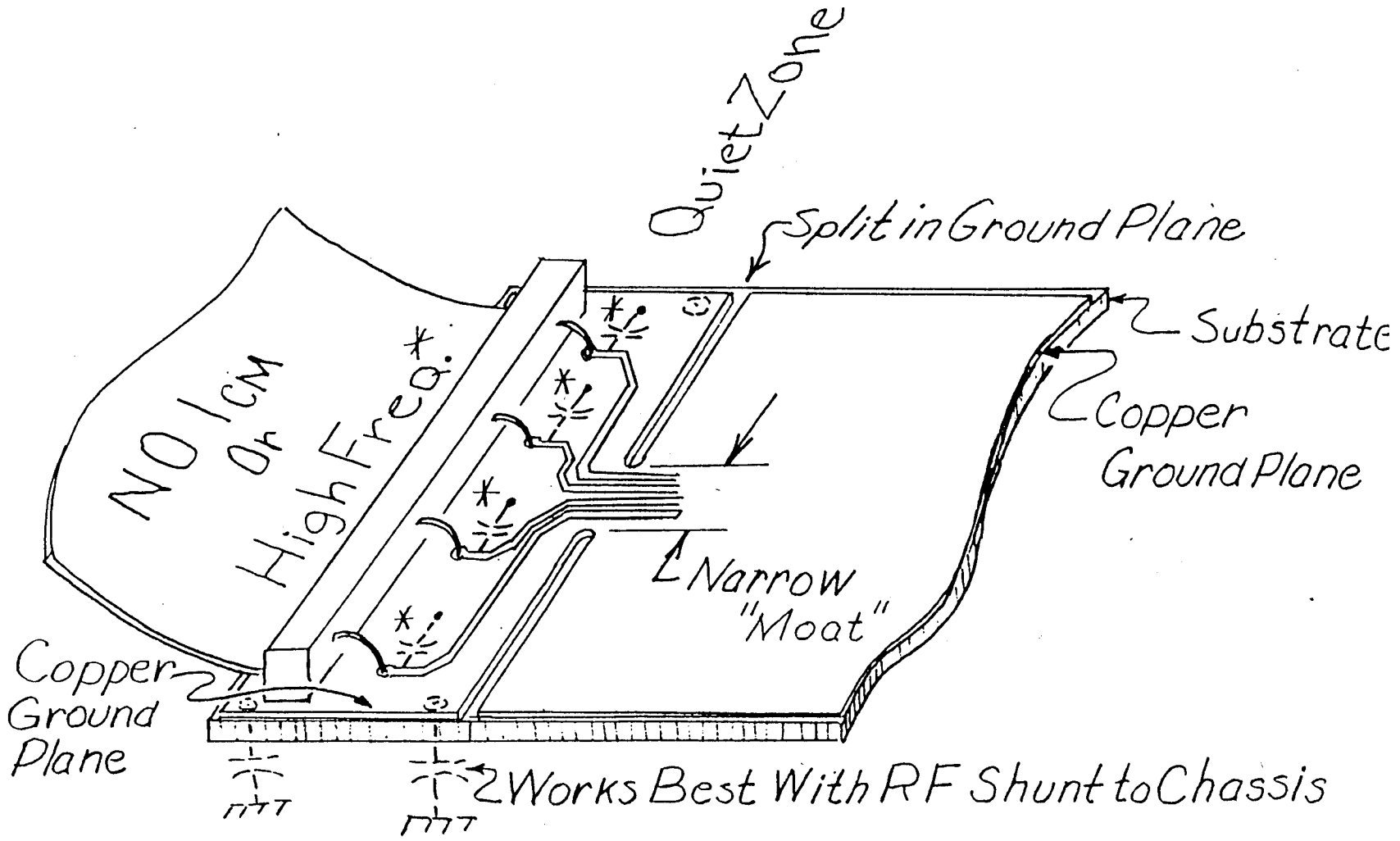

# How to Decouple Common Mode Current to Chassis and Preserve HF



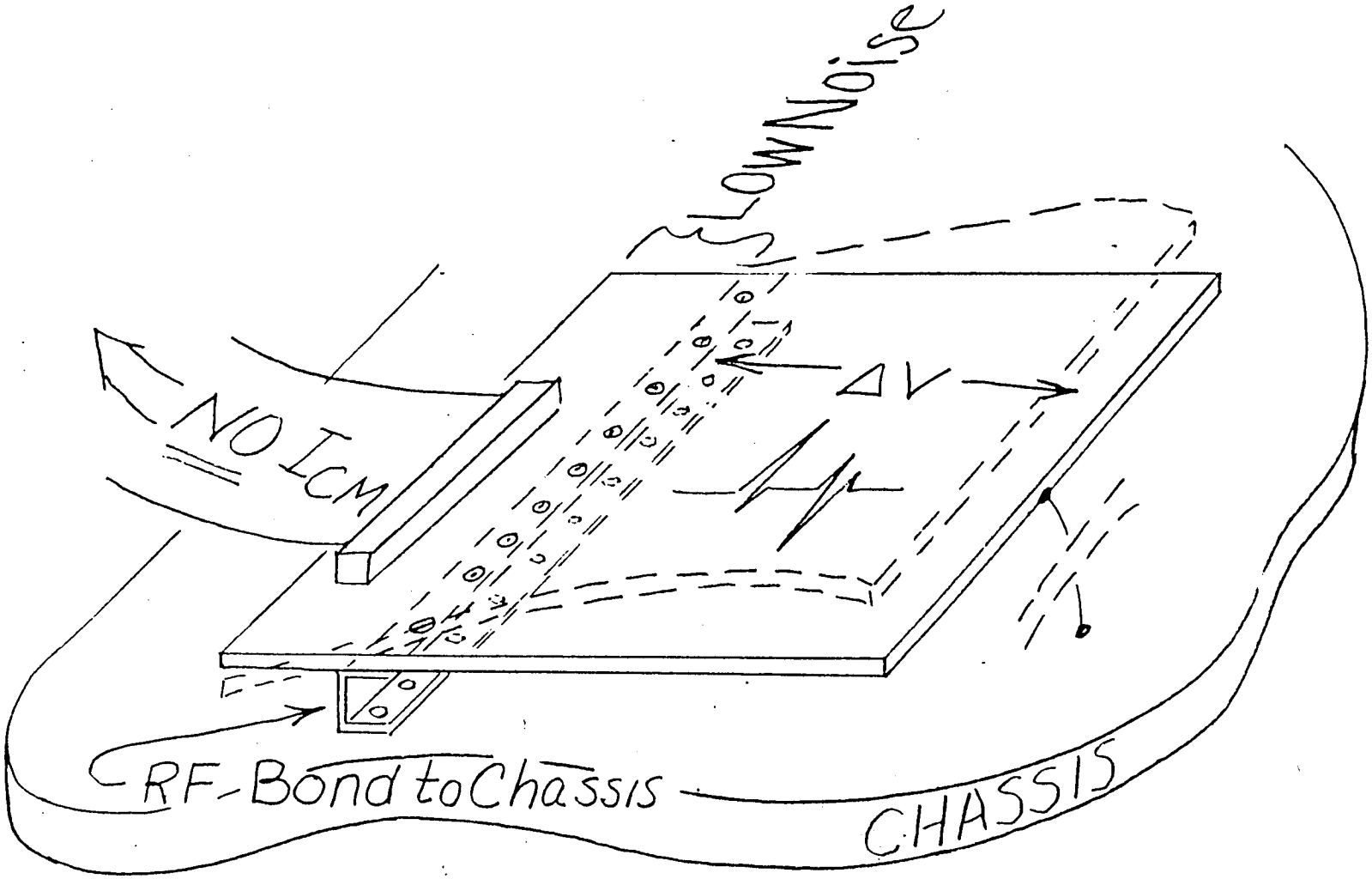

# Decoupling Common Mode Currents at the Chassis




Quiet Zone plus a Fence




Alternate Quiet Zone-The Moat




Establishing a PWB Low Noise Zone