Power Distribution System Decoupling— "how 'bout them vias?"

Presented by

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Ansoft Calculations and Curves Preparation by

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prepared for

Rocky Mountain Chapter of the EMC Society of the IEEE
January 23, 2003

- INTRODUCTION (Where we are and where we seem to be going)
-
- **WHERE THE NOISE STARTS** (and SI and EMI become intertwined)
-
- **PWB DECOUPLING** (One of the several necessary ways to control noise)
- **VIAS** (today, yesterday and tomorrow)

Moore's Law and Design

In 1972 Gordon Moore, co-founder of Intel Corporation predicted that the performance of computers would double every 18 months[1]. Over the last 21 years, the rate of development of computers based on that prediction has held firm.

At the time of Mr. Moore's prediction, the first Intel 4004™ microprocessor slogged along at a 108 KHz rate and contained 2300 transistors. On May 6, 2002 IBM™ announced its latest Intel Pentium IV® driven Computer. Its clock rate is 2400 MHz, and it is reported to contain over 10 million transistors. It is apparent that the progression of computer development up to the present day has closely followed Mr. Moore's prediction. In fact, by the late fall of 2002 Dell ™ and others began offering Pentium IV's® operating at 2670 MHz.

The rate of electronic design complexity is accelerating too. New designs must incorporate new features in order to allow them to operate at ever increasing speeds. Signal Integrity and Electromagnetic Compatibility are key elements in the feature development process.

[1] Page 4, "*High Speed Digital System Design—A handbook of Interconnect theory and Design*", Hall, Hall and McCall, Copyright 2000 by Wiley and Sons, ISBN 0-471-36090-2

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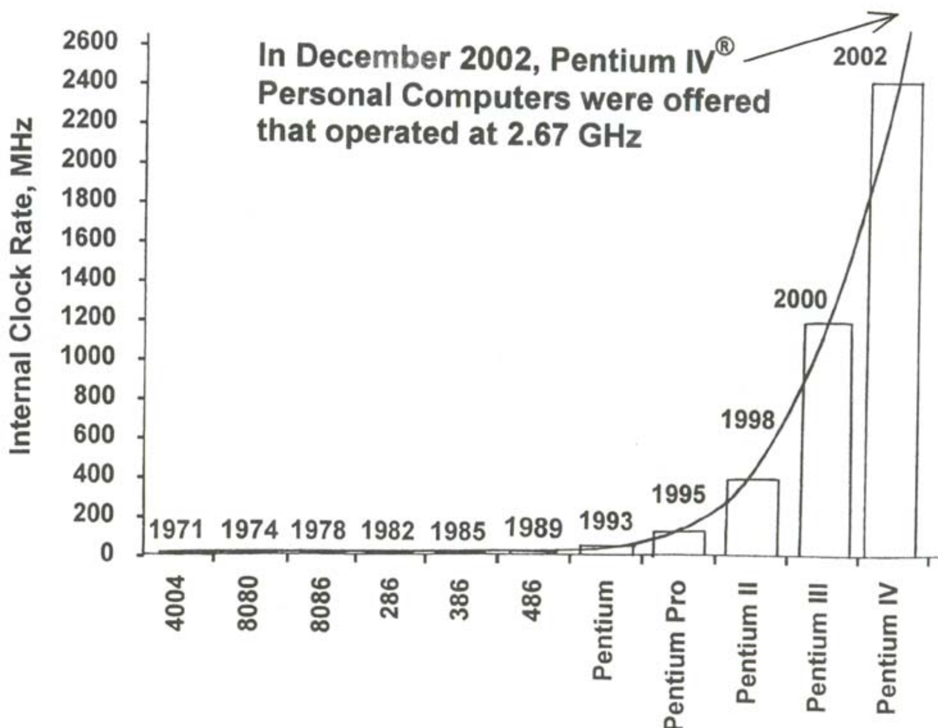
Moore's Law in Action



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Semiconductor Device Speed–Where Are We Today?[1]

One Example of Leading Edge Integrated Circuit Technology is composed of Heterojunction Bipolar transistors

- Device Technology: Silicon-Germanium (SiGe) Heterojunction Bipolar transistors (HBT)
- Process: 0.13 um with copper interconnects and 50 Ohm internal T-Lines
- Vendor: IBM Microelectronics
- HBT Transistor/Circuit Capabilities:

HBT Transistor F_t	285 GHz
Equivalent Gate Delay	4.23 ps
Demonstrated Toggle Rate:	110 GHz

NOTE: this technology will be available commercially before the end of 2002

[1] April 1, 2002, *Electronic Design Magazine* (US Edition), page 27

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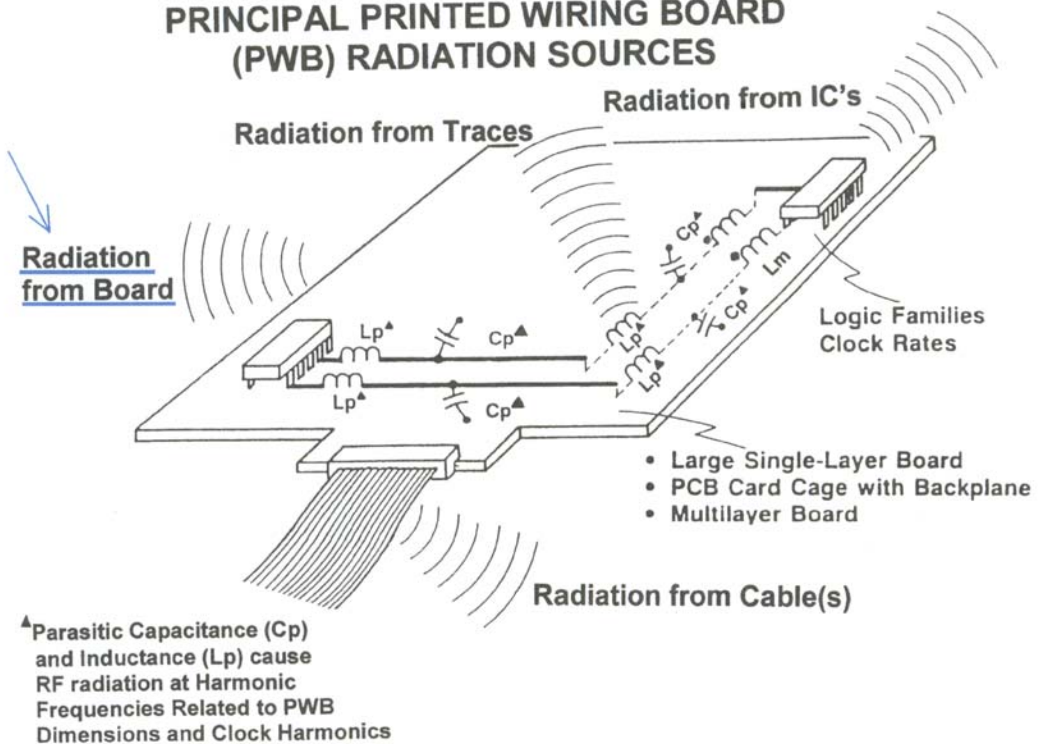
PRINCIPAL PRINTED WIRING BOARD (PWB) RADIATION SOURCES



▲Parasitic Capacitance (Cp) and Inductance (Lp) cause RF radiation at Harmonic Frequencies Related to PWB Dimensions and Clock Harmonics

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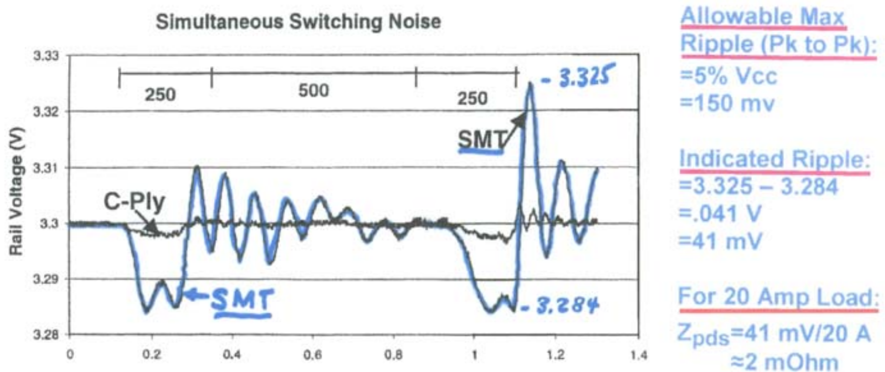
PWB Power Supply Noise Ripple Comparison for Surface Mount (SM) and Embedded Capacitor Decouplers▲



Curves based on numerical analysis of idealized board using Partial Element Equivalent Circuit (PEEC) formulation—

PWB Length:	4 inches (1 cm)
PWB Width:	4 inches (1 cm)
Via Length:	1 mm (to Vcc), 0.5 mm (to Common)
SMT Capacitor:	0.96 nF (1206)
C-Ply Capacitor:	0.96 nF (embedded)
Driving Signal:	1 nS duration 250 pS rise and fall time
Logic Family:	3.3 Volt supply with five deep 0.5 um CMOS Cells followed by simple inverter

▲Diaz-Alvarez et al: MODELING AND SIMULATION OF INTEGRATED CAPACITORS, pages 611-619, *IEEE Transactions on Components and Packaging Technologies*, December 2000

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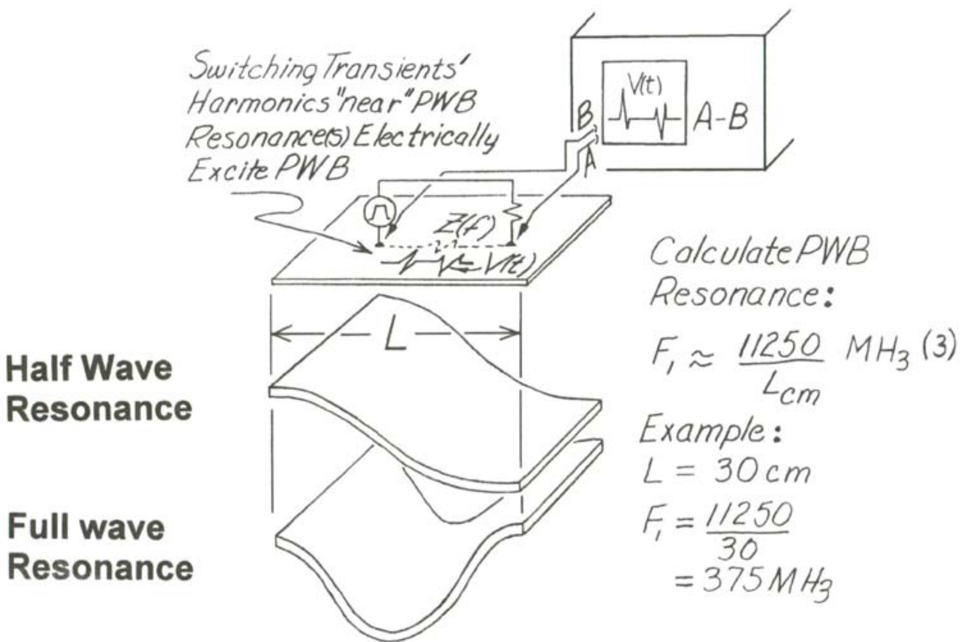
PWB RESONANCE ILLUSTRATION



[3] Dockey, "Asymmetrical Mode Radiation from Multi-layer Printed Circuit Boards", pages 247 – 251, *Conference Proceedings of EMC/ESD International Symposium*, Denver Colorado, April 22-24, 1992, published by Cardiff Publishing Company

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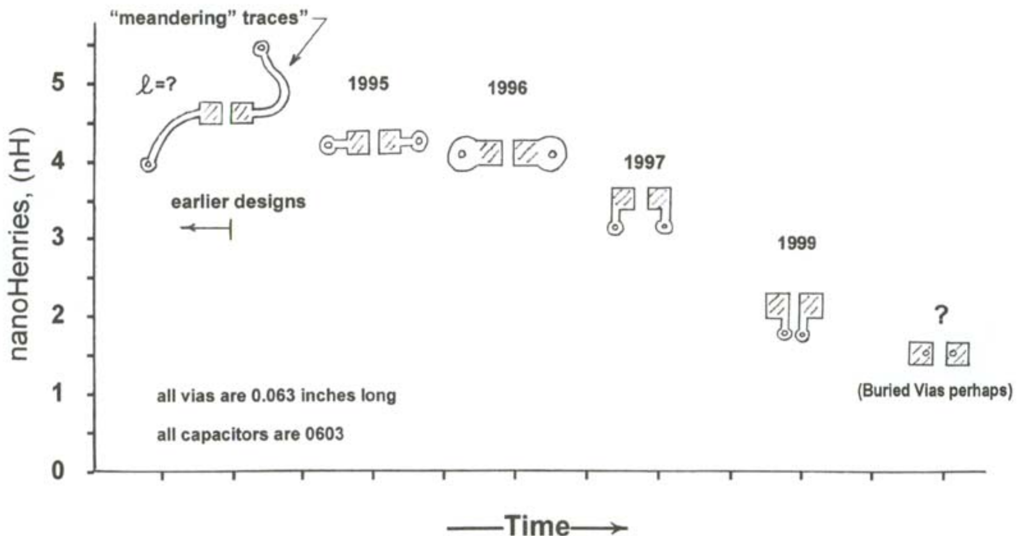
Surface Mount (SM) Decoupling Capacitor PCB Mounting Techniques—Shortened Trace Length and Via Location—used to Reduce Equivalent Series Inductance (ESL)[1]



[1] Adopted from "*ESR and ESL of Ceramic Capacitor Applied to Decoupling Applications*"; Tanmoy Roy, Larry Smith, and John Prymak; IEEE Electrical Performance of Electronic Packaging Conference; August 1998

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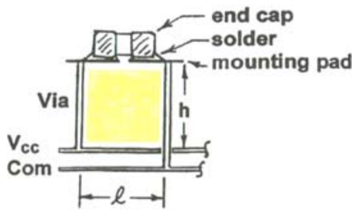
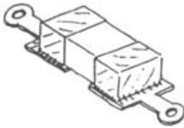
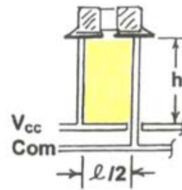
Reducing SM Decoupling Capacitor PCB Assembly Equivalent Inductance by Minimizing Via Separation and Via Length[1]



$L_{eq} \propto \ell \times h$

SM Capacitor PCB mounting technique Circa 1995

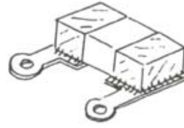


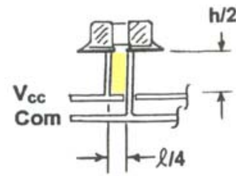


$L' \propto \ell/2 \times h$

$L' = \underline{L_{eq}/2}$

SM Capacitor PCB mounting technique Circa 1997





$L'' \propto \ell/4 \times h/2$

$L'' = \underline{L_{eq}/8}$

SM Capacitor PCB mounting technique Circa 1999

[1]Adopted from "Power Distribution System Design Methodology and Capacitor Selection for Modern CMOS Technology", Larry Smith, et. al., *IEEE Transactions on Advanced Packaging*, Vol. 22, No. 3, August 1999

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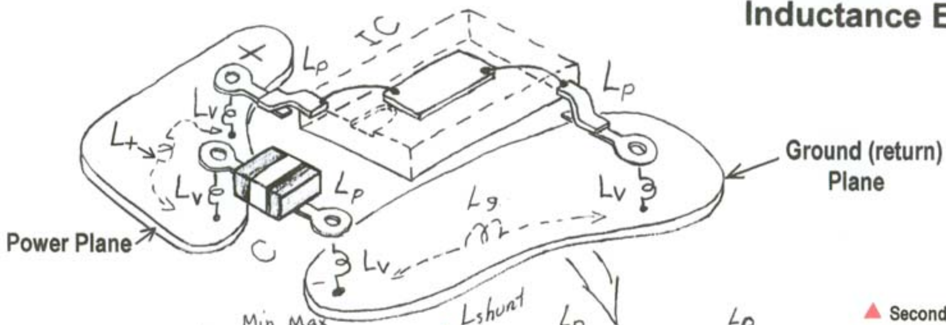
Visualization Sketch of Typical Decoupling Capacitor Circuit Showing Parasitic Inductance Effects



▲ Second parallel via, or addition of shunt from capacitor to + pin

		Min Max
L_c	1-2 nH	1-2
L_v	1-1.5 nH	4-6
L_p	Σ ≈ 1nH	1 1
L_g	≈ .1nH	.1 .1
L_+	≈ .1nH	.1 .1
		6.2 - 9.2

Minimized "L" (see ▲'s)

$L_c = 0.1$ nH (AVX "IDC")

$L_v = 1$ nH (bridged and shunted)

$L_p \simeq .8$ nH

$L_g \simeq .1$ nH

$L_+ \simeq \underline{.1 \text{ nH}}$

$L_{Total} \simeq 2.1$ nH

$$|\Delta e| = L \frac{\Delta i}{\Delta t}$$

$$R_{dyn} = \Delta e / \Delta i = L / \Delta t$$

L_T, nH	R_{dyn}	F_r resonance
9.2	18 Ω	3 MHz
6.2	12 Ω	6 MHz
2.1	4 Ω	11 MHz

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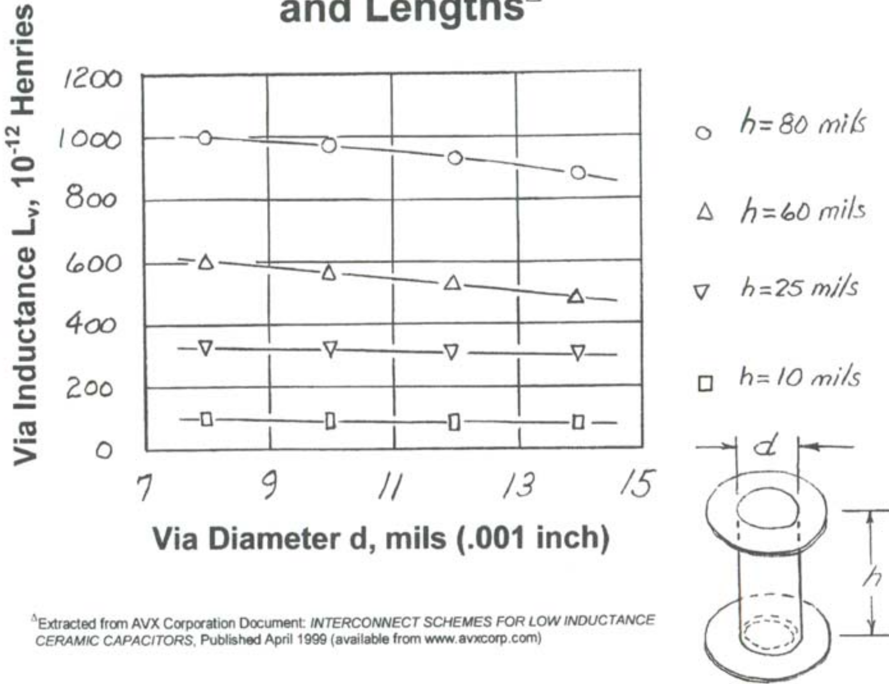
Inductance for Various Via Diameters and Lengths[Δ]



[Δ]Extracted from AVX Corporation Document: *INTERCONNECT SCHEMES FOR LOW INDUCTANCE CERAMIC CAPACITORS*, Published April 1999 (available from www.avxcorp.com)

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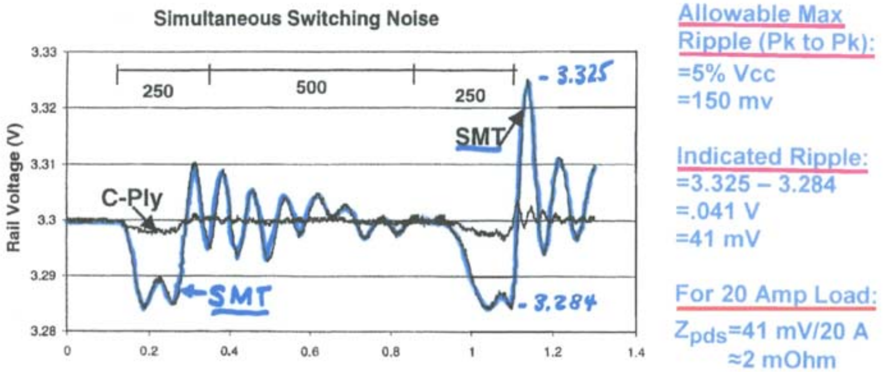
PWB Power Supply Noise Ripple Comparison for Surface Mount (SM) and Embedded Capacitor Decouplers[▲]



Curves based on numerical analysis of idealized board using Partial Element Equivalent Circuit (PEEC) formulation—

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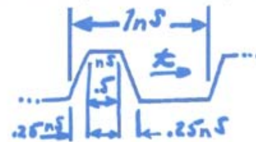

[▲]Diaz-Alvarez et al: MODELING AND SIMULATION OF INTEGRATED CAPACITORS, pages 611-619, *IEEE Transactions on Components and Packaging Technologies*, December 2000

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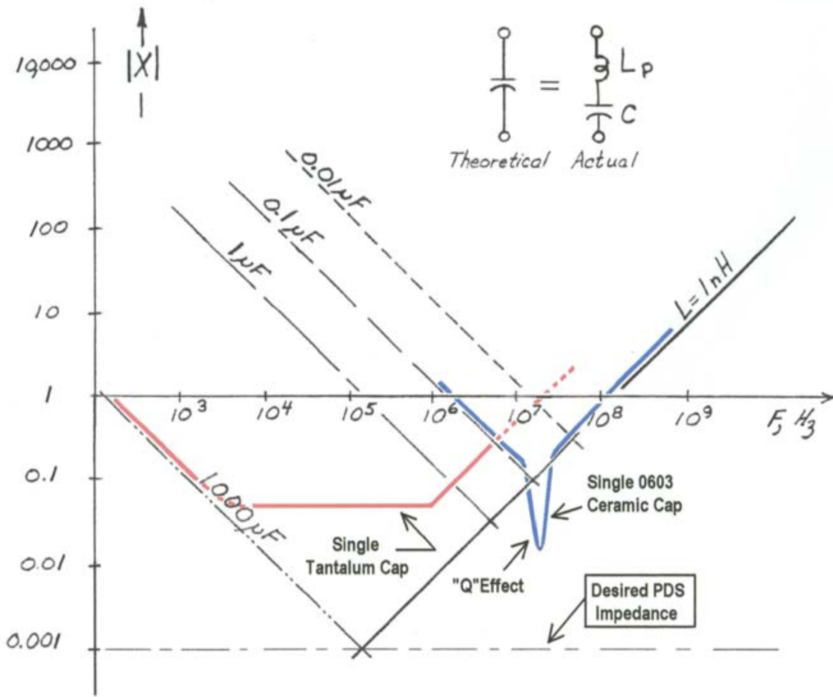
Conceptual Sketch Showing Surface Mount Capacitor Parasitic Inductance Effects



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Low Inductance Chip Capacitors

Low Inductance Chip Arrays (LICA®)

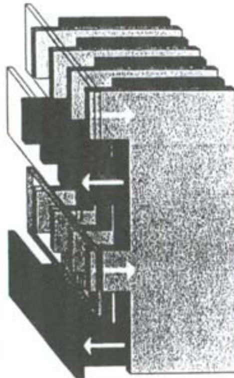


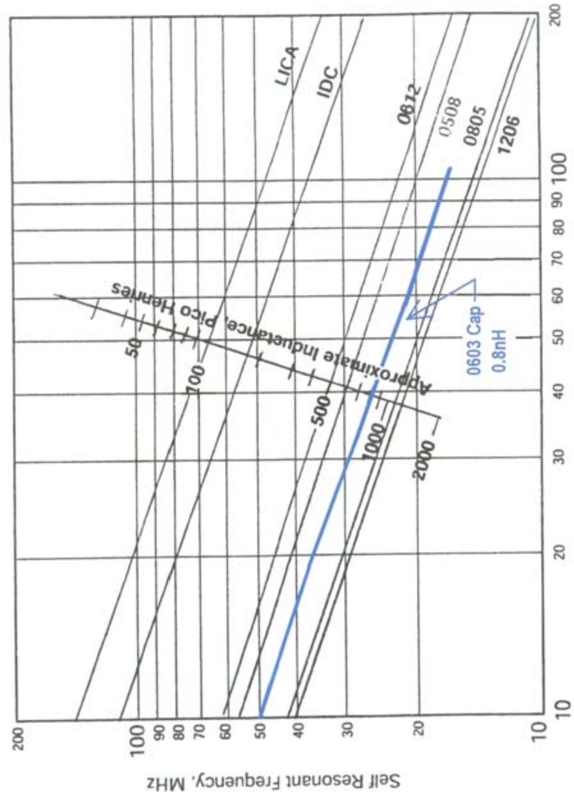
Figure 4. LICA's Electrode/Termination Construction. The current path is minimized – this reduces self-inductance. Current flowing out of the positive plate, returns in the opposite direction along the adjacent negative plate – this reduces the mutual inductance.

Also the effective current path length is minimized because the current does not have to travel the entire length of both electrodes to complete the circuit. This reduces the self inductance of the electrodes. The self inductance is also minimized by the fact that the charging current is supplied by both sets of terminals reducing the path length even further!

The inductance of this arrangement is less than 100 pH, causing the self-resonance to be above 50 MHz for the same popular 100 nF capacitance. Parts available in the LICA design are shown on pages 6 and 7.

Figure 5 compares the self resonant frequencies of various capacitor designs versus capacitance values. The approximate inductance of each style is also shown.

Active development continues on low inductance capacitors. C4 termination with low temperature solder is now available for plastic packages. Consult AVX for details.



Self Resonant Frequencies vs. Capacitance and Capacitor Design

Figure 5

Curve shown courtesy of AVX Corp

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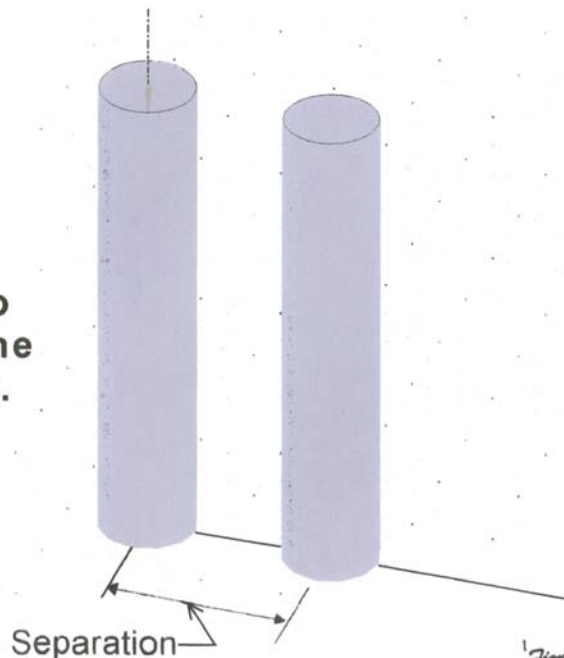
Two Via Simulation Model[1]

Via diameter: 15 mils
Via height: 62 mils
Via separation: variable

Simulation model of two vias embedded in a plane – Note absence of pads.



[1] Figure Courtesy of:

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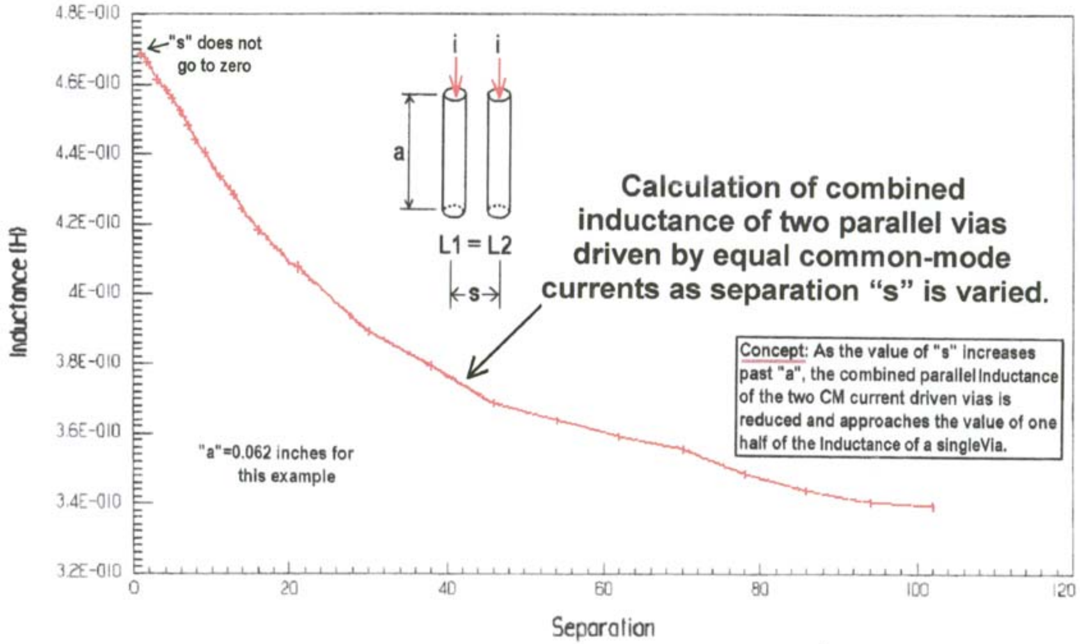
Via Common-Mode Current Scenario[1]



[1] *Calculations and Figure Courtesy of:*

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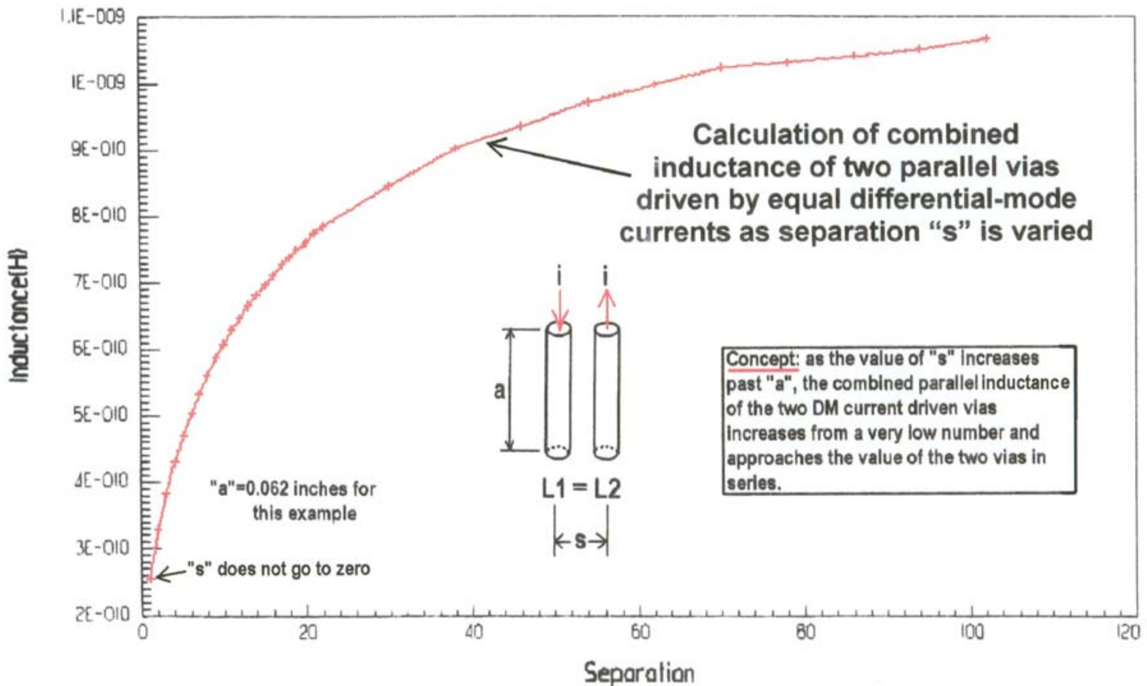
Via Differential Current Scenario[1]



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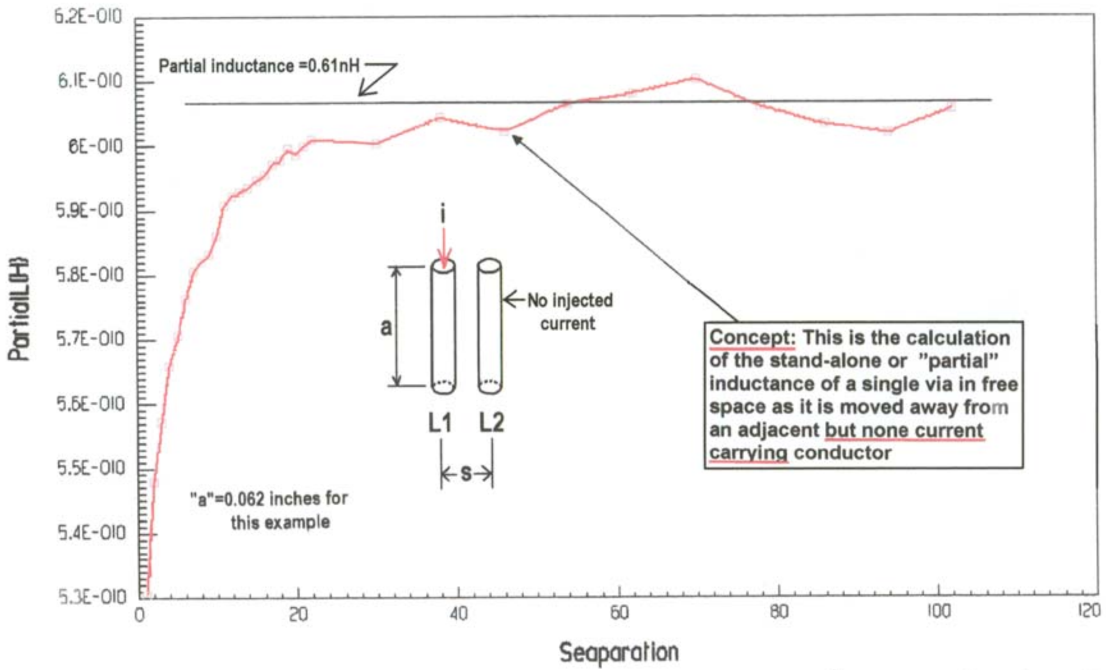
Single "Stand-Alone" Via Scenario[1]



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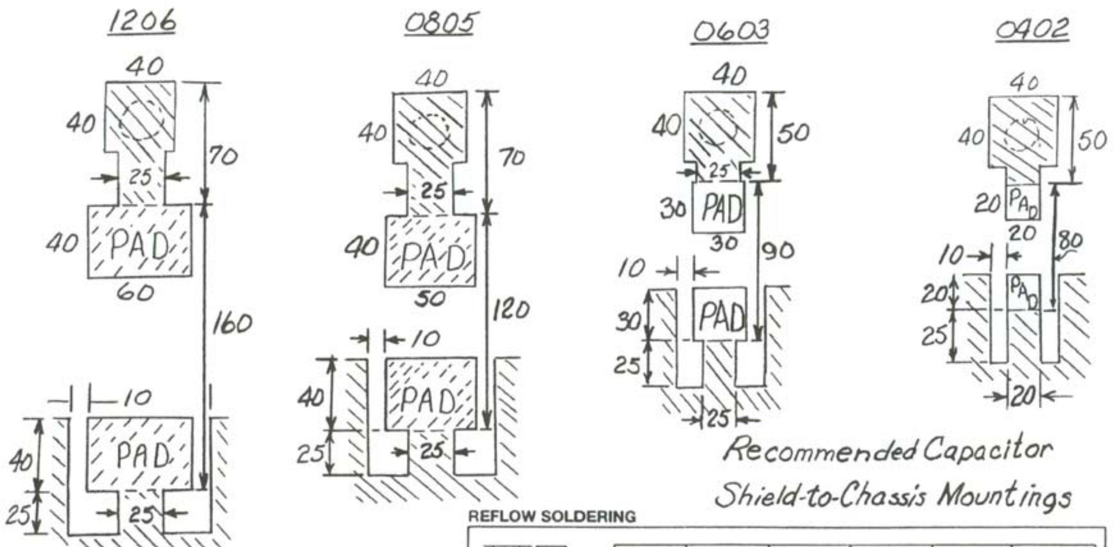

Sketch dimensions in mils (.001")

REFLOW SOLDERING

Case Size	D1	D2	D3	D4	D5
0402	1.70 (0.07)	0.60 (0.02)	0.50 (0.02)	0.60 (0.02)	0.50 (0.02)
0603	2.30 (0.09)	0.80 (0.03)	0.70 (0.03)	0.80 (0.03)	0.75 (0.03)
0805	3.00 (0.12)	1.00 (0.04)	1.00 (0.04)	1.00 (0.04)	1.25 (0.05)
1206	4.00 (0.16)	1.00 (0.04)	2.00 (0.09)	1.00 (0.04)	1.60 (0.06)
1210	4.00 (0.16)	1.00 (0.04)	2.00 (0.09)	1.00 (0.04)	2.50 (0.10)
1808	5.60 (0.22)	1.00 (0.04)	3.60 (0.14)	1.00 (0.04)	2.00 (0.08)
1812	5.60 (0.22)	1.00 (0.04)	3.60 (0.14)	1.00 (0.04)	3.00 (0.12)
1825	5.60 (0.22)	1.00 (0.04)	3.60 (0.14)	1.00 (0.04)	6.35 (0.25)
2220	6.60 (0.26)	1.00 (0.04)	4.60 (0.18)	1.00 (0.04)	5.00 (0.20)
2225	6.60 (0.26)	1.00 (0.04)	4.60 (0.18)	1.00 (0.04)	6.35 (0.25)

Dimensions in millimeters (inches)

Surface Mounting Guide AVX

MLC Chip Capacitors

Component Pad Design

Component pads should be designed to achieve good solder filets and minimize component movement during reflow soldering. Pad designs are given below for the most common sizes of multilayer ceramic capacitors for both wave and reflow soldering. The basis of these designs is:

- Pad width equal to component width. It is permissible to decrease this to as low as 85% of component width but it is not advisable to go below this.
- Pad overlap 0.5mm beneath component.
- Pad extension 0.5mm beyond components for reflow and 1.0mm for wave soldering.

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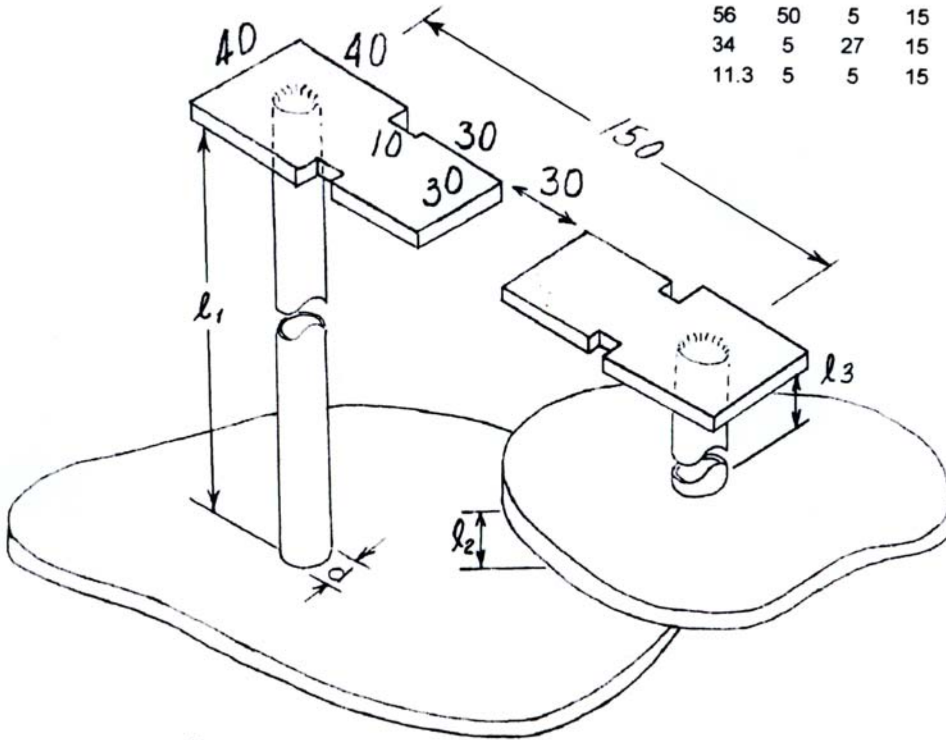
"Standard" SM Capacitor Mounting

l_1	l_2	l_3	d	*Loop* Inductance[1], nH
56	50	5	15	1.10
34	5	27	15	1.54
11.3	5	5	15	0.83

[1] *Calculations Courtesy of:*



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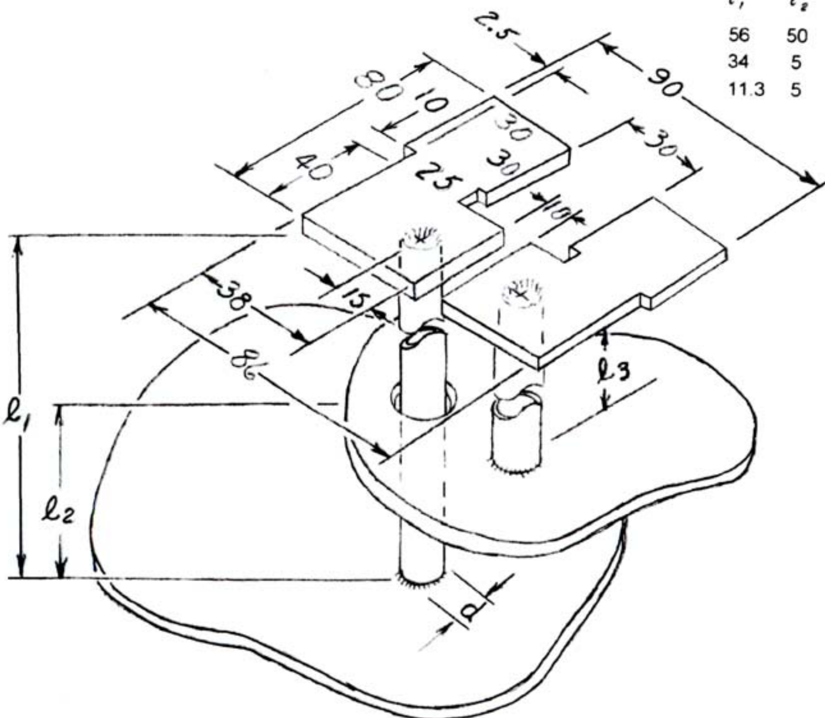
"Enhanced" SM Capacitor Mounting

l_1	l_2	l_3	d	*Loop* Inductance[1], nH
56	50	5	15	0.74
34	5	27	15	0.60
11.3	5	5	15	0.60

[1] *Calculations Courtesy of:*



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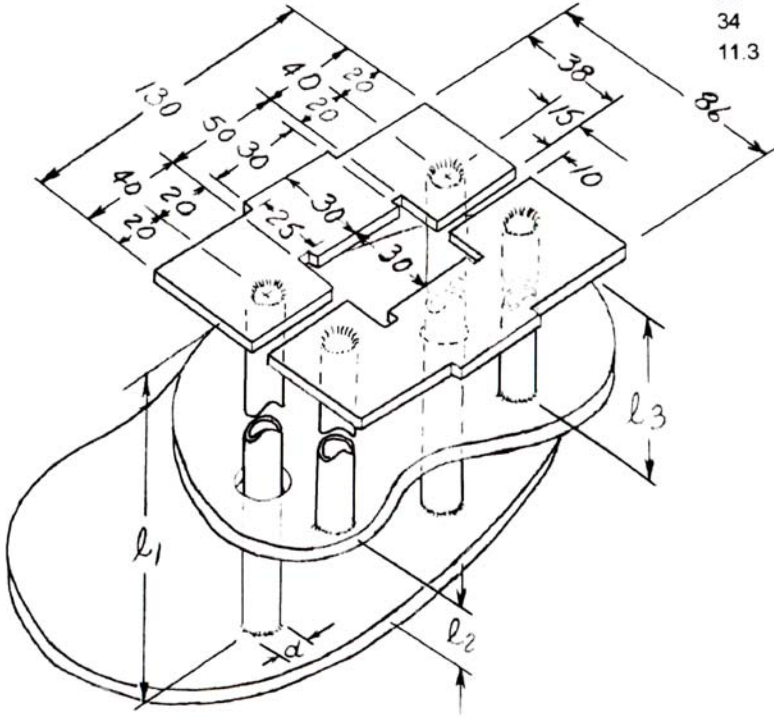
"Optimized" SM Capacitor Mounting

ℓ_1	ℓ_2	ℓ_3	d	*Loop* Inductance[1], nH
56	50	5	15	0.55
34	5	27	15	0.42
11.3	5	5	15	0.23



[1] *Calculations Courtesy of:*

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