Power Integrity and Ground Bounce Simulation of High Speed PCBs

Presentation #11

Agenda

- **Power Integrity (PI) Design Flow**

xDSM Board for Fiber Optic/Broadband Wireless Network

- Resonances on Power/Ground Plane Structure
- Concept of Target Impedance
- Decoupling Capacitor Effects on Power Delivery System (PDS) Impedance
- Full-Wave Spice Model for Power/Ground Planes Using SIwave
- Ground Bounce Simulation Using Full-Wave Spice

- **SIwave Simulation vs. Ansoft HFSS/Measurement**

Power Integrity Design Questions for Multi-Layer PCBs

Q1 : How to layout power/ground plane's structure?

Q2 : How to place IC chips?

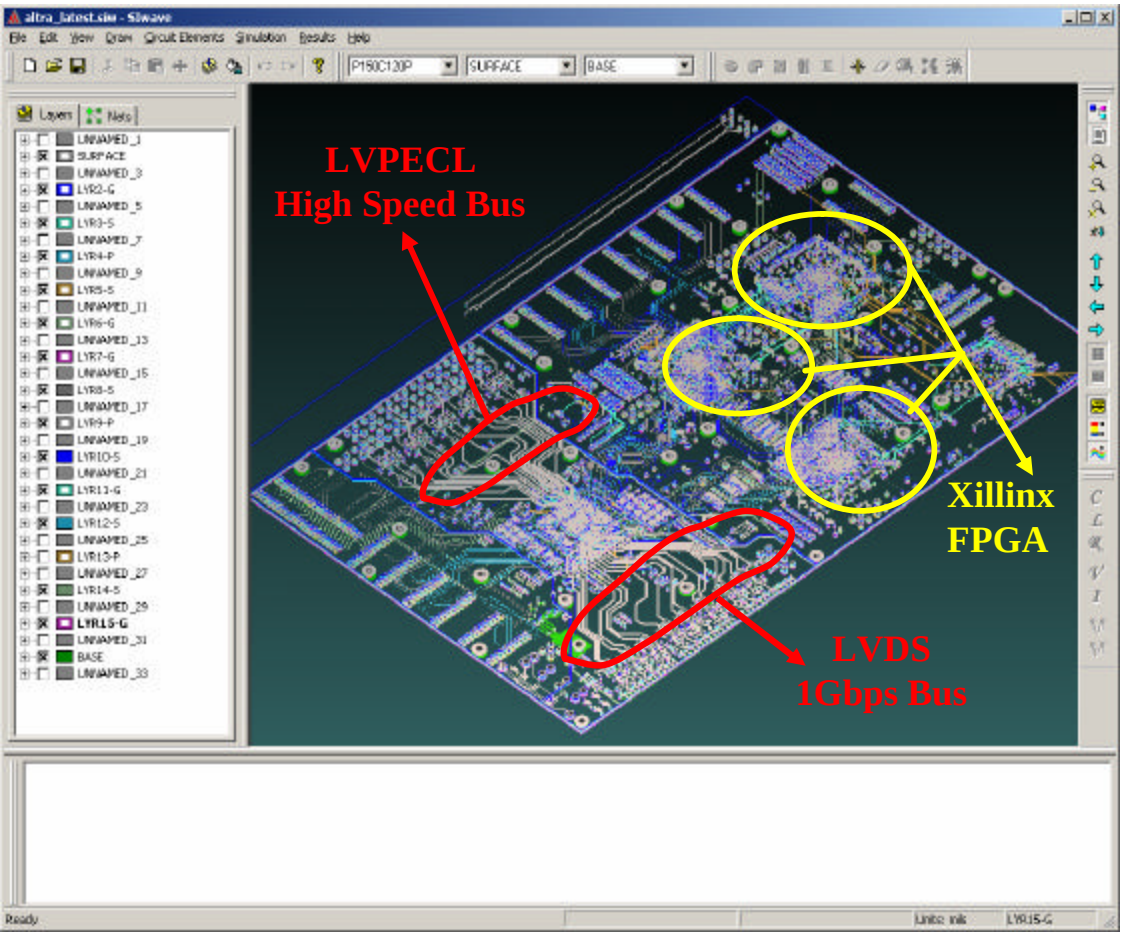
Q3 : How to select decoupling capacitors?

Q4 : How to place the decoupling capacitors ?

Q5 : How many decoupling capacitors are needed?

Q6 : What happens with Ground Bounce Voltage?

An xDSM Board for Fiber Optic and Broadband Wireless Network!



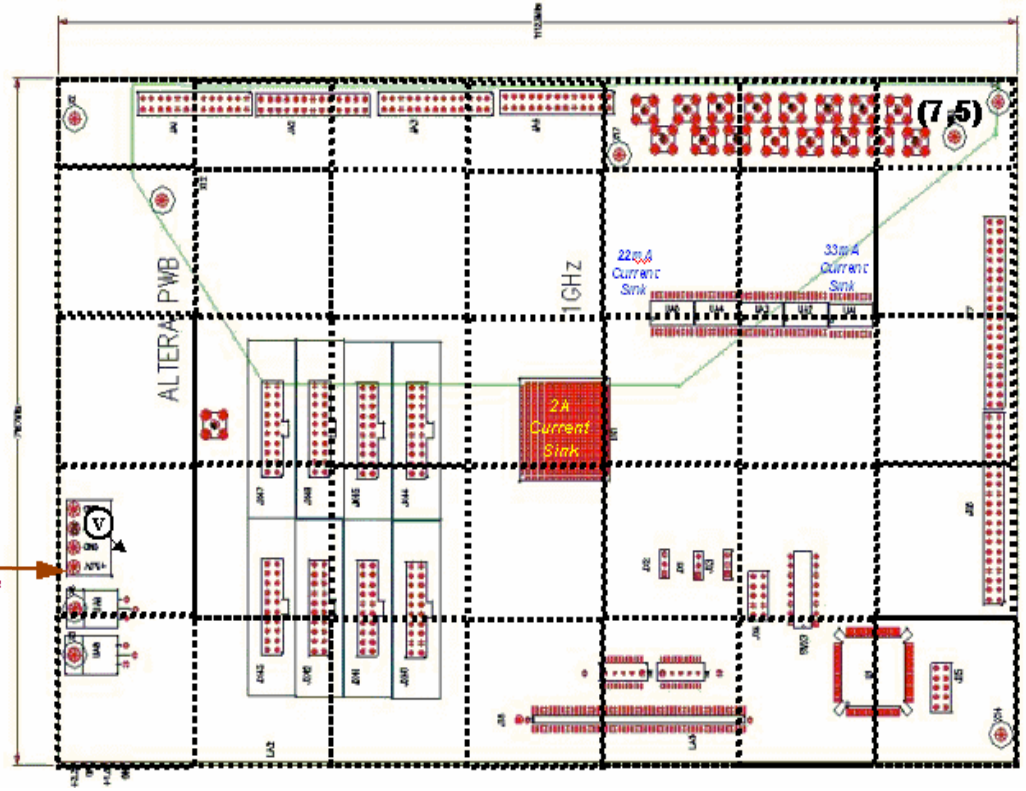
Application:

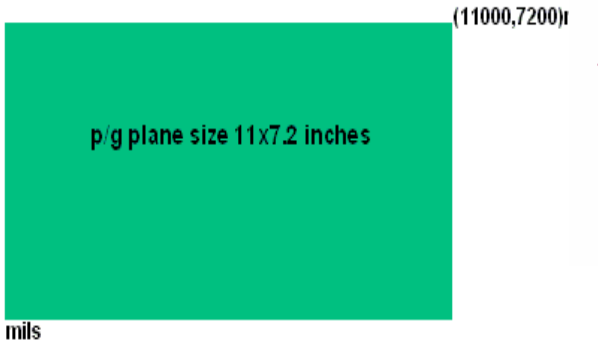
- Fiber Optic and Broadband Wireless Network System.
- 256 QAM/OFDM- 5 Times Larger Bandwidth Efficiency than On/Off Key.

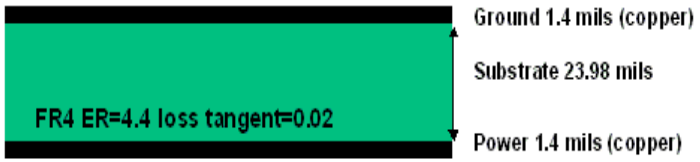
PI Design Goal:

Power/Ground Bounce below 5% of Supply Voltage.

Layer Stack Up and Component Arrangement on **xDSM Board**







Answers for

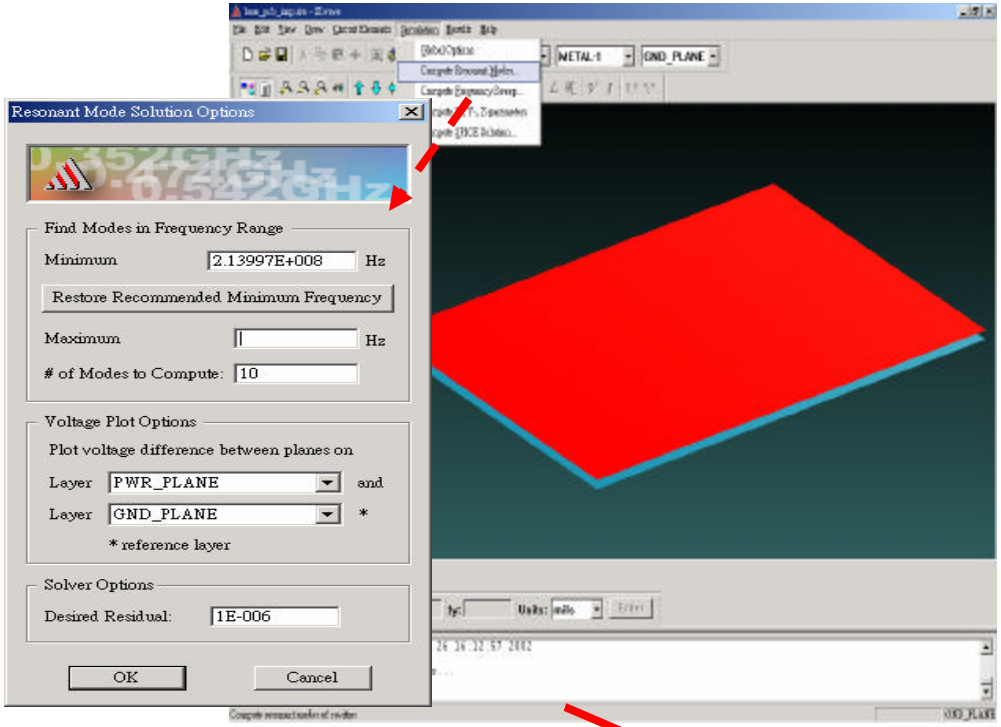
Q1 : How to layout power/ground plane's structure?

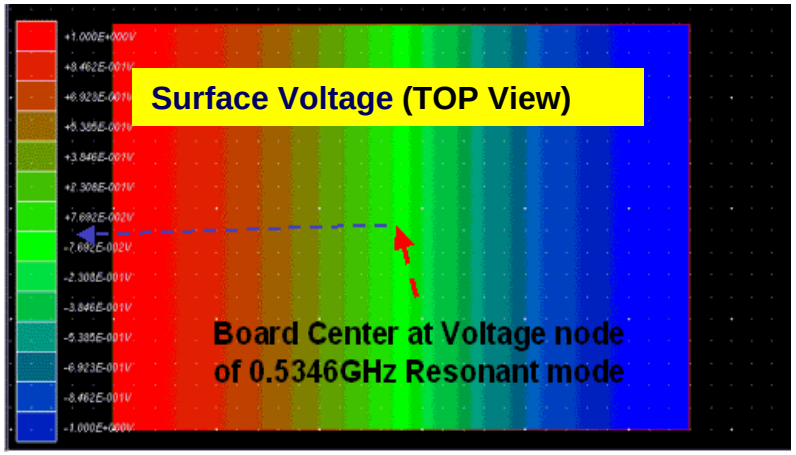
Q2 : How to place IC chips?

Basic Concept :

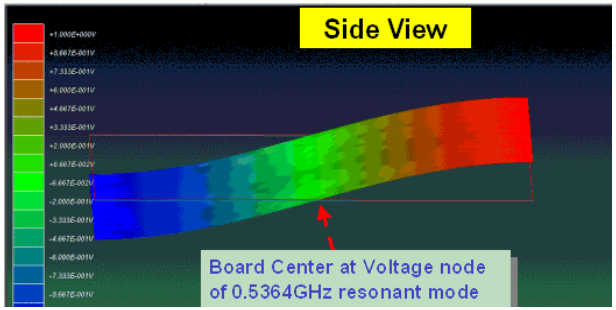
1. **Resonant Mode Voltage Distribution**
2. **Model IC chip as current sink/source**

Pre-Layout and Computing Resonant Modes

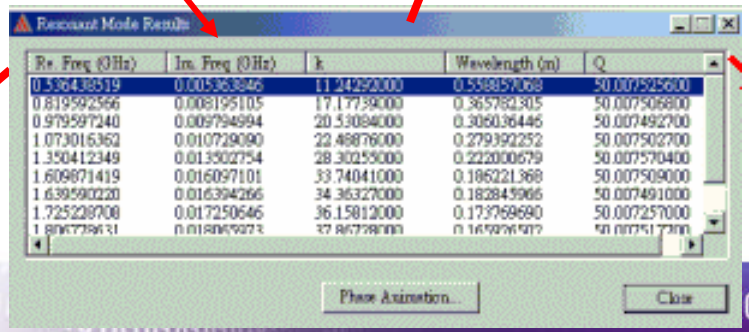




Resonant Mode occur at 0.5364GHz



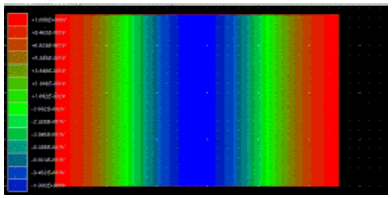
Compute the natural resonant modes for this power/ground structure



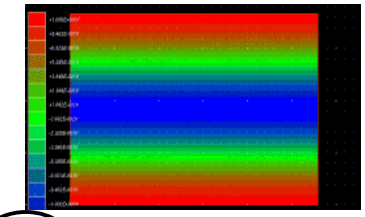
$$\vec{E}(t) \approx e^{jst}$$

$$s = \omega_{real} + j\omega_{imaginary}$$

Resonant Modes and Surface Voltage

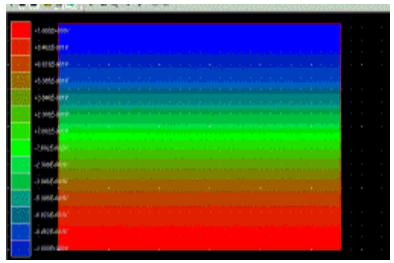


1.073GHz

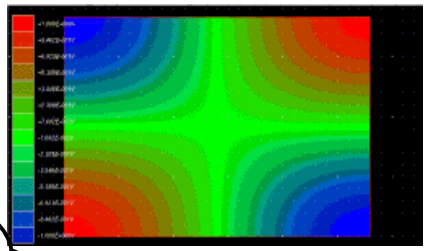


1.639GHz

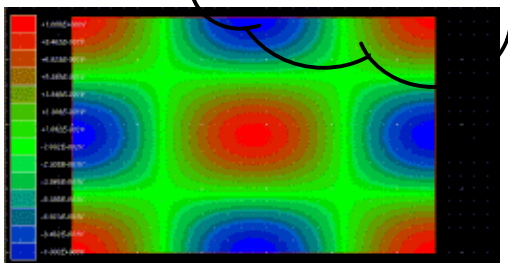
Board Center at Voltage peak/dip for these modes!



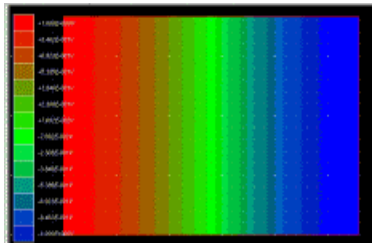
0.81GHz



0.97GHz

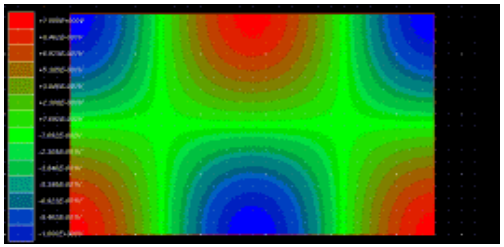


1.96GHz



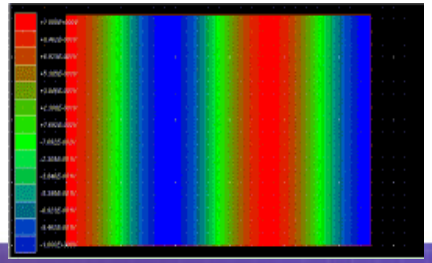
0.536GHz

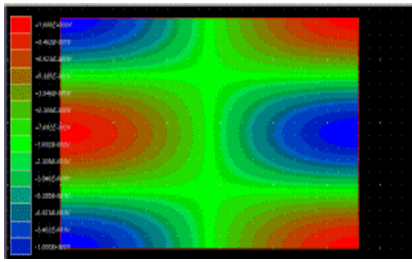
Board Center at Zero Voltage node for these modes!



1.72GHz

1.60GHz





1.35GHz

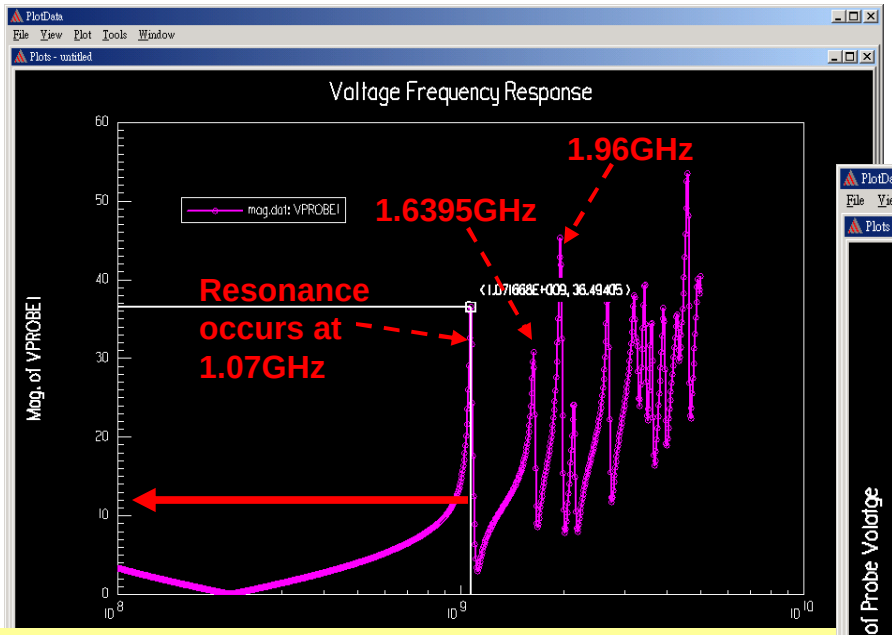
How to Place IC ?

In this case, we have an IC chip which draws 2A at 0.2 ns.

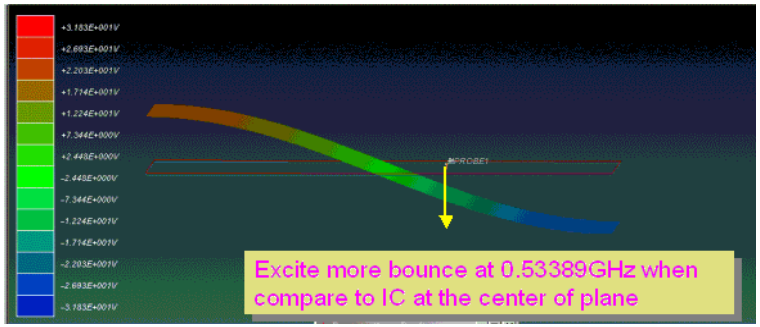
Consider placing this IC at the board center (5500,3600) mils.

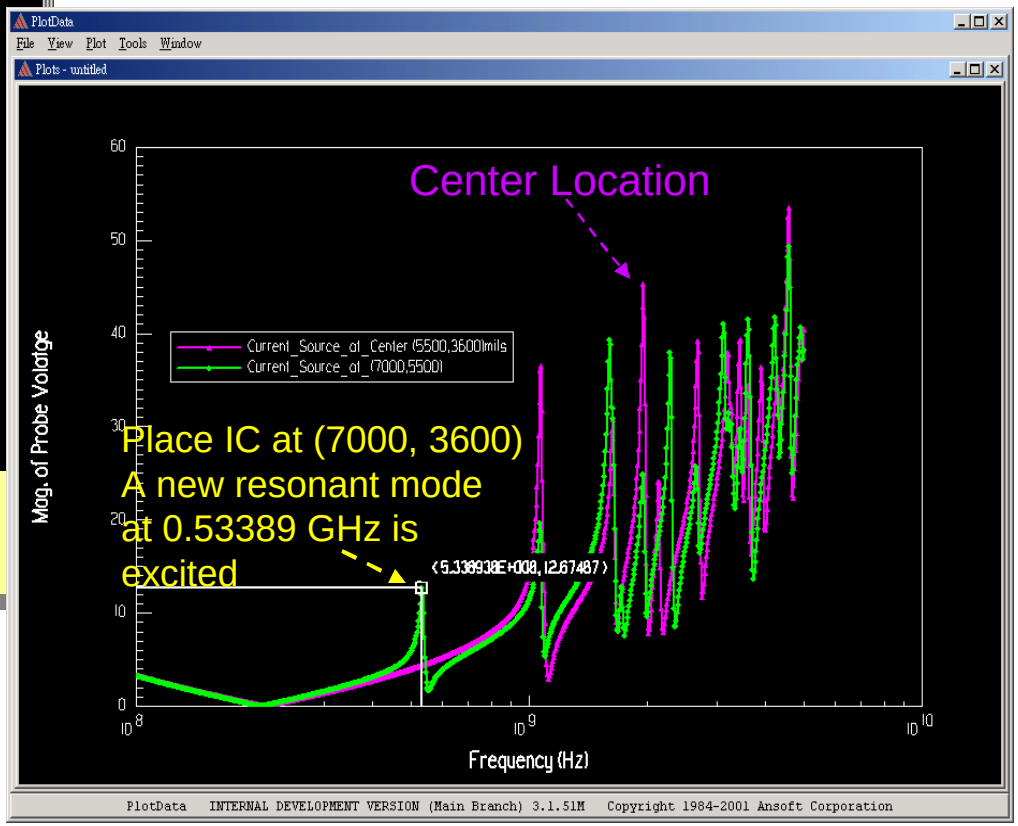
According to the previous plots and the proposed IC location, we can easily predict that only 1.0730, 1.63959 and 1.9600 GHz resonant modes will be excited!

Frequency Response of Voltage Probes when IC Chip Draws Current



There is no resonance below 1GHz, when IC is at the center of the board.





Comparison of Voltage Frequency Response for IC at (5500,3600) and (7000,3600)mils location

Answers for

Q3 : How to select decoupling capacitors?

Q4 : How to place the decoupling capacitors ?

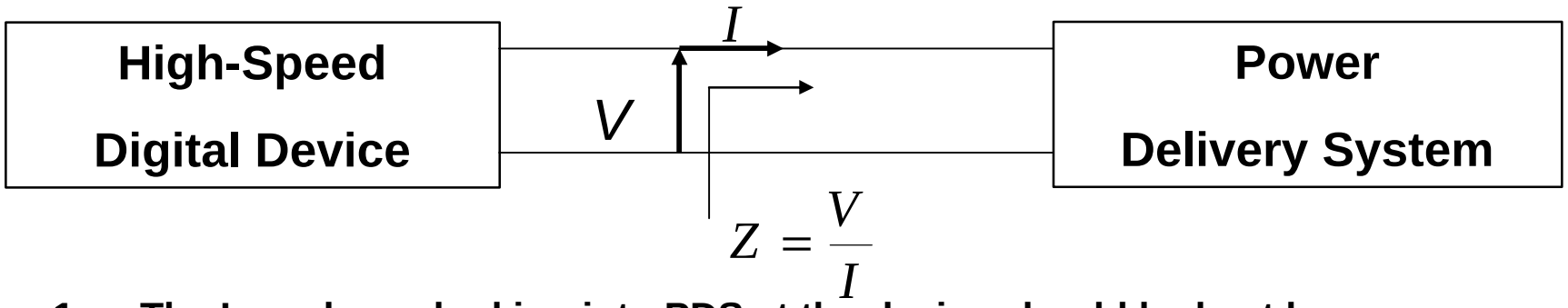
Q5 : How many decoupling capacitors are needed?

Q6 : What happen on Ground Bounce Voltage?

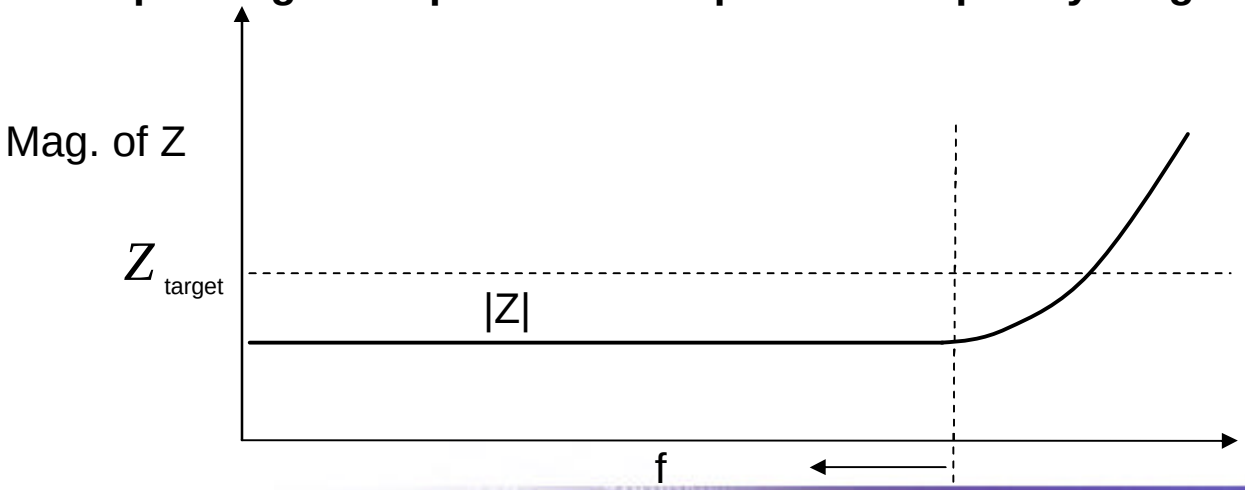
Basic Concept :

1. Plane Impedance due to different structures
2. IC Power/Ground terminal pair as a port
3. Target Impedance
4. Effects of Decoupling Capacitors on PDS
5. Non-Ideal Effects of Decoupling Capacitors

Basic Requirement: Target Impedance of PDS



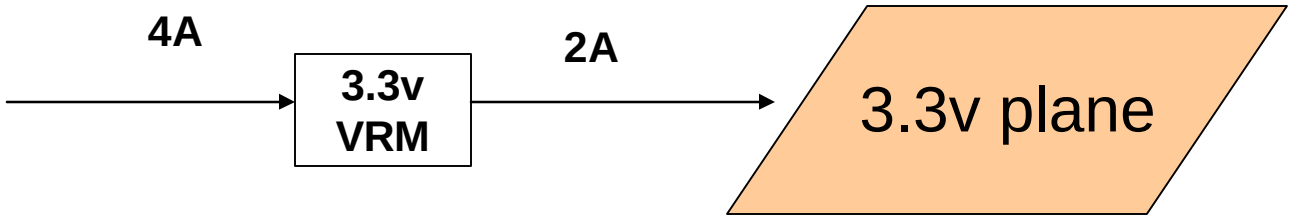
1. The Impedance looking into PDS at the device should be kept low over a broad frequency range (from DC to several harmonics of clock frequency)
2. The Desired Frequency Range and Impedance Value is called **Target Impedance.**
3. The Target impedance goal is set with the help of allowable ripple on the power/ground plane over a specified frequency range.



Target Impedance Calculation

$$Z_{Target} = \frac{(Power\_Supply\_Voltage) \times (Allowed\_Ripple)}{Current}$$

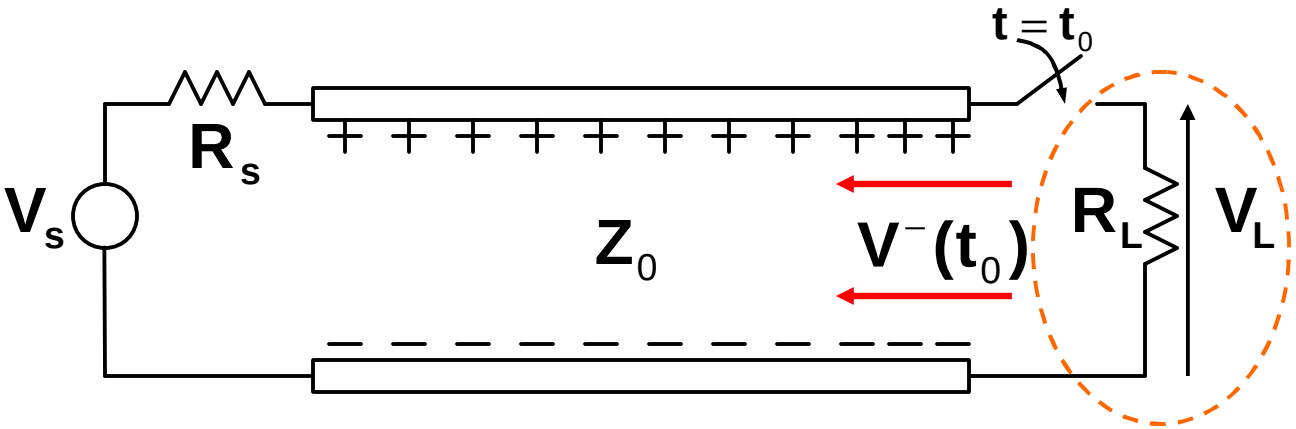
Example:



$$Z_{Target(3.3v)} = \frac{(3.3v) \times (5\%)}{2A} = 82.5m\Omega$$

Target Impendence is the goal that designers should hit !!!

Low Plane Impedance Minimizes Reflective SSN

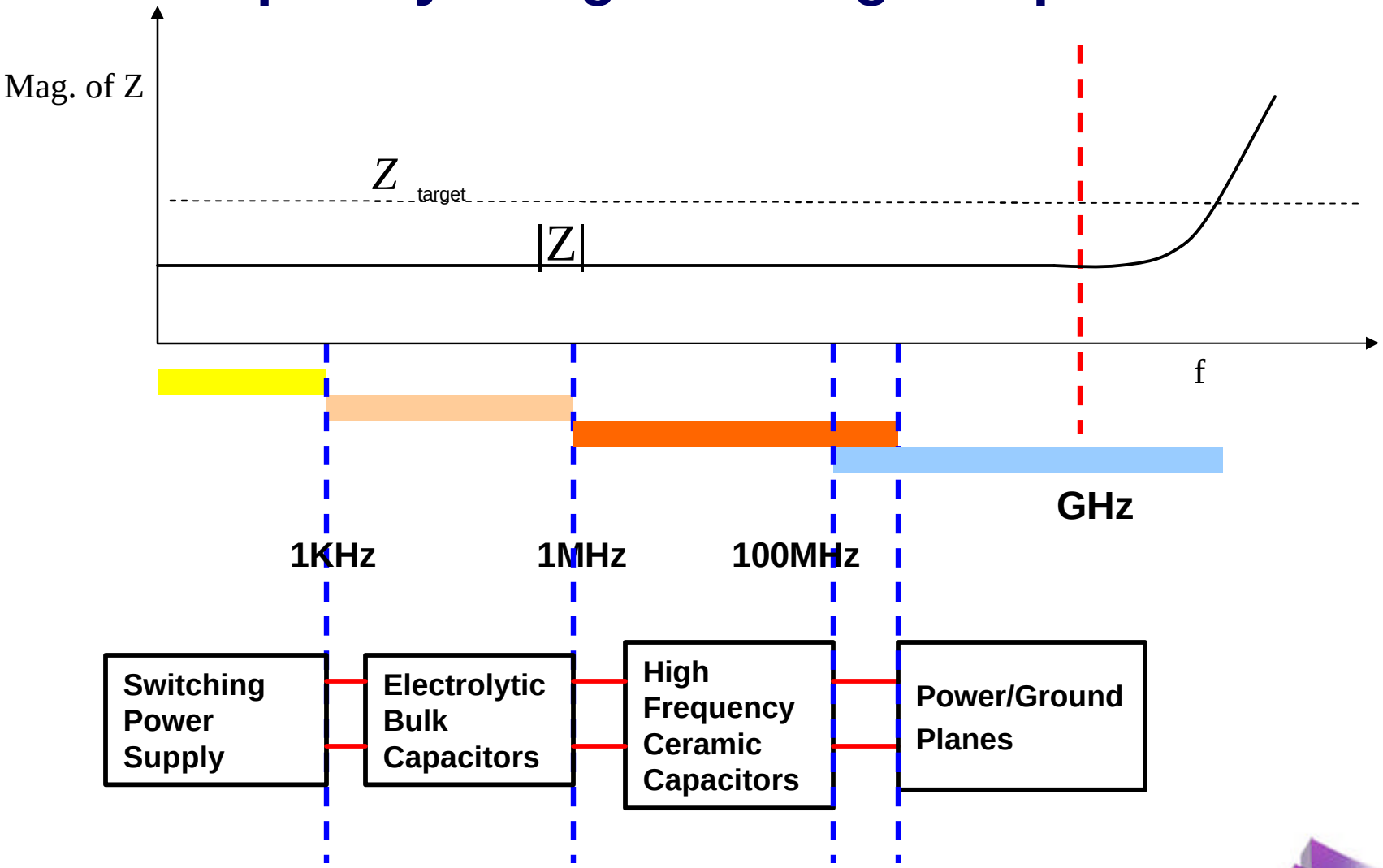


$$V_L(t_0) = \frac{R_L}{R_L + Z_0} V_s$$

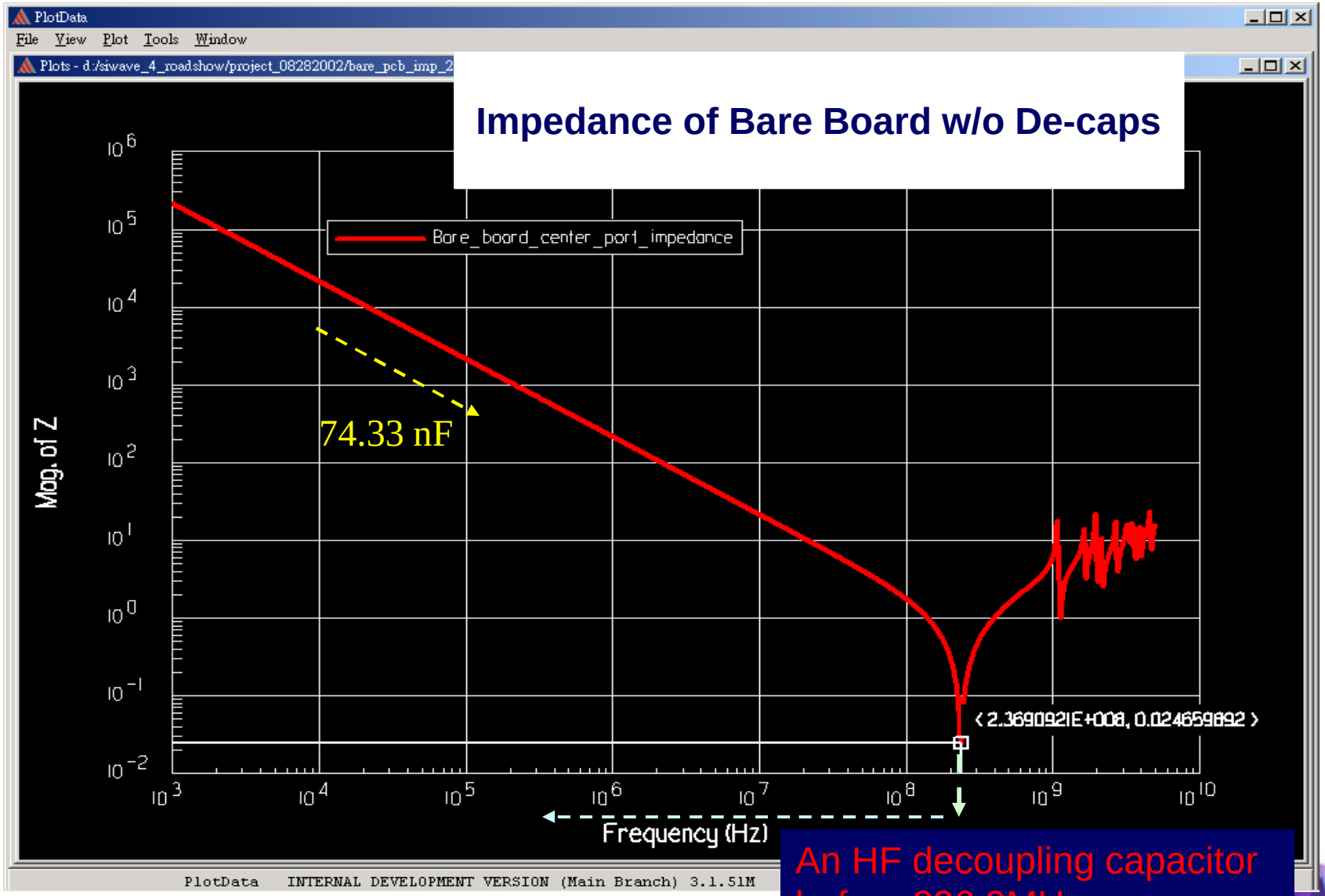
$$V^-(t_0) = V_s - V_L(t_0) = \frac{Z_0}{R_L + Z_0} V_s$$

$$\text{If } Z_0 << R_L \text{, then } V^-(t_0) \to 0$$

PDS Components and their Effective Frequency Range on Target Impedance

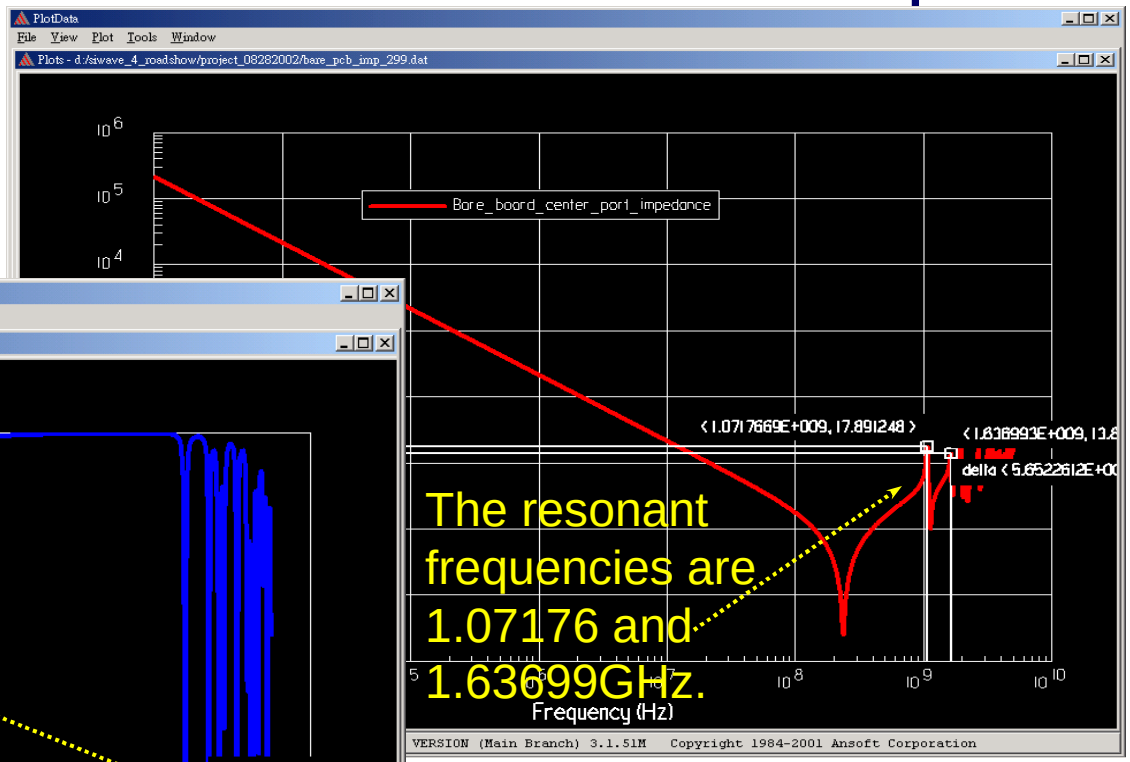


Compute Bare Board S-, Y-, Z-Parameters

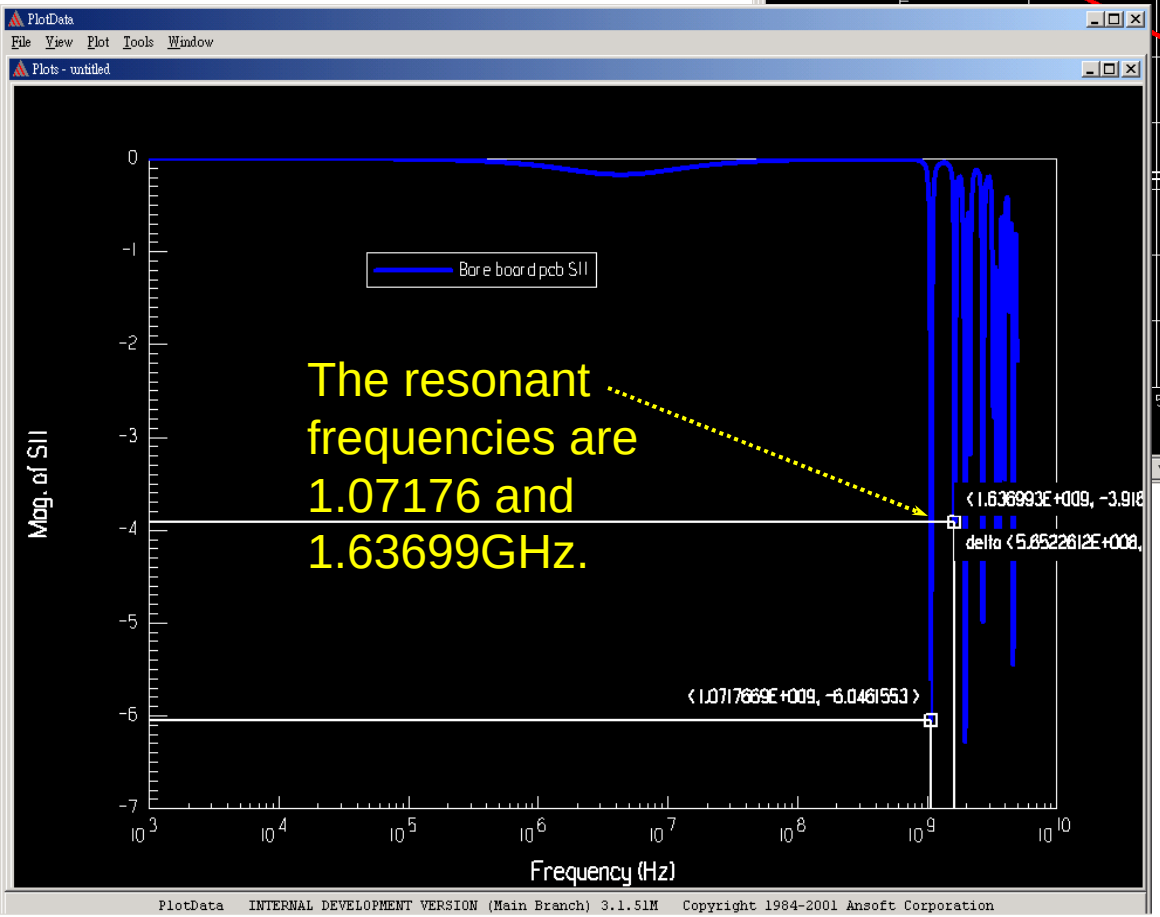


An HF decoupling capacitor before 236.9MHz

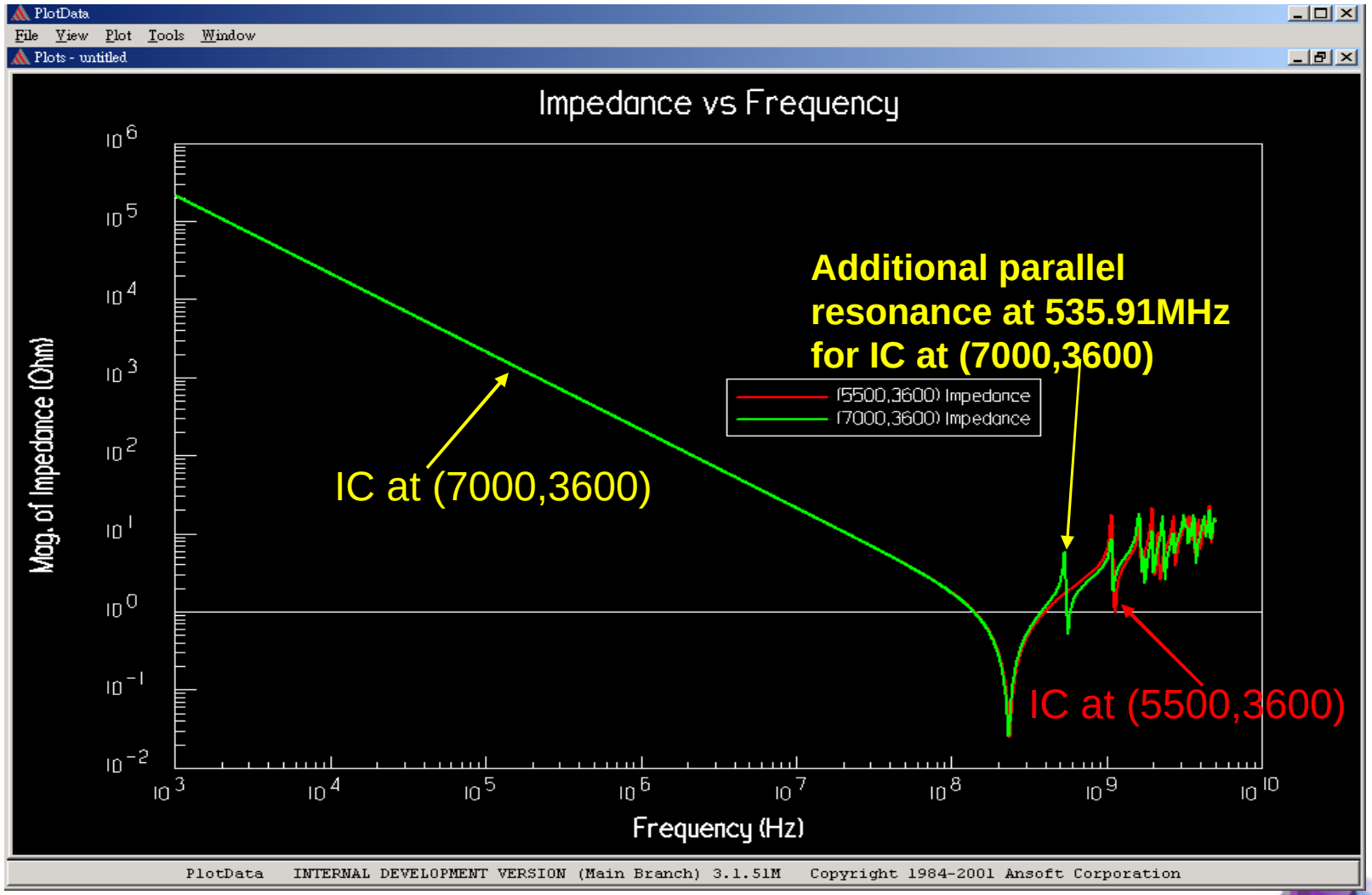
Bare Board Parallel Resonant Frequencies



Bare Board S-Parameters



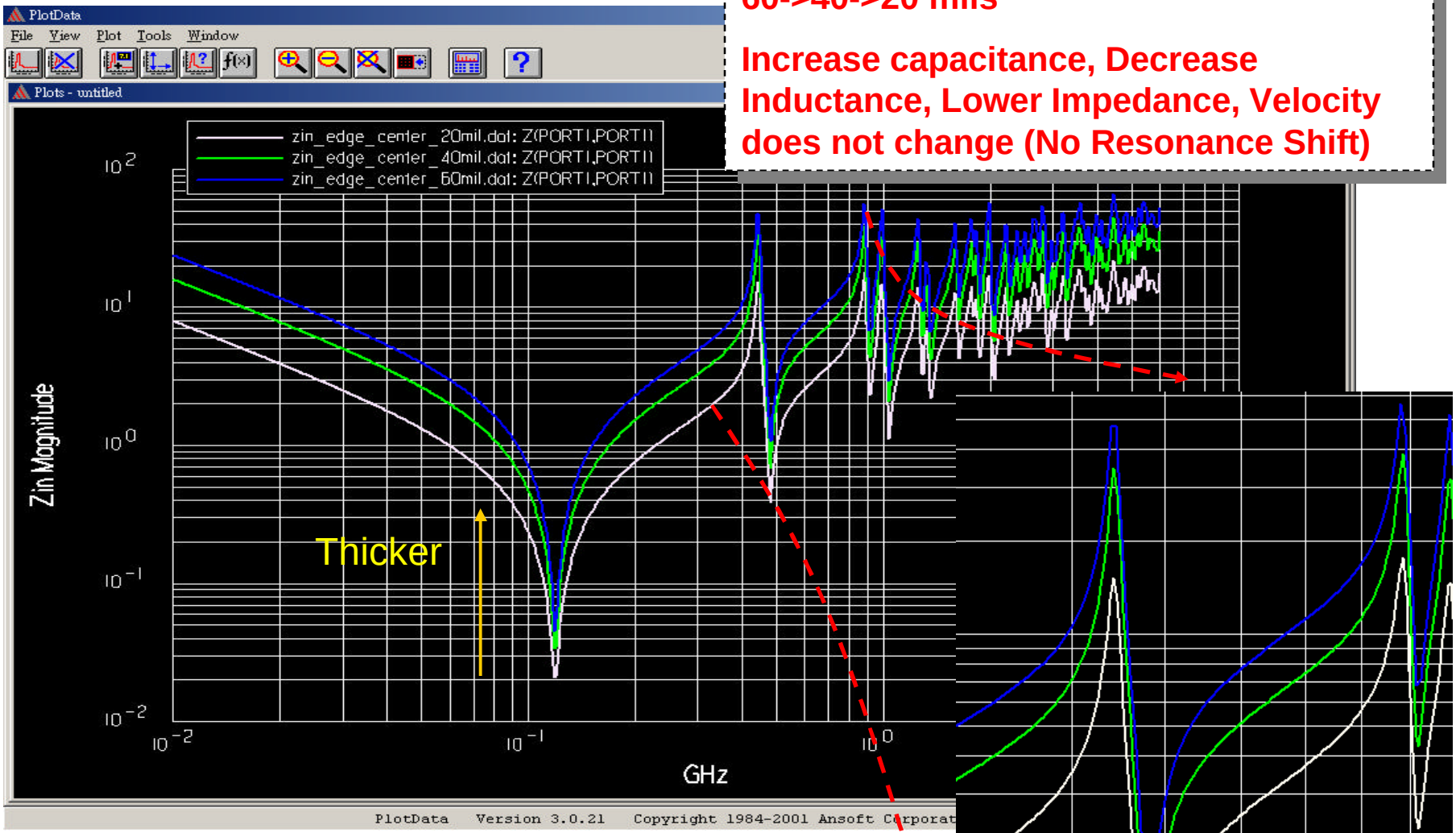
Impedance Comparison for IC at (5500,3600) and (7000,3600) mils



Simulate the Effect of Dielectric Thickness on Plane Impedance

60->40->20 mils

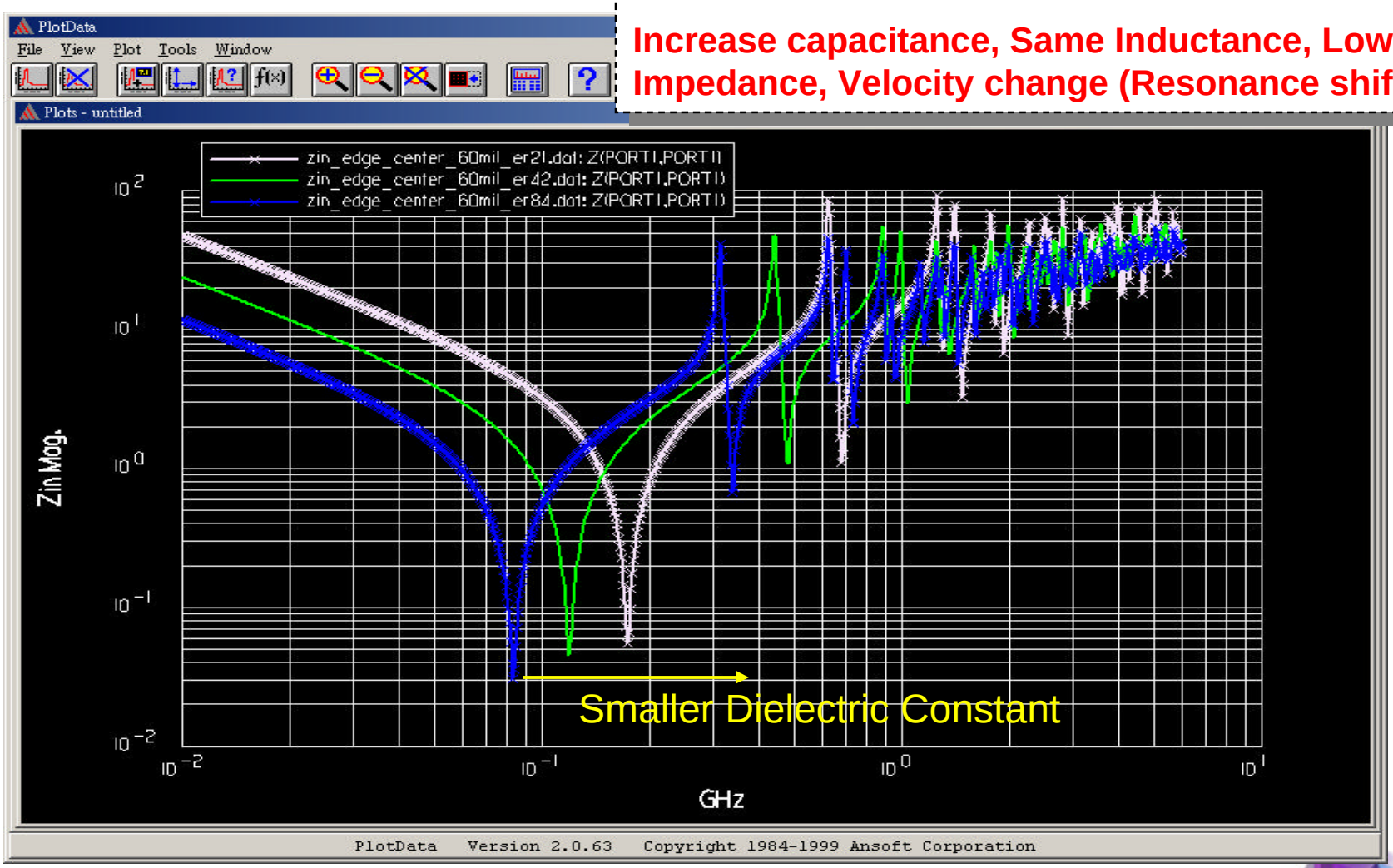
Increase capacitance, Decrease Inductance, Lower Impedance, Velocity does not change (No Resonance Shift)



Simulate the Effect of Dielectric Constant

Er 8.4->4.2->2.1

Increase capacitance, Same Inductance, Lower Impedance, Velocity change (Resonance shift)



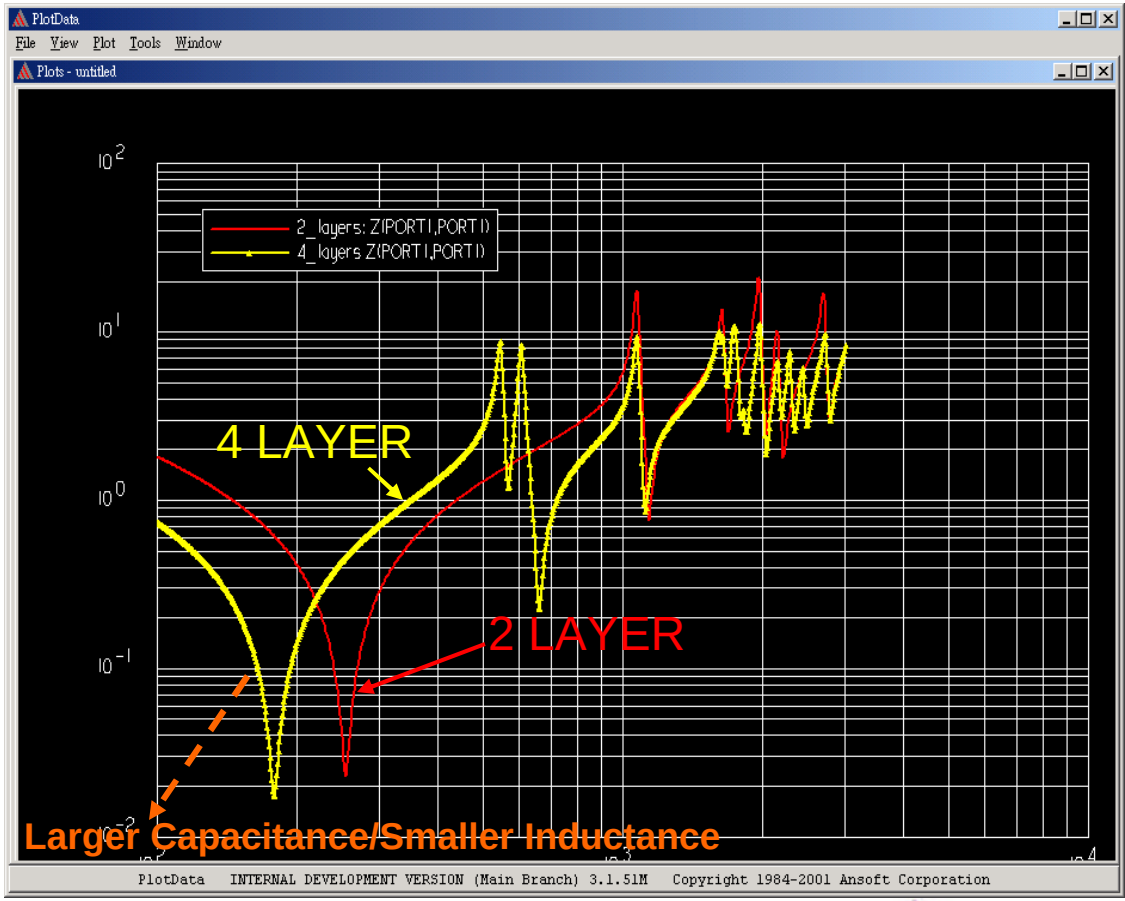
Four Layer Power/Ground Plane Structure

p/g plane size 11x7.2 inches

(11000,7200) mils

(0,0) mils

Compare Impedance for 2/4 layers



Ground 1.4 mils (copper)

FR4 ER=4.4 loss tangent=0.02

Substrate 23.98 mils

Power 1.4 mils (copper)

FR4 ER=4.4 loss tangent=0.02

Substrate 23.98 mils

Power 1.4 mils (copper)

FR4 ER=4.4 loss tangent=0.02

Substrate 23.98 mils

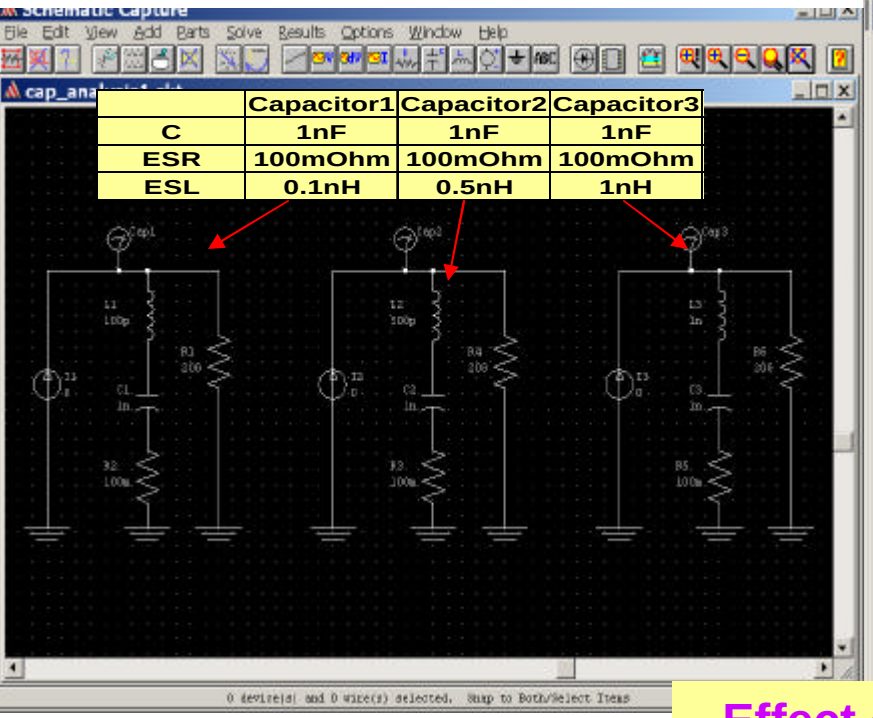
Ground 1.4 mils (copper)

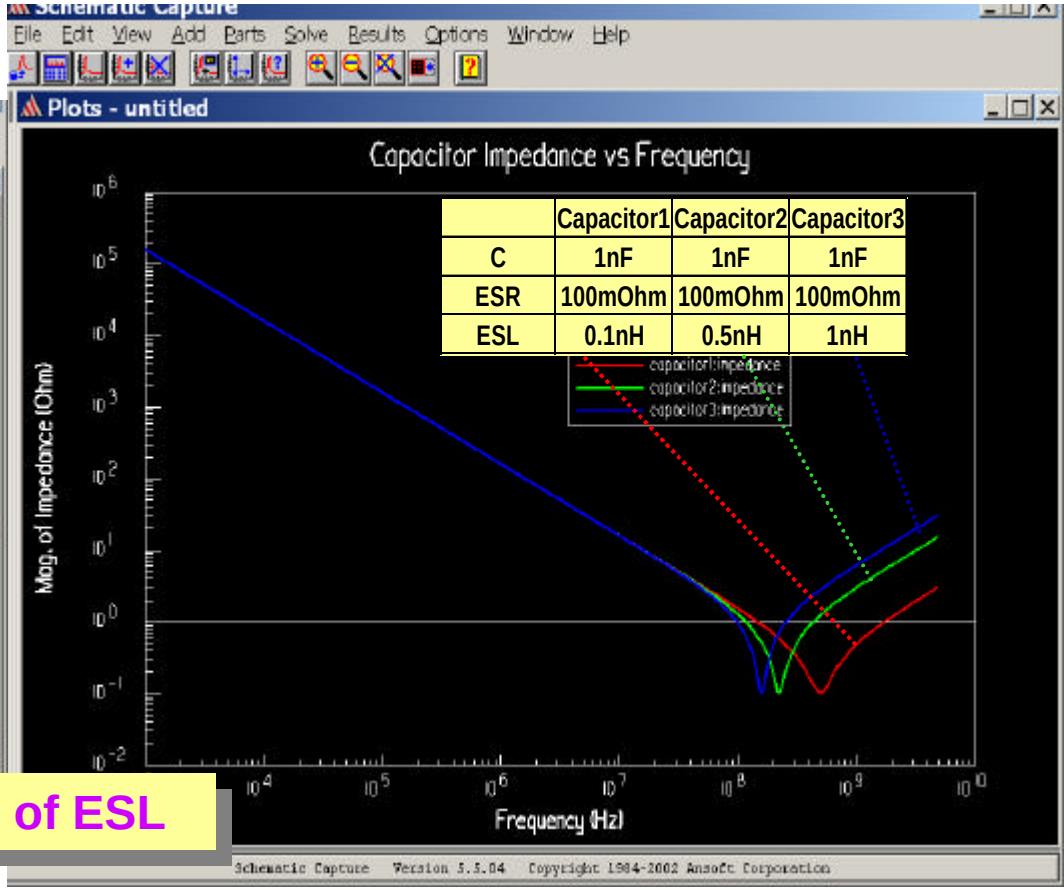
Function of Decoupling Capacitors

1. Supply current bursts for fast switching circuit (PDS issue)
2. Lower impedance of the power delivery system and prevent energy transference from one circuit to another (PDS issue)
3. Provide AC connection between power and ground planes for signal return current
4. Control EMI

The Non-Ideal Effect Analysis of Decoupling Capacitors using Ansoft Full-Wave Spice

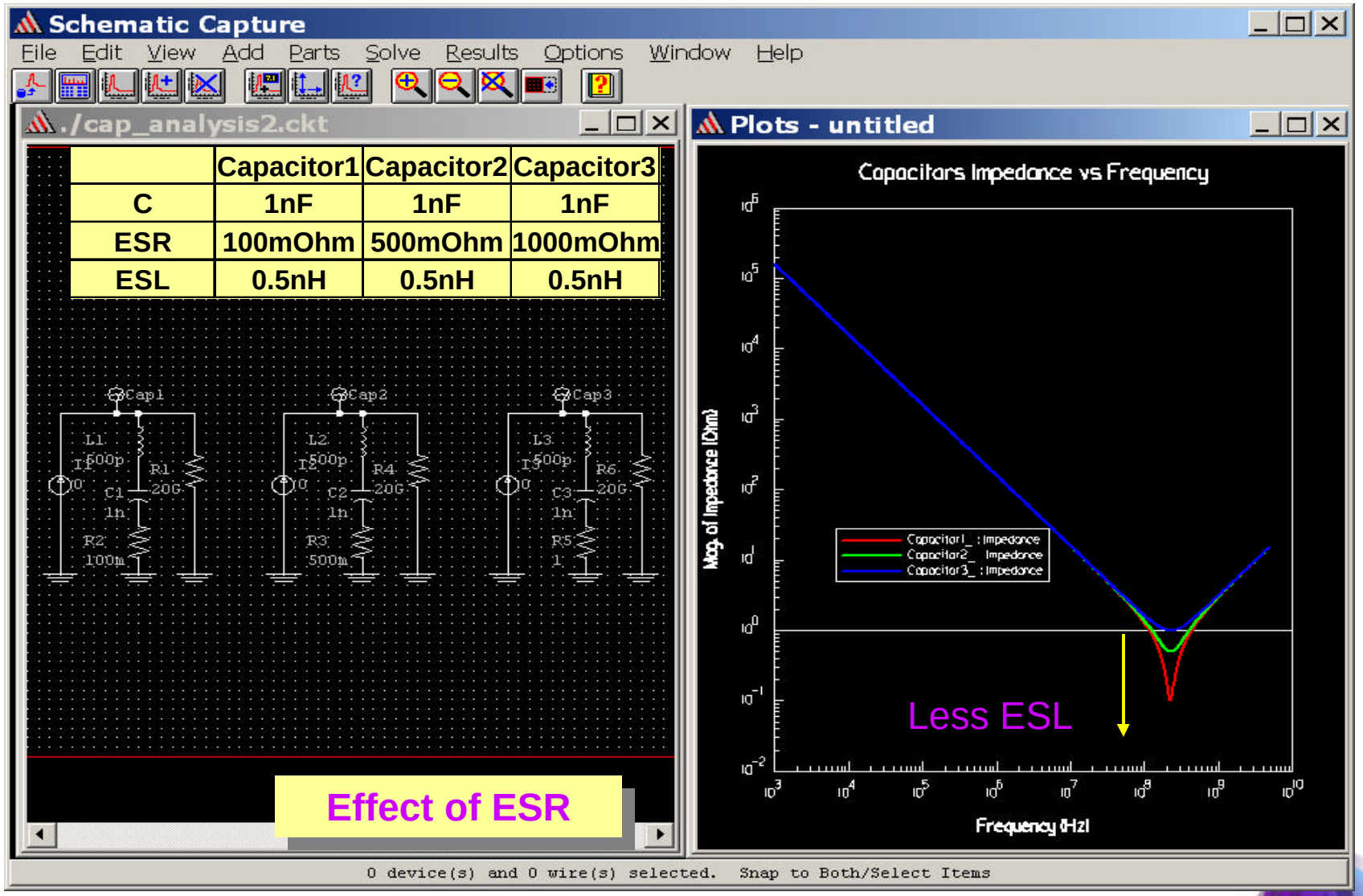
Decoupling Capacitor Impedance for Different ESL



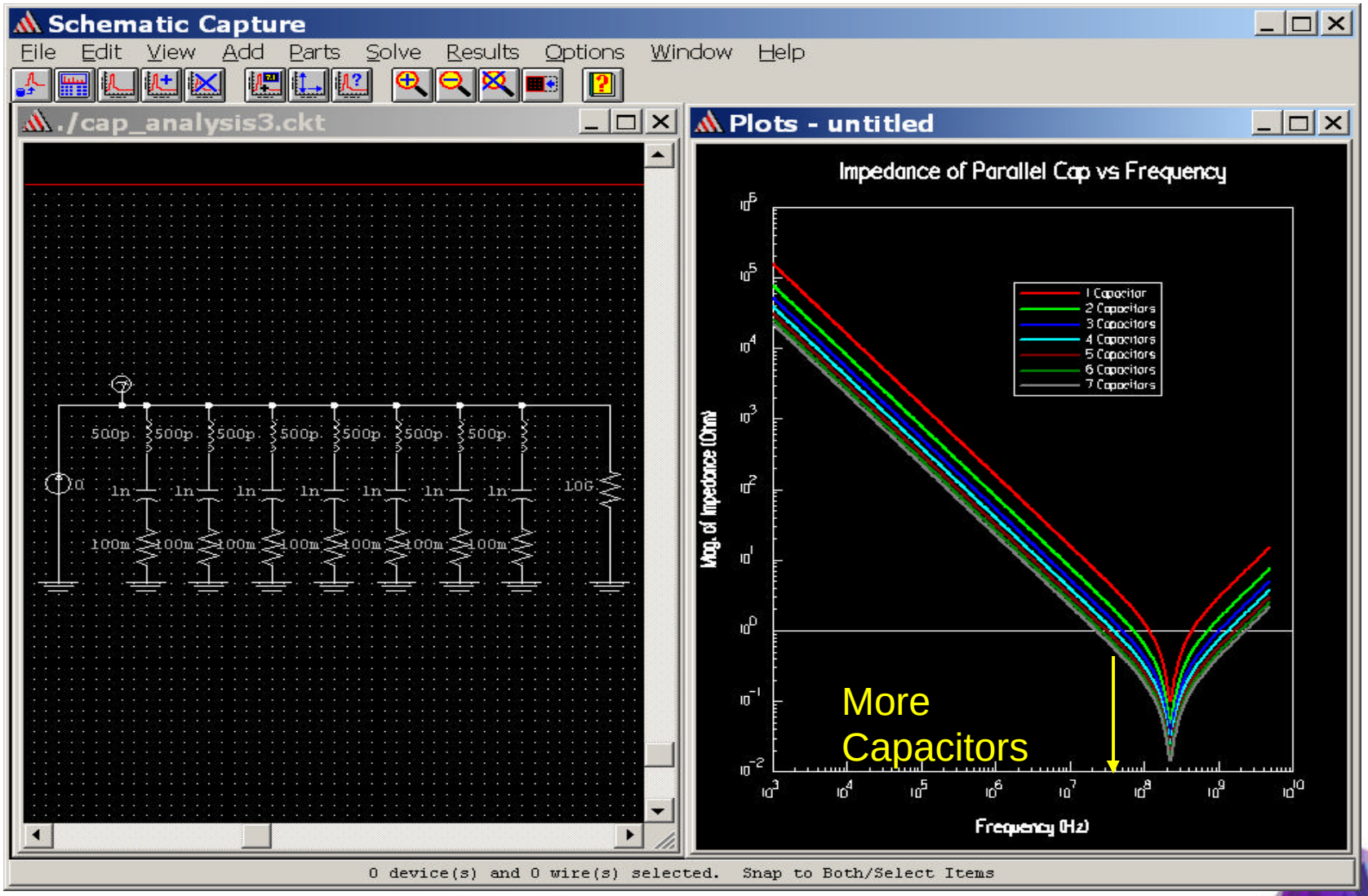


Effect of ESL

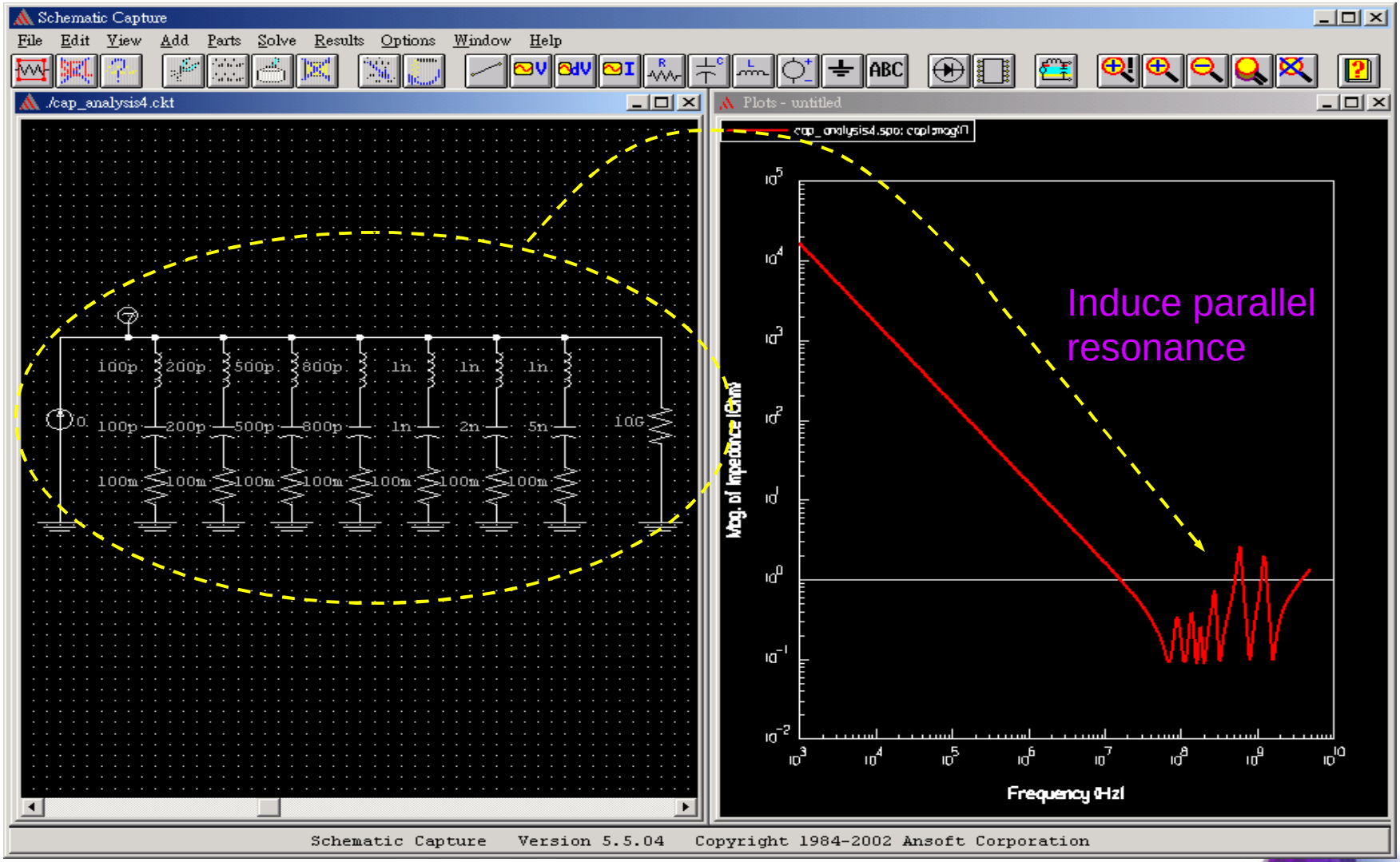
ESR Effect on Decoupling Capacitors



Parallel Capacitors (same values) and Decoupling Capacitor Impedance



Parallel Capacitors (skewed values) and Decoupling Capacitor Impedance

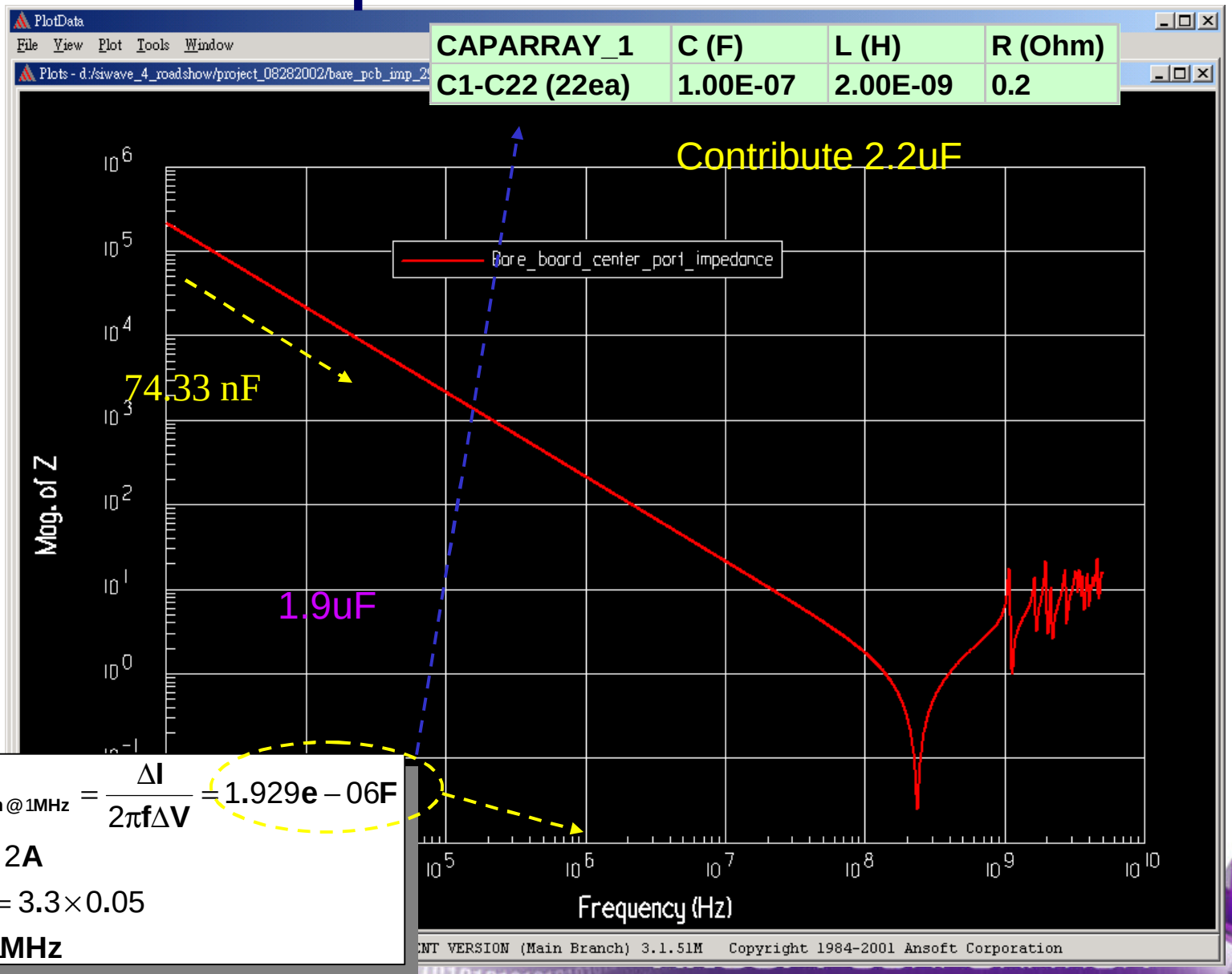


Physical High Frequency Capacitor Characteristics

1. High frequency ceramic capacitors are an increasingly important part of the PDS.
2. Calculations for the number of capacitors necessary to maintain a target impedance are made in the frequency domain.
3. **NPO** capacitors have the **lowest ESR** and **best temperature and voltage properties**, but are **only available up to a few nF**.
4. **X7R** capacitors have reasonable voltage and temperature coefficients and are **available from several nF to several uF**.
5. **X5R** is **similar to X7R**, but with **reduced reliability** and are being **extended to 100uF**.
6. **Y5V** dielectric is used to achieve high capacitance values, but has **very poor voltage and temperature characteristics**.

Calculate the Required Minimum Capacitance Value at 1MHz

CAPARRAY_1	C (F)	L (H)	R (Ohm)
C1-C22 (22ea)	1.00E-07	2.00E-09	0.2



$$C_{mim@1MHz} = \frac{\Delta I}{2\pi f \Delta V} = 1.929e-06F$$

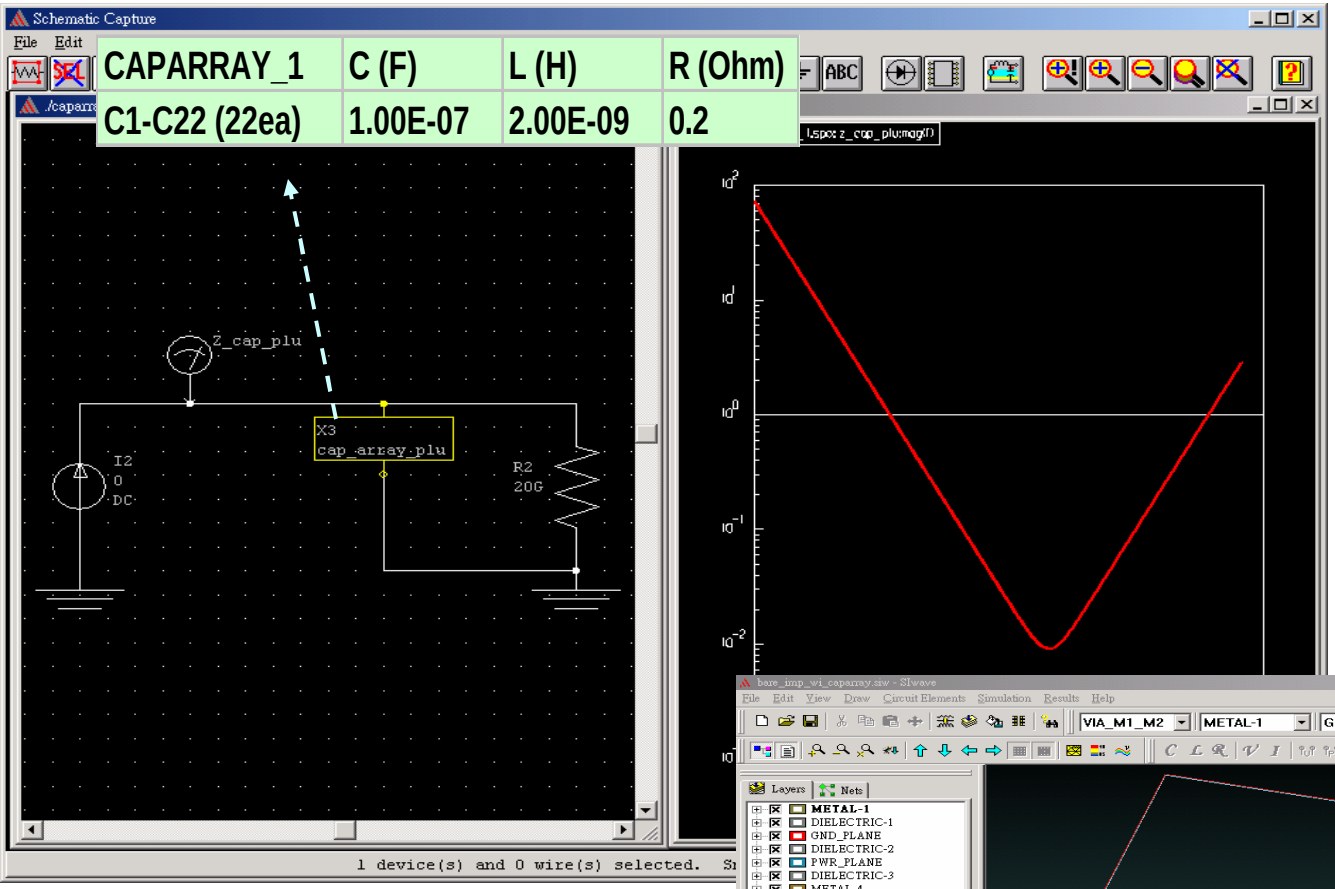
$\Delta I = 2A$

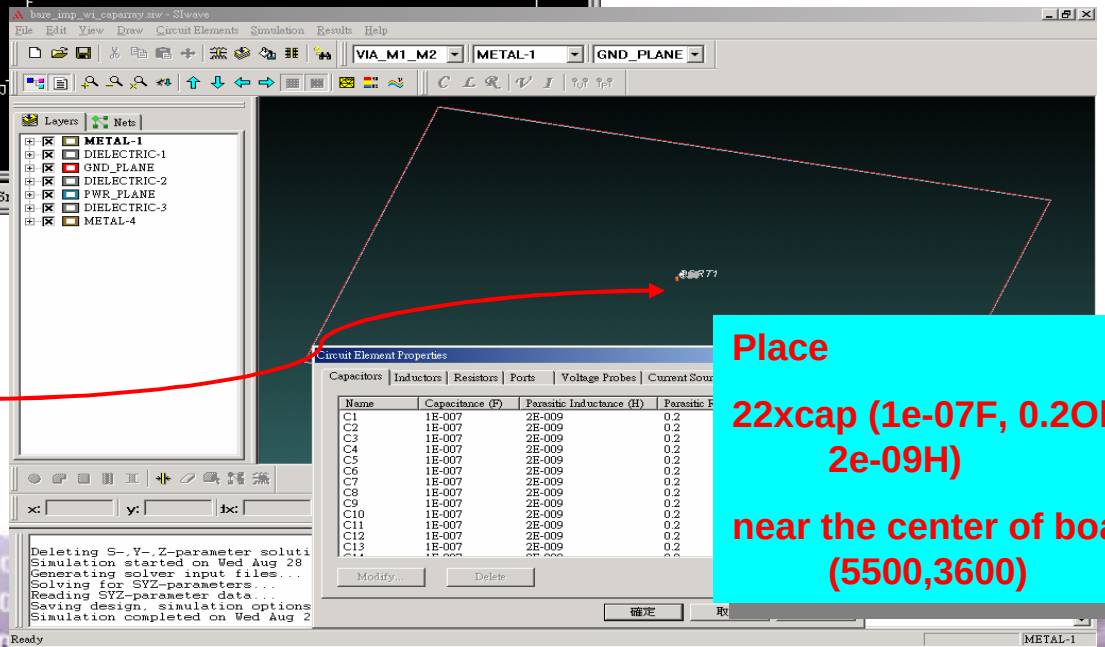
$\Delta V = 3.3 \times 0.05$

$f = 1MHz$

Caparray_1 and its Impedance

CAPARRAY_1	C (F)	L (H)	R (Ohm)
C1-C22 (22ea)	1.00E-07	2.00E-09	0.2





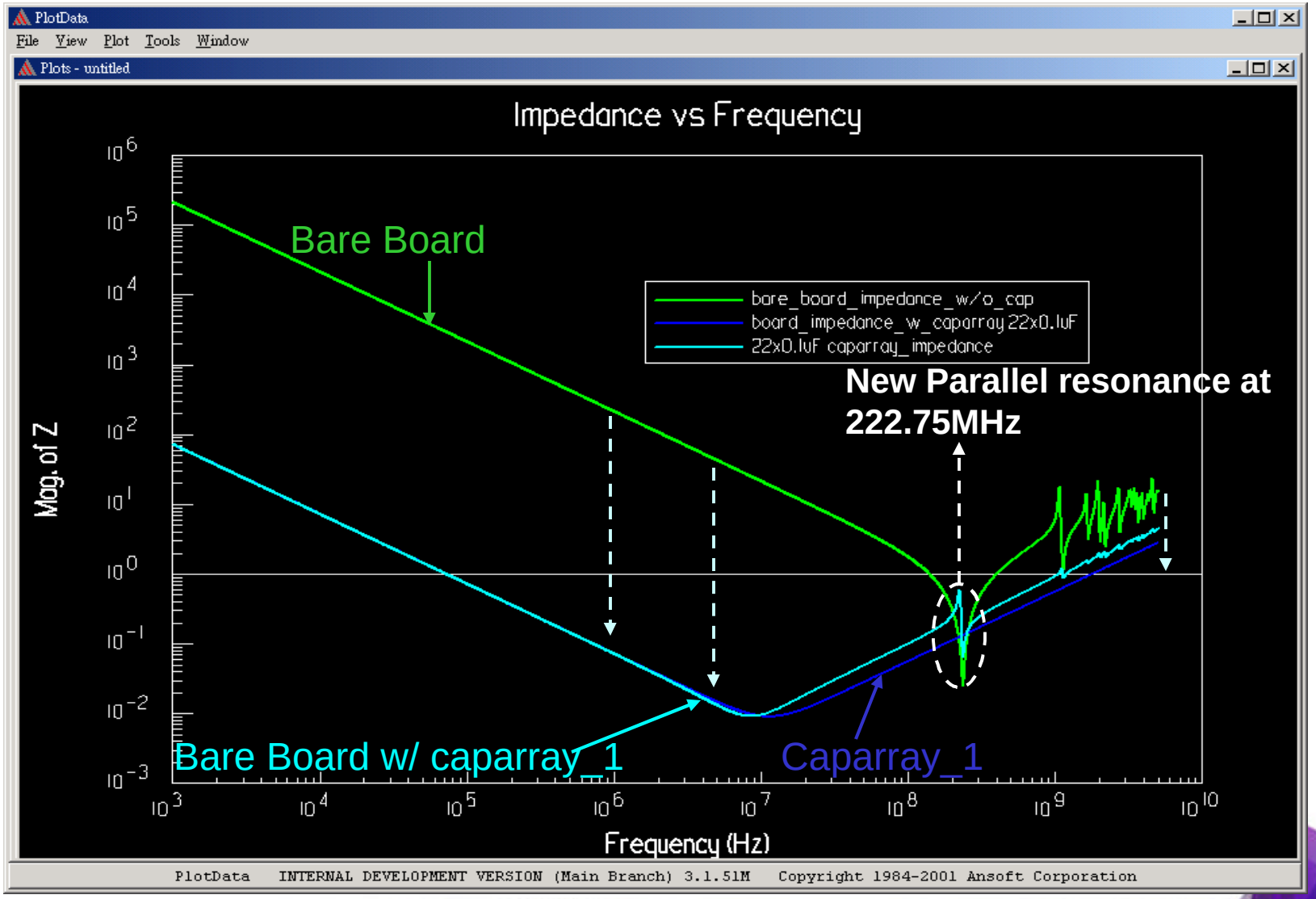
SIwave Simulation of Caparray_1 Effect on Bare board

Place

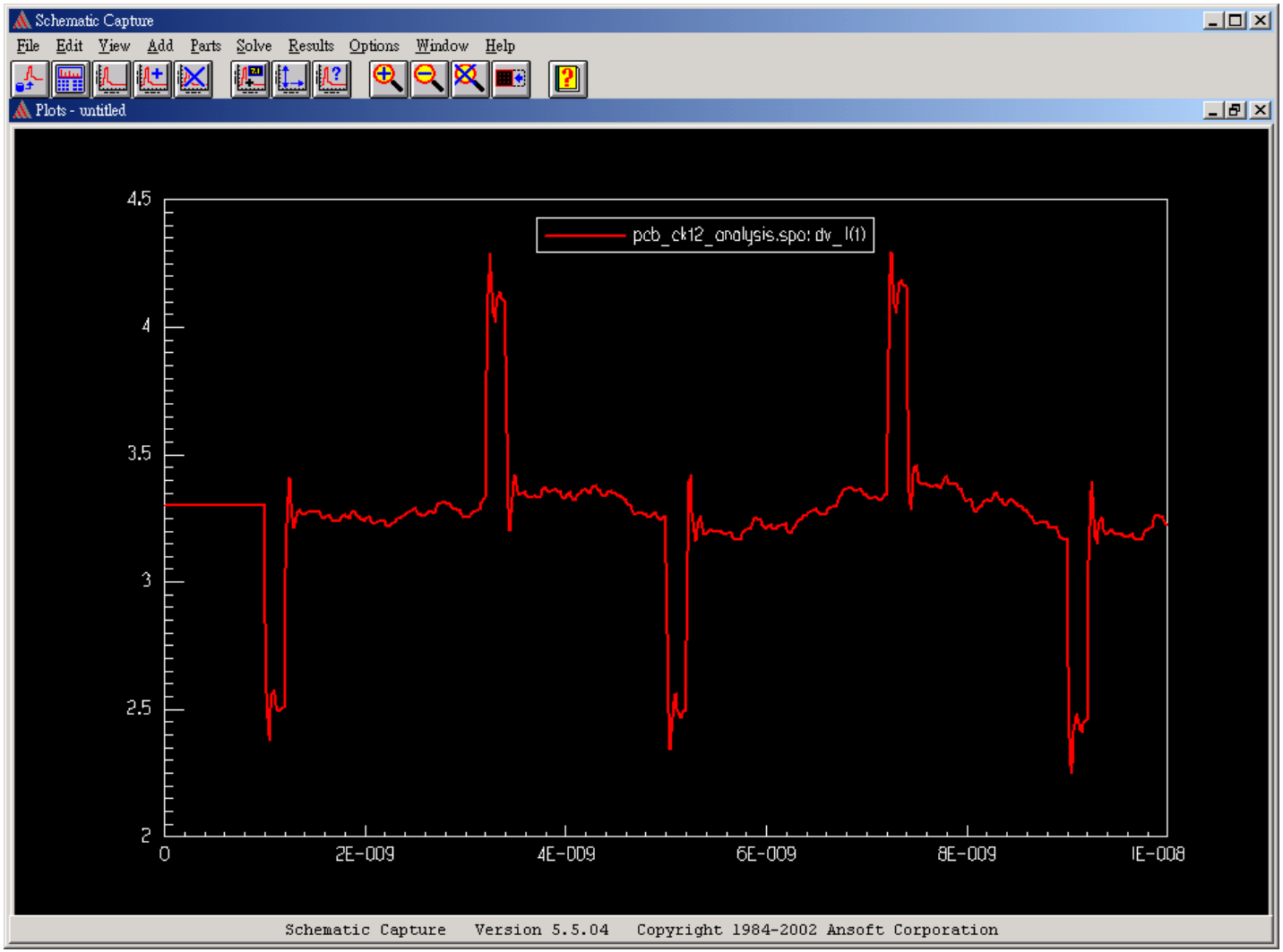
22xcap (1e-07F, 0.2Ohm, 2e-09H)

near the center of board (5500,3600)

Effect of Caparray_1 on Board Impedance



Time Domain Power/Ground Bounce Waveform w/ Caparray_1

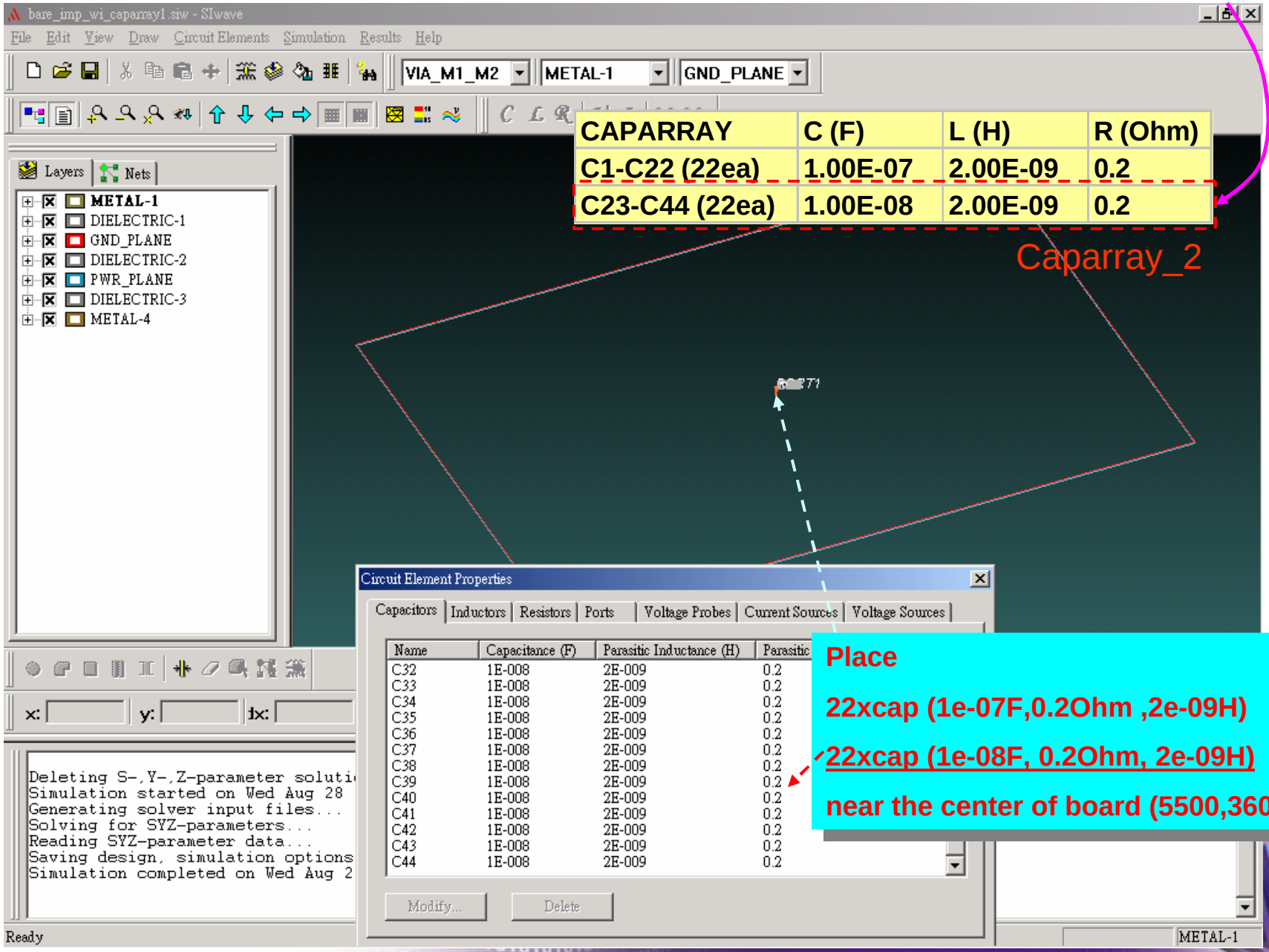


Power/Ground Bounce Waveform not within 5%(3.3V)!!! Need More Decaps

Add More Caps

Caparray_2

Add Caparray_1 and Caparray_2



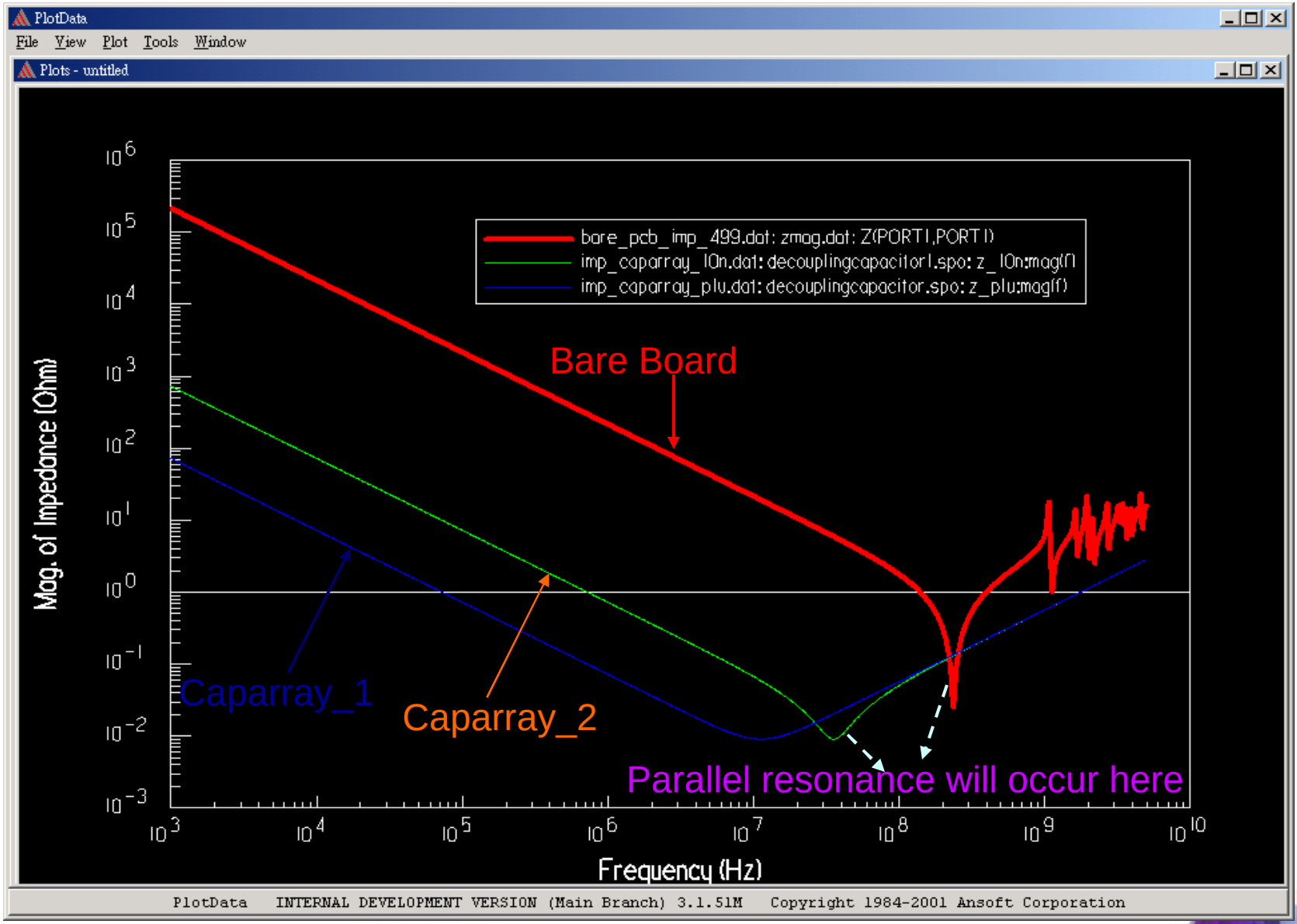
Place

22xcap (1e-07F,0.2Ohm ,2e-09H)

22xcap (1e-08F, 0.2Ohm, 2e-09H)

near the center of board (5500,3600)

Plane Impedance w/ Caparray_1 and Caparray_2



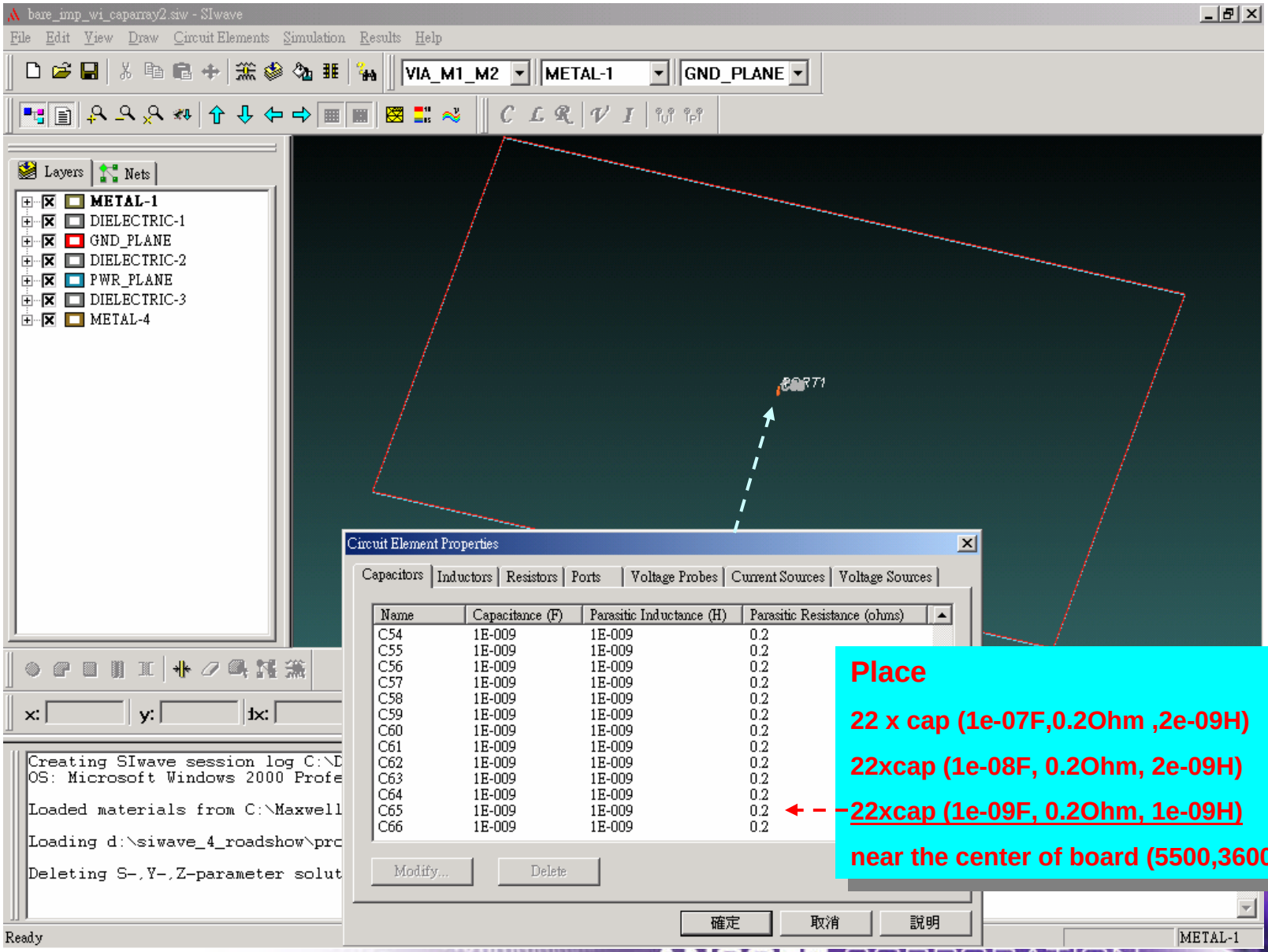
Time Domain Power/Ground Bounce Waveform w/ Caparray_1+_2

Ground Bounce has been improved a lot!!! But, still doesn't meet the design goal

Add more Caps

Caparray_3

Add Caparray_1+_2+_3



Place

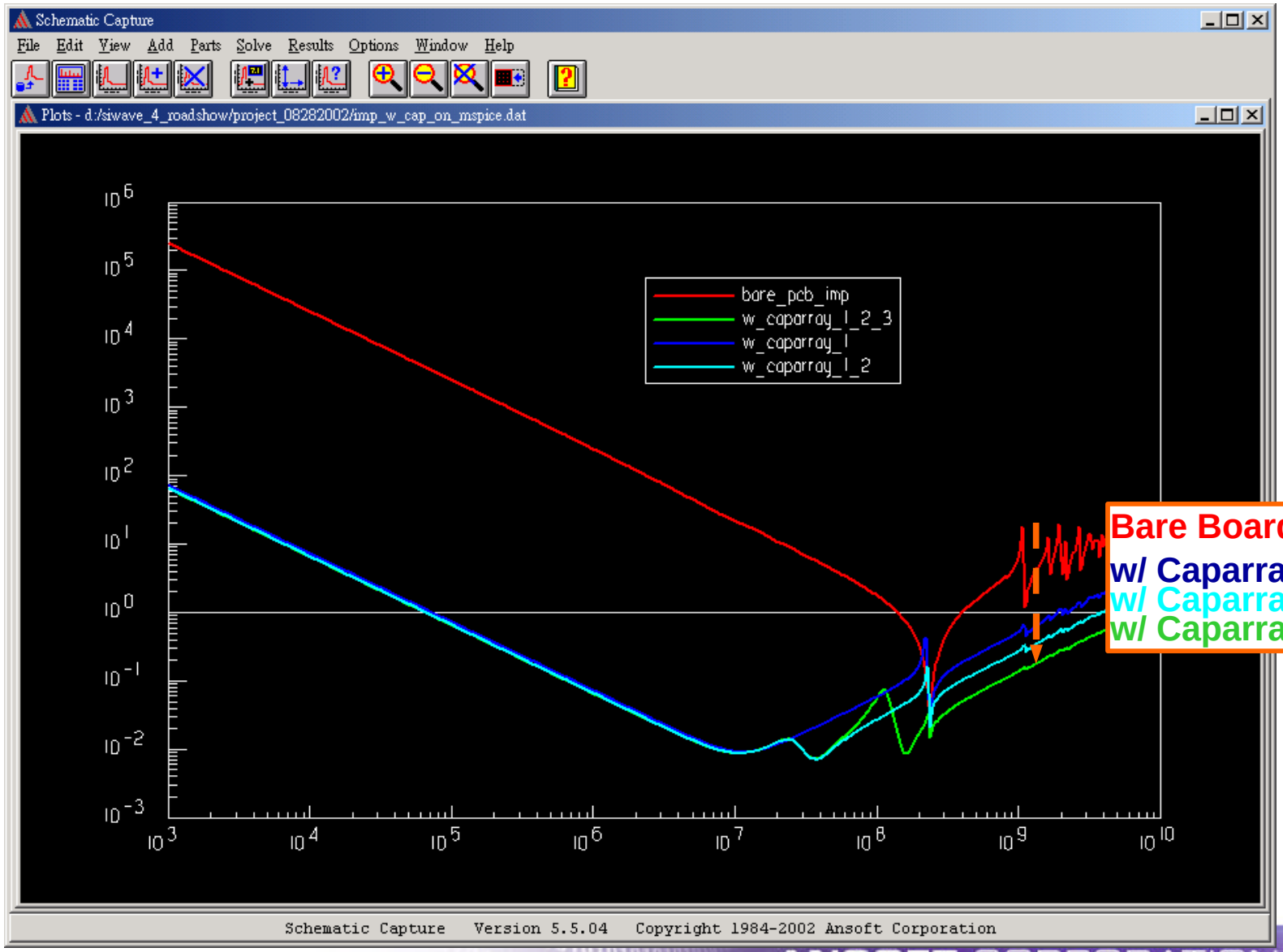
22 x cap (1e-07F,0.2Ohm ,2e-09H)

22xcap (1e-08F, 0.2Ohm, 2e-09H)

22xcap (1e-09F, 0.2Ohm, 1e-09H)

near the center of board (5500,3600)

Caparray_1 vs Caparray_1+_2 vs Caparray_1+_2+_3 Impedance



Bare Board

w/ Caparray_1

w/ Caparray_1+_2

w/ Caparray_1+_2+_3

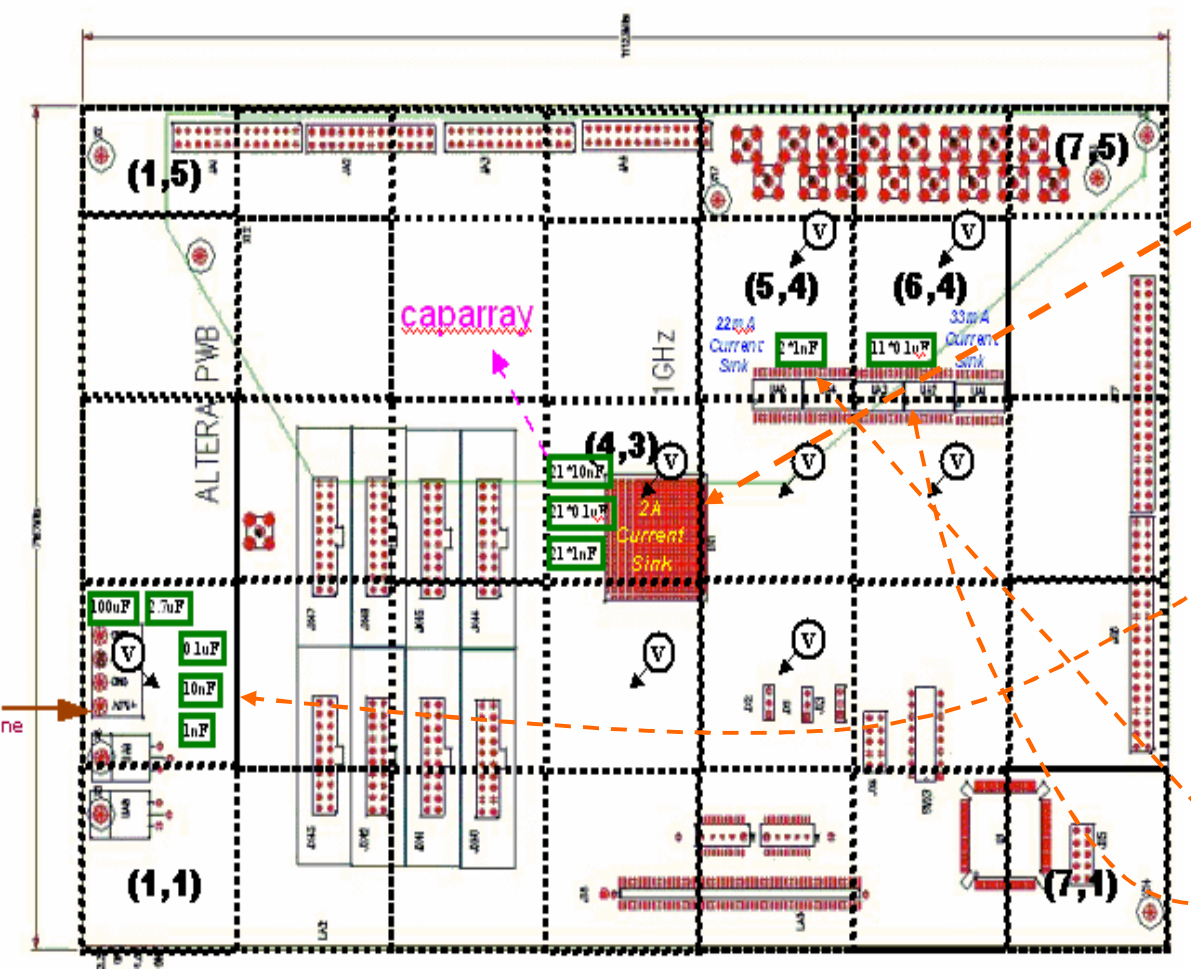
Time Domain Power/Ground Bounce Waveform w/ Caparray_1+_2+_3

Almost meets the design goal of Power Bounce.

Next Step

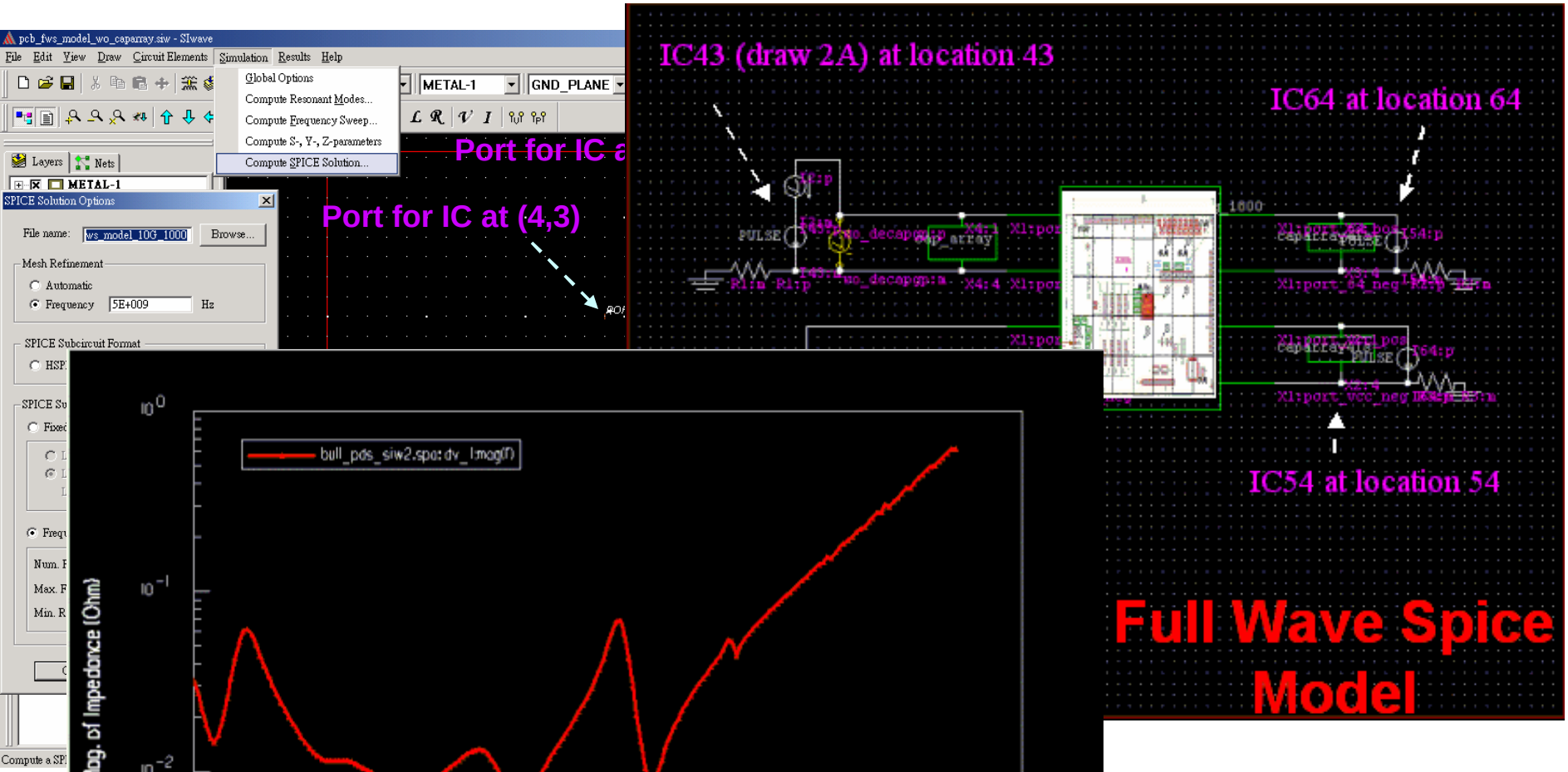
Export Entire Board's Full Wave Spice Model.

Positions of the Decoupling Capacitors and IC

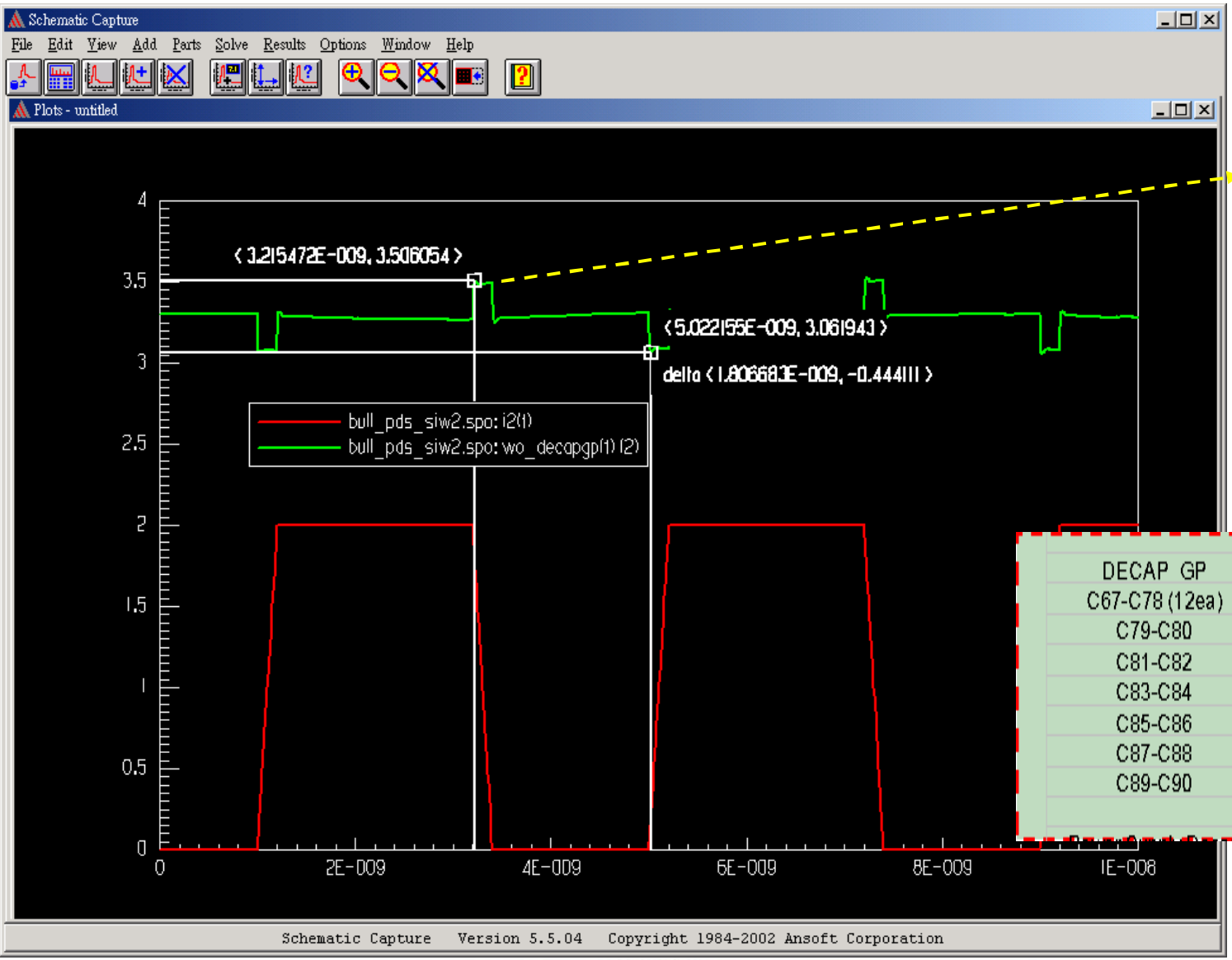


CAPARRAY	C (F)	L (H)	R (Ohm)
C1-C22 (22ea)	1.00E-07	2.00E-09	0.2
C23-C44 (22ea)	1.00E-08	2.00E-09	0.2
C45-C66 (22ea)	1.00E-09	1.00E-09	0.2
Power Supply Decap			
C91	1.00E-04	5.00E-09	0.01
C92	2.70E-06	5.00E-09	0.01
C93	1.00E-07	1.00E-09	0.01
C94	1.00E-08	1.00E-09	0.01
C95	1.00E-09	1.00E-09	0.01
Decap54 (7086.6,5511.8)			
C96-C102	1.00E-07	2.00E-09	0.2
Decap64 (8661.4,5511.8)			
C103-C109	1.00E-07	2.00E-09	0.2

Export Full-Wave Spice Model for PCB Plane



Current Sink and Power/Ground Bounce Voltage at IC(4,3)

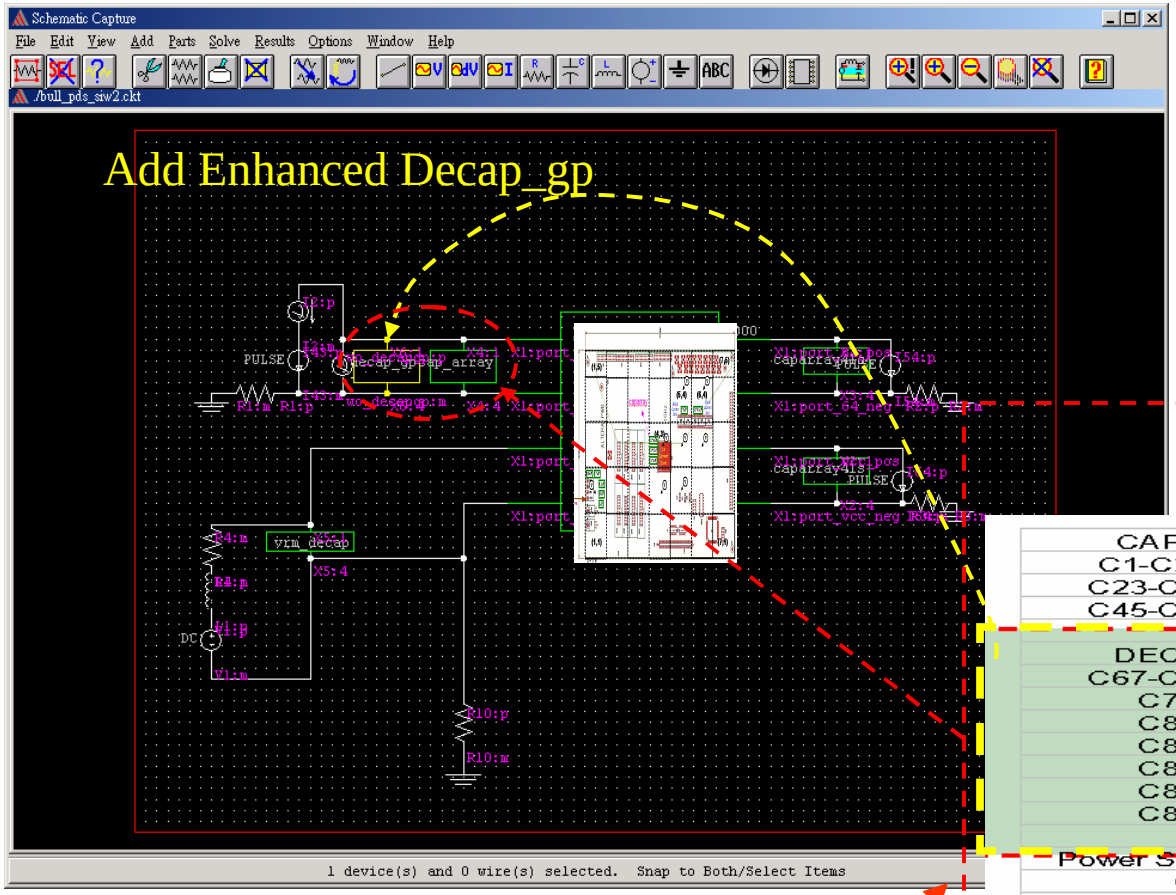


Slightly over spec. Need to add more decaps

Enhanced Decaps

DECAP GP			
C67-C78 (12ea)	1.00E-09	5.00E-10	0.2
C79-C80	2.50E-09	5.00E-10	0.2
C81-C82	5.00E-09	5.00E-10	0.2
C83-C84	1.00E-08	8.00E-10	0.2
C85-C86	2.50E-08	8.00E-10	0.2
C87-C88	5.00E-08	8.00E-10	0.2
C89-C90	1.00E-07	8.00E-10	0.2

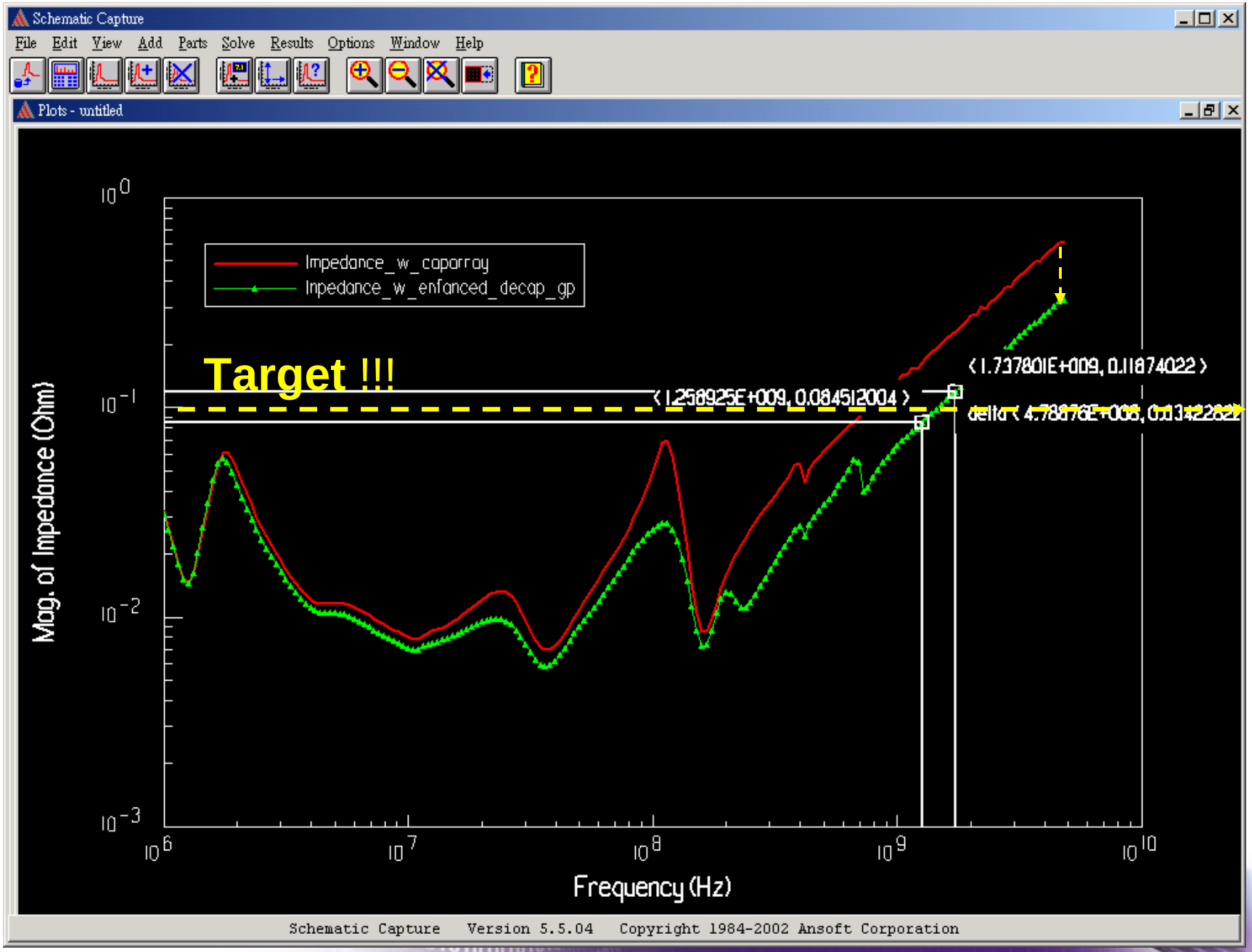
Schematic with Total Decaps



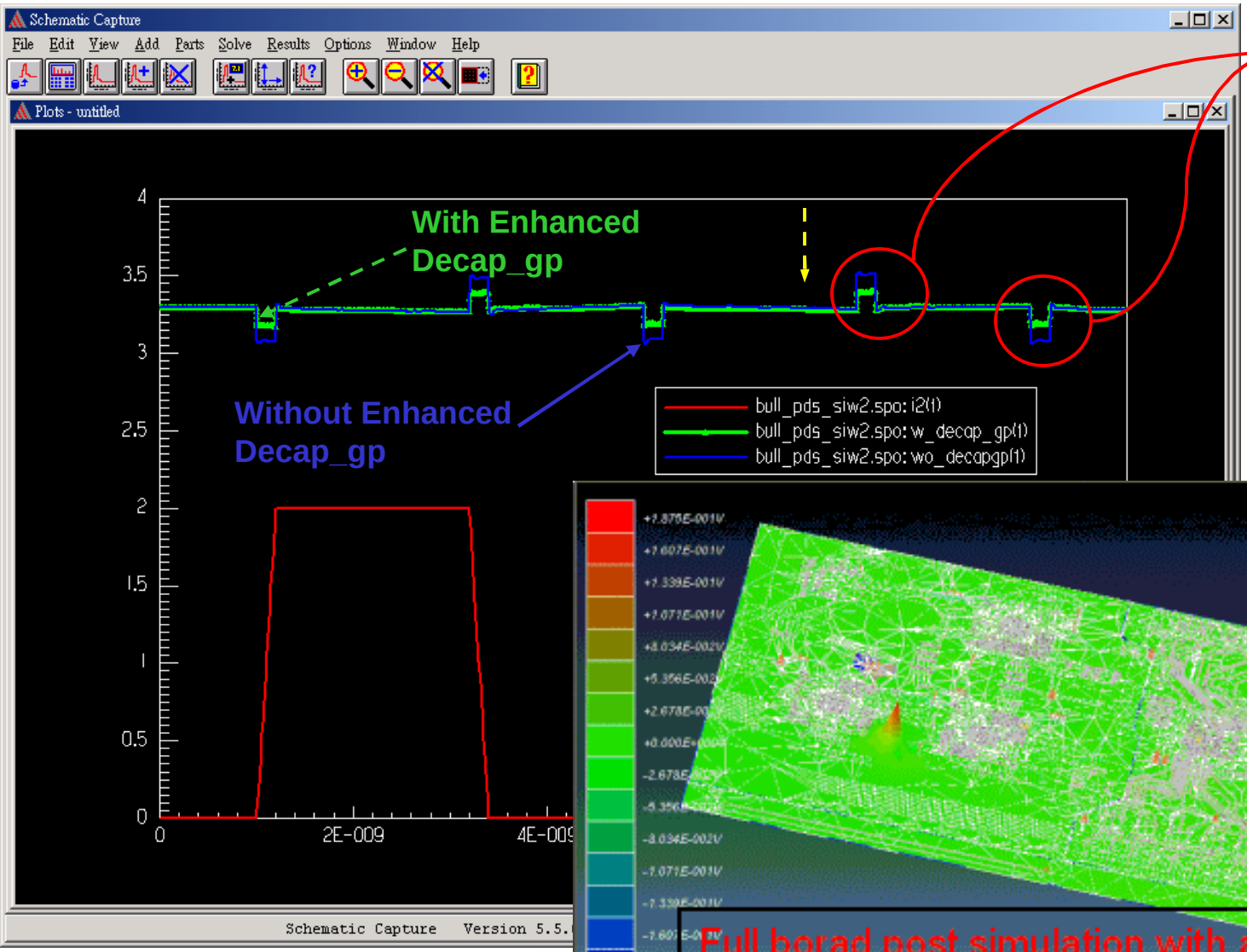
CAPARRAY	C (F)	L (H)	R (Ohm)
C1-C22 (22ea)	1.00E-07	2.00E-09	0.2
C23-C44 (22ea)	1.00E-08	2.00E-09	0.2
C45-C66 (22ea)	1.00E-09	1.00E-09	0.2
DECAP_GP			
C67-C78 (12ea)	1.00E-09	5.00E-10	0.2
C79-C80	2.50E-09	5.00E-10	0.2
C81-C82	5.00E-09	5.00E-10	0.2
C83-C84	1.00E-08	8.00E-10	0.2
C85-C86	2.50E-08	8.00E-10	0.2
C87-C88	5.00E-08	8.00E-10	0.2
C89-C90	1.00E-07	8.00E-10	0.2
Power Supply Decap			
C91	1.00E-04	5.00E-09	0.01
C92	2.70E-06	5.00E-09	0.01
C93	1.00E-07	1.00E-09	0.01
C94	1.00E-08	1.00E-09	0.01
C95	1.00E-09	1.00E-09	0.01
Decap54 (7086.6,5511.8)			
C96-C102	1.00E-07	2.00E-09	0.2
Decap64 (8661.4,5511.8)			
C103-C109	1.00E-07	2.00E-09	0.2

All Decaps to be added in this PCB
Decaparray_1+_2+_3+Enhanced Decap_gp

IC(4,3) Impedance Value w/wo Decap_gp



Current Sink and Power/Ground Bounce Voltage on IC(4,3)



Bingo!!!

We meet the PI design goal.

Power Integrity Design Flow using Full-Wave field solver (Ansoft Slwave)

STEP 1: Resonant modes

1.1 Pre-layout PDS's power/ground plane structures(Layer stack-up, Materials,Shapes) to make the inherent natural resonant modes (usually first) not occur with the target impedance required band-width or in the higher band.

1.2 Preview the voltage distribution of the resonant mode, avoid placing ICs which draw large currents near the resonant' voltage peaks/dips. The reason is when the source is closer to the peaks/dips it is easier to excite the resonant modes.

STEP 2: Frequency Sweep

2.1 Probe voltage

Replace the IC with current sources around their layout placement location, at the same time, put voltage probes on the desired locations to test that locations' voltage frequency response. In the voltage frequency response, the frequencies of voltage peaks will show which resonant mode has been excited.

2.2 Surface voltage

Based on the voltage peak frequencies, plot the surface voltage distribution on that frequency, place the required decoupling capacitor on the voltage peaks/dips location (how to place decoupling capacitors)

Power Integrity Design Flow using Full-Wave field solver (Ansoft Slwave) cont'd

STEP 3: S,Y,Z Parameters (include export Touchstone SNP file)

3.1 Compute/plot one port (IC location) Z parameter (usually log-log scale in Hz) From the Z frequency response, figure out the required "total capacitance, parasitic inductance and ESR" which should contributed by the physical capacitors (this will determine the required size of decoupling capacitors)

3.2 Use embedded Ansoft Full-Wave Spice to investigate the physical de-coupling capacitor effect (resonant, ESL and ESR, parallel skew etc.)

3.3 From the actual AC sweep response to select the required capacitors which should meet the total required "R/L/C value"

3.4 Place the capacitor on different locations to check the path inductance effect (this will determine the location of the de-coupling capacitors)

3.5 Use multi-ports Z parameter to check the trans-impedance

3.6 Use multi-ports S-parameters to investigate the signal transmission and coupling

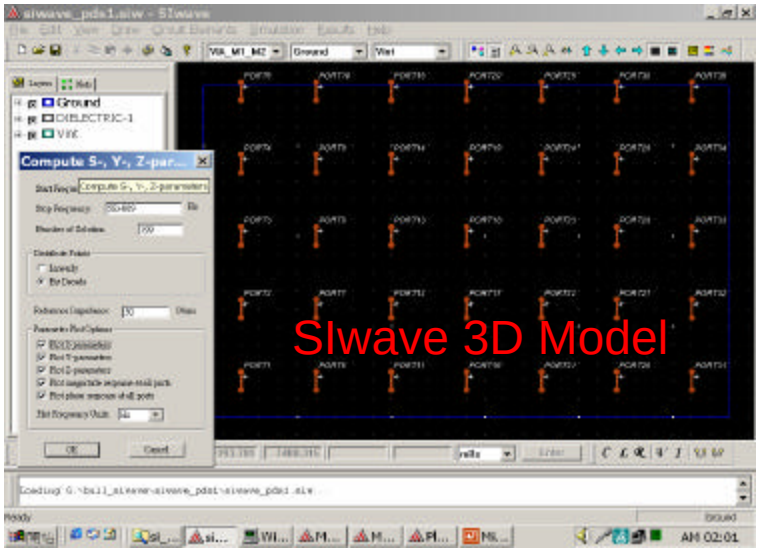
STEP 4: export Full-Wave Spice model and Spice simulation

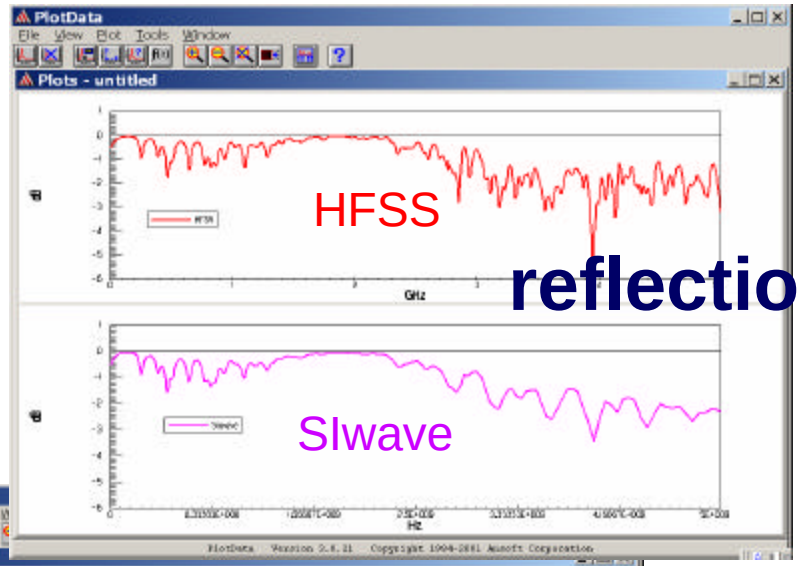
Use Spice (e.g. Ansoft Full-Wave Spice) to simulate the supply voltage fluctuation, simultaneously switching noise in time domain

Examples Involving Measured Data

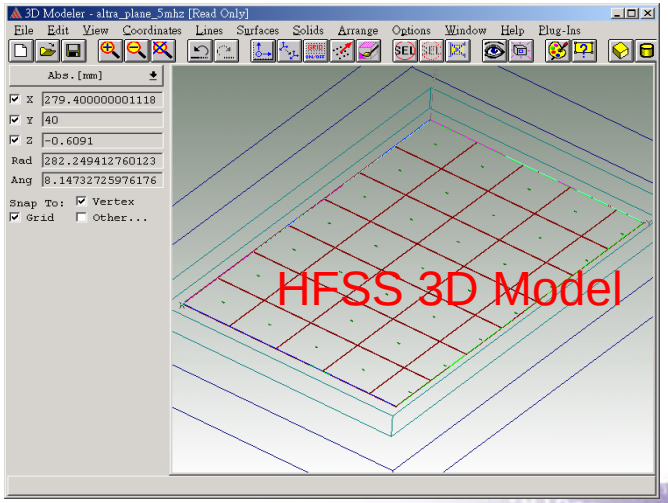
With Comparisons to SIwave

HFSS vs. SIwave simulation



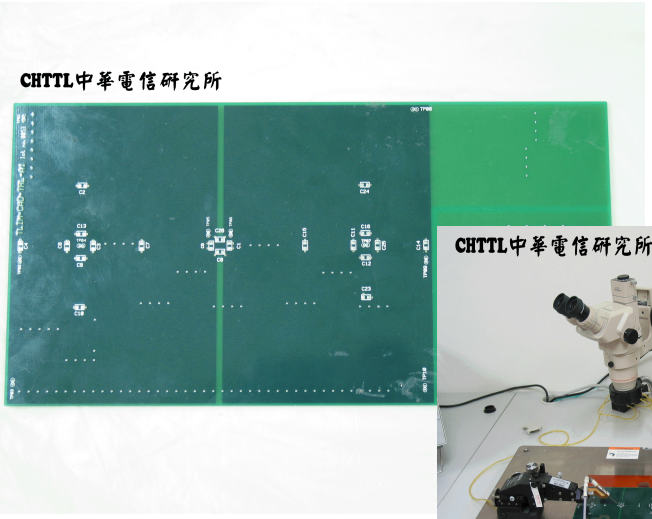


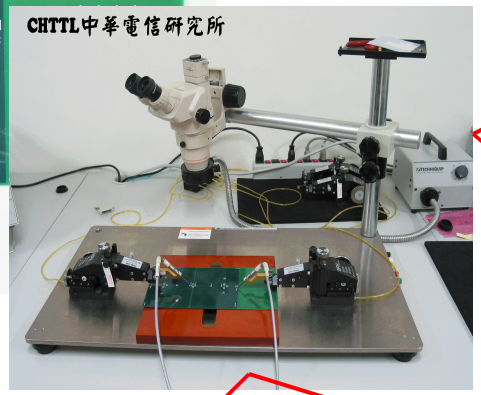
reflection

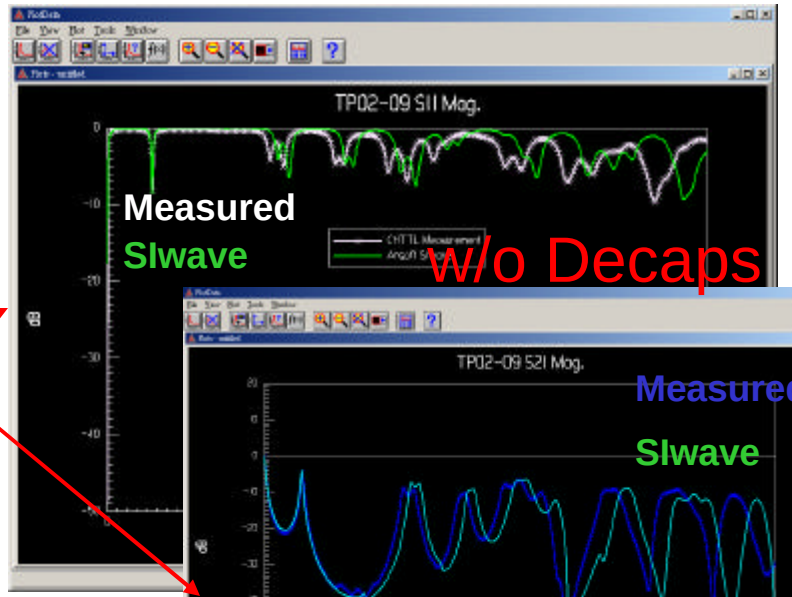


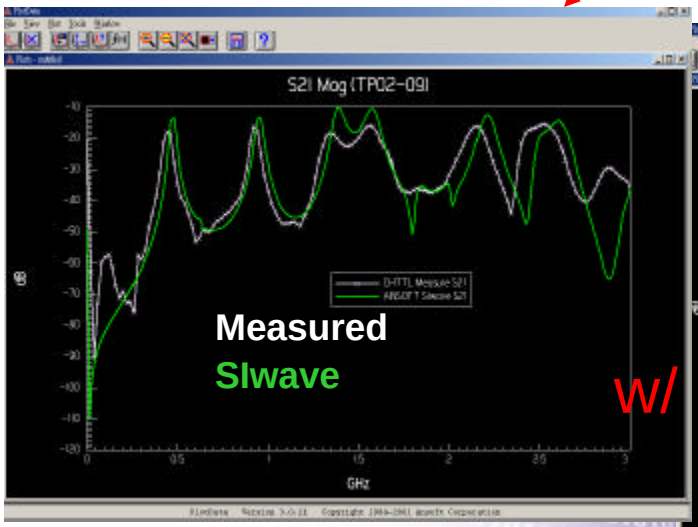
transmission

CHTTL Test Board for Mixed-Signal Design with a Split Power Plane

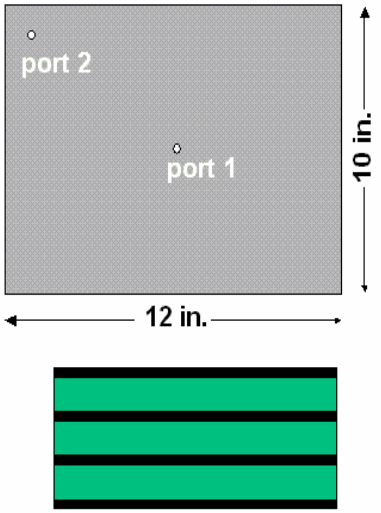




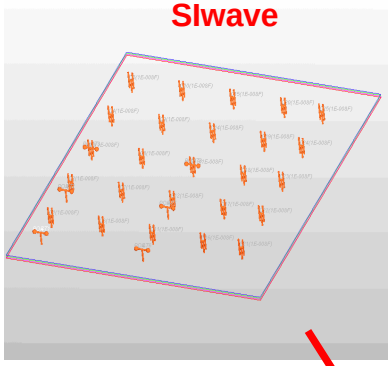


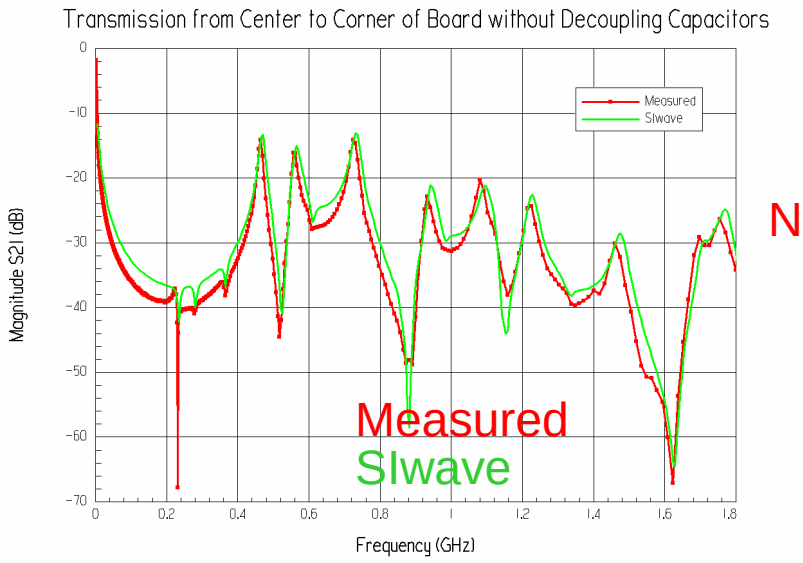


Four Layer PCB Power Integrity



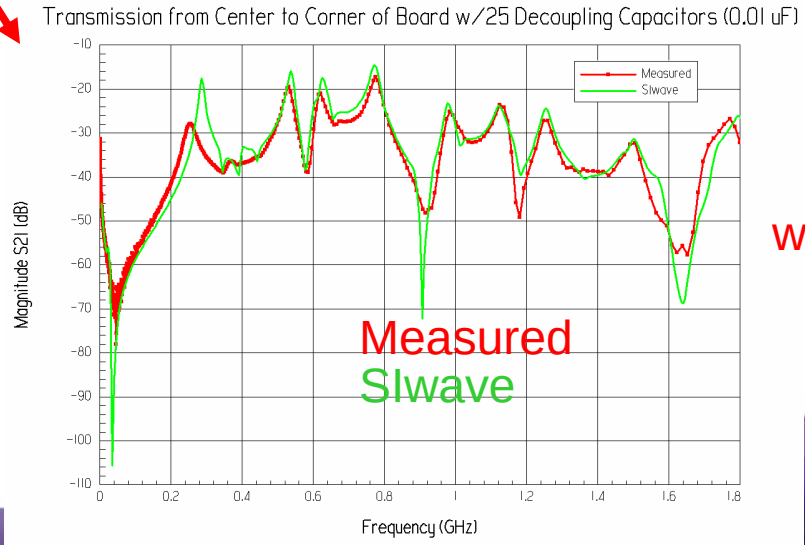
Setup for 25 Decaps in SIwave





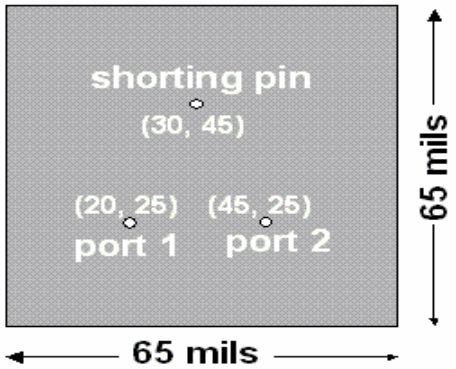
No Caps

- **Examine S21 for board with and without Decoupling Capacitors**
- **Compare Measurement data to SIwave data**
- **Four 0.000138” copper layers**
- **Three 0.04” FR-4 layers**
- **Ports and Capacitors between layers 2 and 4**



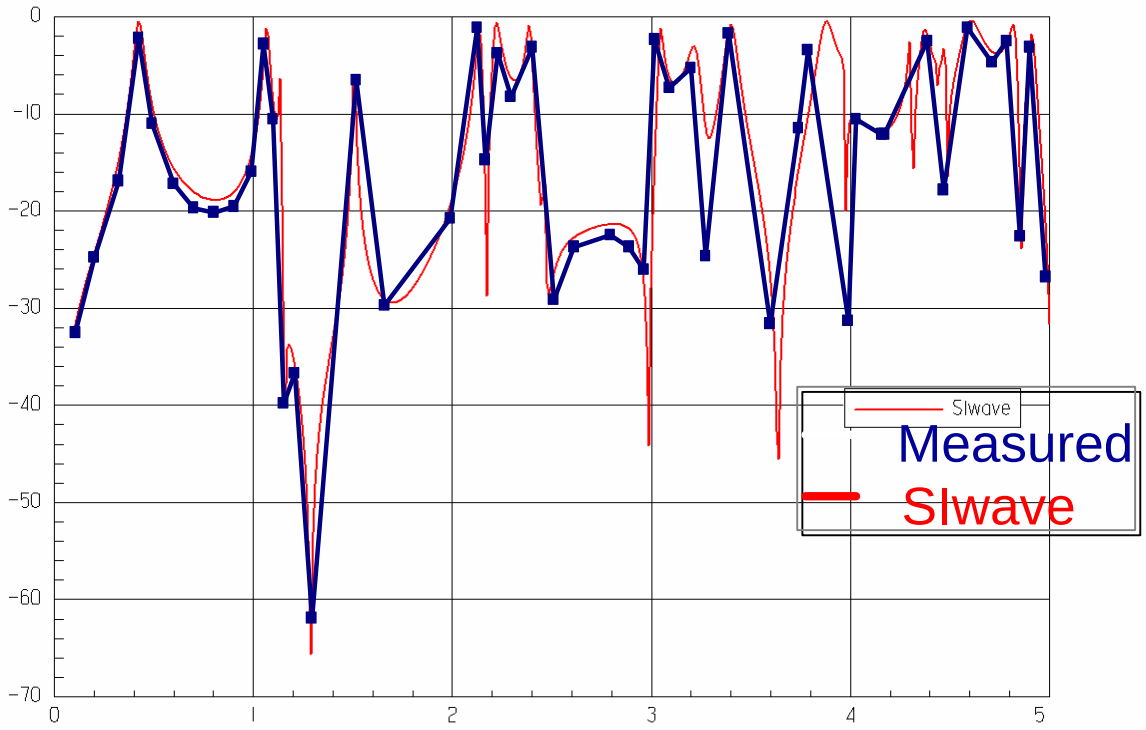
w/ Caps

DC Power Bus

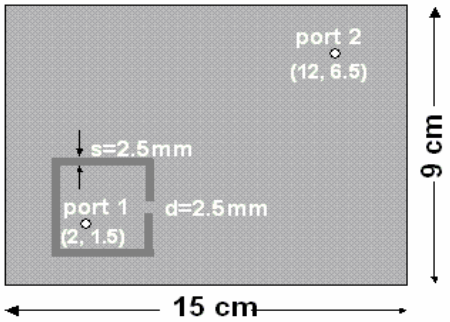


- Examine S21 for board with a shorting pin
- Compare Measurement data to Slwave data

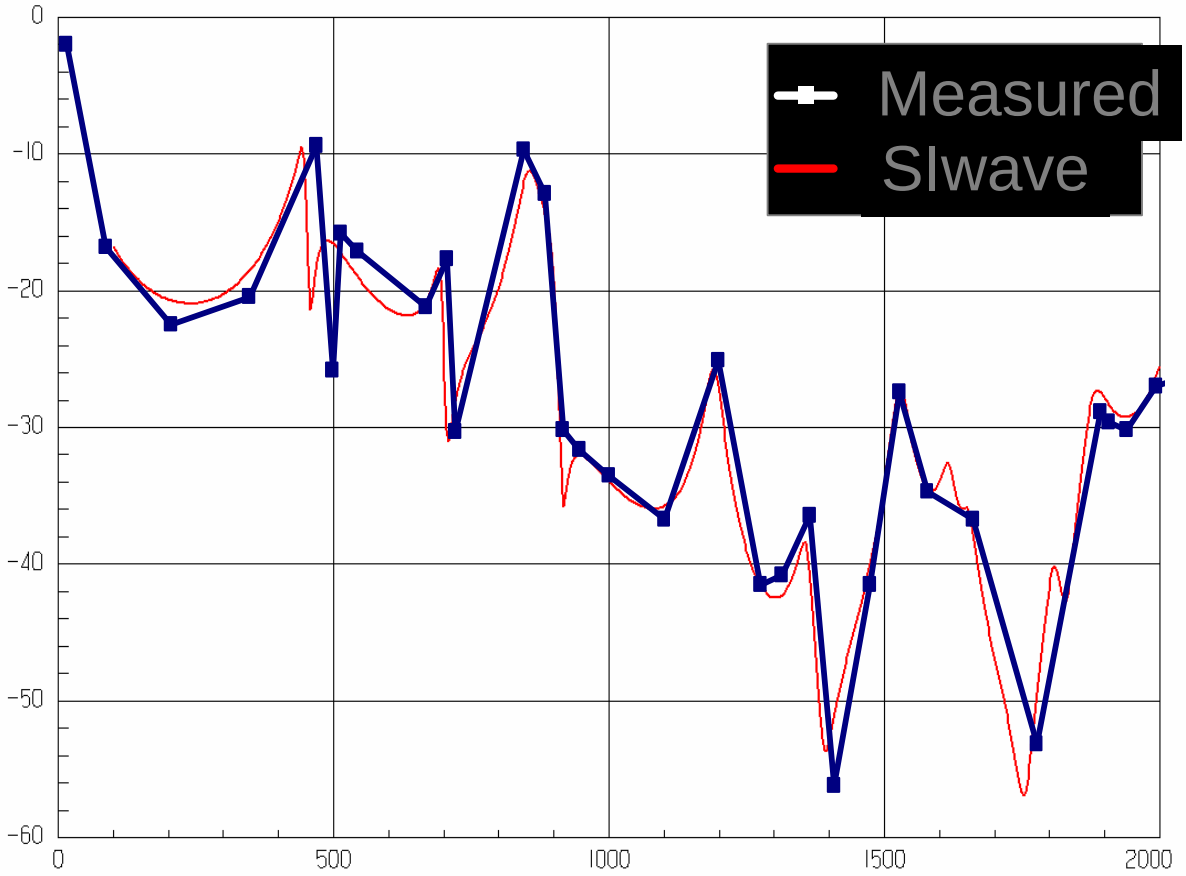
- Two copper layers
- One 44 mil FR-4 layer
- Ports and Capacitors between layers 2 and 4



Power Island with PEC Bridge



- **Examine S21 for board with a square (3x3cm) power island**
- **Compare Measurement data to SIwave data**
- **Two copper layers**
- **One 45 mil FR-4 layer**



Conclusions

- The PI Flow to make the impedance of the PDS meet the target impedance using Ansoft SIWave has been shown.
- This Flow can be used in post layout analysis to get the optimum decoupling capacitors and save money.
- Meeting the PI target will help reduce the SSN and SI Issues.
- The approach of Lumped and T-cell is no longer valid due to the wave effect dominance on higher-speed.
- Ansoft SIwave uses Full-Wave EM Technology to account for the wave effect on PDS and to meet the future high speed requirement.
- SIwave simulation agrees with HFSS/Measurement .
- SIwave provides a fast and easy design/analysis flow to meet Power Integrity and to prevent under/over design condition.