Design Solutions in Foundry Environment

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1. Introduction
2. Custom design flows overview
3. Foundry design access
4. Foundry design solutions:
   - Standard cells
   - IO
   - Technology files and PDK
   - Memory
   - IP initiatives
5. New world of custom IC products
6. Summary
Access to foundry leading edge processes has become a common practice for fabless companies and IDMs looking to leverage their capacity.

Foundries do not offer a process solution alone, but the complete product, consisting of:

1. Process with multiple variants.
2. Design access.
3. Turn key services (i.e. test, assembly, drop ship, etc.)

The use of design solutions through foundries is increasing:

- 25% of 0.25 um tapeouts at the leading foundry use provided libraries.
- 60% of 0.18 um tapeouts at the leading foundry use provided libraries.
- 85% of 0.13 um tapeouts at the leading foundry use provided libraries.
Foundry Design Access Model

- GDS II Tapeout
- Physical Implementation (Back-end Design)
- Functional Implementation (Front-end Design)
- Product Conceptualization (Architecture Design)
- Customer

- Foundry Process Specs
- Design Kits & Verification Tools Support
- STD Libraries
- Analog IPs

- Partner
- Foundry
- Customer

- Mask Tooling

- Verified in Silicon
- Foundry Technology

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Generic Custom Digital Design Flow

Front End Library
Verilog, Synopsys, Floorplan Abstract, Trial P&R Abstract

Functional Implementation → Synthesis

Timing Analysis

Floor Plan

Place & Route → Extraction → DRC/LVS

Back End Library GDSII, LVS Netlist

Front End Flow
Back End Flow
Modern challenges in advanced semiconductor product designs can be divided into three broad areas:

1. Challenges in traditional design hierarchy (such as logic design, layout design) due to increased product functionality and SoC integration.
   => New EDA tools, technique, and methodology. (This is expected to lead to further consolidation among EDA and design IP vendors).

2. Challenges related to shrinking technology: new materials, exponentially increasing leakages currents, increasingly complex interconnect structures, design related yield loss.
   => The merger of design and manufacturing process development
   => Further development of Design For Yield (DFY).

3. Challenges related to IP acquisition and management; mass production know-how.
   => New emerging IP industry.
   => Technology research and manufacturing “constellations” (between major foundries and IDMs)
Access to Complete Design Solutions

Various design solutions are available through foundries

Design Tools

Library Solution

IP Solution

Design Service

Turnkey

- cadence
- SYNOPSYS
- simplex
- Mentor Graphics
- Artisan Components
- VIRAGE Logic
- Agilent Technologies

- synopsys
- UNIVERSE
- ARM
- MoSys
- eSilicon
- IC Design

- Siemens
- Fujitsu
- MIPS Technologies Inc
- GDA Technologies
- Flextronics
Design Solutions: Foundry Pyramid

- **SYSTEM IP ACCESS**
  - ARM Cores
  - MIPS Cores
  - USB
  - SSTL
  - LVDS
  - VCX Program

- **BASELINE DESIGN ACCESS**
  - Low Power Library
  - High Performance
  - Derivative Vt Libraries
  - PDK
  - Std Cells & Baseline I/O’s
  - Memory Compilers
  - 1T-SRAM

- **PLUG-IN PROCESSES**
  - RFCMOS Module
  - Analog Module
  - SRAM Module

- **BASELINE PROCESSES**
  - Process Design Rules
  - Silicon SPICE & Interconnect Models
  - Reference Bit-cells
  - ESD Reference Structures

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Due to complexity of the problem and long term design engagements, serious considerations have to be given to access design solutions from a foundry.

Next we will examine some of the major aspects of design IP access which needs to be analyzed and reviewed prior to foundry engagement.
1. Key points to consider in EDA IP offerings from foundry:

- Foundry’s EDA partner selection
- IP suitability for current and future design projects
- Schedule of IP availability
- Cost model of EDA IP access (cost of acquisition, NRE and royalty structure)
- Portability of library and IP solution (open model vs. captive model)
- IP deliverables to customer
- IP selection: libraries for process variants, special digital IP blocks (i.e. IOs, ARM, etc.), analog IP.
2. EDA IP verification and characterization methodology:

- Foundry methodology to validate EDA libraries, compilers, etc.
  - resources: expertise and tools
  - silicon verified vs silicon hardened

- Process/SPICE changes:
  - approval of changes in regards to EDA IP
  - EDA IP characterization: time, schedule (before the changes or after)
  - foundry’s flexibility for existing and on-going designs
3. Design support from foundry:

- Local expertise in different IP

- Foundry resources:
  - engineers vs project managers
  - design tools used at foundry

- Foundry support model

- Design services
4. IP Tapeout support:

- Procedures for “black box” models (i.e. ARM)
- IP tagging for royalty payments (i.e. specialized vs industry standard VSIA)

**Conclusion:**
Selection of design IP from foundry makes a significant difference in the long term success of foundry engagement. The key elements discussed above need to be considered.
Foundry Design Solutions

- Libraries
- Technology Files and PDK
- Memory
- IP Initiatives
EDA library design solutions provided by major foundries usually consist of:

1. Standard Cell Libraries;
2. IO libraries;
3. Memory compilers and embedded special memories such as embedded 1T SRAM, E\textsuperscript{2}PROM, OTPROM, etc.

Each part of library solution has its unique challenges and requires special considerations.
Standard Cell Libraries: Architecture

- Cell height optimized for each process technology, driven by
  - Back-end process
  - Transistor performance (i.e. $I_{\text{Dsat}}$, $I_{\text{OFF}}$, $V_t$, $G_m$, etc.)
- Cell height is consistent across a library, however a library can have double height cells.
- Cell dimensions are reported in terms of routing grids or tracks
  i.e. two-input NAND gate is typically 3 tracks wide and 8-10 tracks tall depending on the technology
- Cells are designed to share power & ground rails - “Flip and Abut”
- Input/Output pins can be staggered to improve router effectiveness.
- Cells designed to be “Tiled” together.
Standard cell libraries from major IP providers typically include:

• **Front End Views**
  – Behavioral models
  – Simulation timing models:
    – Cadence NC-Verilog, NC-VHDL, Verilog-XL
    – Synopsys synthesis models
    – Design Compiler, Module Compiler, Physical Compiler,
    – Power Compiler
    – Synopsys PrimeTime Static Timing Models
  – Floorplan abstract

• **Back End Views**
  – Abstract Files for Place & Route Tools
  – CDL Netlists for LVS Verification
  – Physical (Layout) Files for Streaming Out GDSII Database

• **Documentation:** data-books, application notes
Key parameters of IO libraries:

- **Pad Structure:**
  - In-line pads for core limited designs: wide and short
  - Staggered pads for pad limited designs: narrow and tall

- **IO cell height**

- **Pad pitch and pad opening**
  - must be designed to meet particular assembly capabilities

- **Separate I/O power rail**
  - Accommodate I/O drive voltage requirement
  - Isolate “Noisy” I/O power from core power

- **Simultaneous Switching Outputs - SSO**
  - Guideline for the number of power pin pair requirements
## Open Model Library Access

<table>
<thead>
<tr>
<th>Partners</th>
<th>0.35μm</th>
<th>0.25μm</th>
<th>0.18μm</th>
<th>0.13μm</th>
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<td>IO Pad Library</td>
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<td>Memory Compilers</td>
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<td>(SPSRAM, 2P Regfile)</td>
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Source: Chartered Semiconductor Manufacturing web site (http://www.charteredsemi.com/design/library_support.asp)
# 0.13µm Library Offerings

## Components

<table>
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<tr>
<th>Partner</th>
<th>Synopsis (Vista)</th>
<th>Artisan</th>
<th>Virage Logic</th>
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<tbody>
<tr>
<td>Standard Cell Library</td>
<td>SAGE-X Standard Cell Library</td>
<td>Sync Single Port SRAM Compiler</td>
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<tr>
<td>In-line I/O Library 3.3/2.5V</td>
<td>In-Line I/O Library 3.3V</td>
<td>Sync Dual Port SRAM Compiler</td>
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<tr>
<td>Staggered I/O Library 3.3/2.5V</td>
<td>Staggered I/O Library 3.3V</td>
<td>2 Port Register File Compiler</td>
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<tr>
<td>Sync Single Port SRAM Compiler</td>
<td>Sync Single Port SRAM Compiler</td>
<td>1 Port Register File Compiler</td>
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<tr>
<td>Sync Dual Port SRAM Compiler</td>
<td>Sync Dual Port SRAM Compiler</td>
<td>Sync ROM Compiler</td>
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<tr>
<td>Async 2 Port SRAM Compiler</td>
<td>2 Port Register File Compiler</td>
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<tr>
<td>Sync ROM Compiler</td>
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## Design Kits

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<td>Q203</td>
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Source: Chartered Semiconductor Manufacturing web site (http://www.charteredsemi.com/design/library_support.asp)
Design Solutions

- Libraries
- Technology Files and PDK
- Memory
- IP Initiatives
A PDK is a complete set of building blocks, generated from foundry’s technology files, that enables customers to create a custom IC design. PDK is most commonly implemented in Cadence design environment format. It must be aligned and verified with foundry’s process technology.

PDK is the equivalent of a Standard Cell Library for digital design, providing an ‘off the shelf’, easy to install design environment tuned to a specific process technology.
EDA support form foundries covers all major aspect of the design flow and all major EDA tools.

Consistent with foundry technologies capabilities

Customers are able to design, simulate, layout, extract, verify & tape-out from transistor level upwards.

Source: Chartered Semiconductor Manufacturing web site (http://www.charteredsemi.com/design/pdks.asp)
Panelists cite shortcomings of process design kits
By Ron Wilson, EE Times, Mar 23, 2004  (http://www.eedesign.com/showArticle.jhtml?articleID=18401470)

Key points:
• Change of process may not be reflected in PDK.

• With the growing complexity and rate of change in processes, IP vendors will be unable to keep their IP current with the process... "It's very likely that the IP you use will have been developed with a different PDK from the one you are using. That will be trouble." - Dan Hillman, VP Virtual Silicon

• PDK revision control.
EDA Library: Memories

Memory Compilers -- Software Packages to build User Defined Memory Blocks

Type of memory compilers typically offered as part of foundry EDA library:

- **Single Port Sync SRAM**
  - 6 Transistor bit cell architecture
  - Read/Write from a single port

- **Dual Port Sync SRAM**
  - 8 Transistor bit cell architecture
  - Two fully independent read/write ports, each with its own clock

- **2 Port SRAM**
  - 8 Transistor Bit Cell Architecture Most Common
  - One port used for read, one port used for write

- **ROM**
  - Diffusion (smaller)
  - Via ROM (more flexible)

- **Register File** – alternative to embedded SRAM
  - Single port and Dual port
Compiled SRAM: Example

Typical Compiled embedded SRAM Architecture

A lot of memory “overhead” is part of generated SRAM. Compiled register file may be a good alternative to small SRAM.
Available Foundry IP Initiatives

Foundry

ARM
MIPS
MoSys
UNIVE
FUJITSU

and many many others …
Benefits for Customers

Foundry supported IP alliances program allows:

- Compare and select from various third-party IP solutions
- Silicon hardened and proven at various foundries
- IP is listed against industry standard specifications, e.g. VSIA (Virtual Socket Integration Assoc.)
- IP provider states level of validation and specific silicon processes in which it has been hardened
- Customers have access to more silicon hardened IP, reducing risk and exposure
- IP flexibility and ownership are understood prior to engagement
New Economical Realities for Custom IC
Cost of new ASIC designs increase with every technology generation:

Average design cost: EDA/COT tools, design engineering, mask set, prototyping, test.
The business dynamics of custom IC products changed:

**ASIC ≠ LOW COST**

Market response:
- High volume ASIC applications (i.e. consumer electronics)
- High performance ASIC applications (at premium cost)
- ASSP
- New technologies such as FPGA core with standard cell ASIC:
  for example, from IBM/Xilinx, reconfigurable ASIC core from LSI, etc.
The gap between ASIC and ASSP is projected to widen.

Custom IC Device market forecast (in $B)
(all categories)

Year	ASIC	ASSP
2002	19.8	28.1
2003	22.5	32.5
2004	26.8	40.1
2005	29.9	46.3
2006	31.2	49.1

43% TAM growth over 4 years
35% TAM growth over 4 years

Source: Gartner Research Semiconductor Forecast, 2003
ASIC and ASSP Growth Areas

Growth areas for ASIC and ASSP in communication sector

ASIC Growth Areas

- Communications Electronics: Other LAN (ASIC)
- Communications Electronics: Routers - Enterprise (ASIC)
- Communications Electronics: LAN Switches (ASIC)
- Data Processing Electronics: Storage Network Infrastructure (ASIC)
- Communications Electronics: SONET/SDH (ASIC)
- Communications Electronics: Routers - Service Provider (ASIC)
- Communications Electronics: Enterprise WAN (ASIC)

ASSP Growth Areas

- Communications Electronics: Other LAN (ASSP)
- Communications Electronics: Routers - Enterprise (ASSP)
- Communications Electronics: LAN Switches (ASSP)
- Communications Electronics: SONET/SDH (ASSP)
- Data Processing Electronics: Storage Network Infrastructure (ASSP)
- Communications Electronics: Enterprise WAN (ASSP)

ASIC top 3 growth areas:
- LAN (switches and access)
- Enterprise routers
- Storage network infrastructure
TAM = $1.4 billion in 2003
TAM = $2.8 billion in 2005

ASSP top 3 growth areas:
- LAN (switches and access)
- Enterprise routers
- SONET/SDH
TAM = $2.1 billion in 2003
TAM = $4.2 billion in 2005

Source: Gartner Research Semiconductor Forecast, 2002
Summary

- Foundries offer complete design access in addition to process, tech files, and libraries.
- Foundries are becoming active participants in design process.
- Foundries EDA IP engagements need to be carefully evaluated against current and future design needs.
- Design IP access model needs to be taken into considerations for a long term foundry engagement.
- Cost of custom designs is increasing rapidly for more advanced technologies. First time TO success is crucial for success => extensive and accurate simulation, virtual prototyping, design for yield.