A 90nm Variable Frequency Clock System for a Power-Managed Itanium® Architecture Processor

Tim Fischer, Ferd Anderson, Ben Patella, Sam Naffziger

Intel, Fort Collins, CO
Presentation Overview

• Montecito Clock System Architecture
• Montecito Voltage to Frequency Converter (VFC) Architecture
  – Digital Frequency Divider (DFD)
  – Regional Voltage Detector (RVD)
• Results
• Summary and Acknowledgements
Montecito Clock Generation Overview

- PLL generates master clock: $F_{\text{max}} = M \cdot F_{\text{bus\_clock}}$
- DFDs lock on $F_{\text{max}}$ using local DLLs
  - Synthesize core / uncore frequencies in 1.6% $F_{\text{max}}$ steps (ticks)
  - DFD range is $F_{\text{max}} \cdot 1.0$ to $F_{\text{max}} \cdot 0.504$
  - Translation table sets DFD frequency at startup
- Supply / Clock Domains
  - 2 Cores: variable $V$, $F$
  - Uncore (bus logic): fixed $V$, $F = N \cdot \text{bus clock}$
  - Foxton controller: fixed $V$, $F = 1 \text{ GHz}$, DSP algorithms
  - Master PLL: fixed $V$, $F$, within clock system only
Clock System Modes

• Fixed Frequency (FFM)
  – Cores/Uncore are frequency and phase aligned
  – Cores/Uncore interfaces synchronous

• Variable Frequency (VFM)
  – Core supply modulated by Foxton Controller to manage power envelope
  – Core frequencies track Vcore via Regional Voltage Detector (RVD) V-F curves
    • Respond to Foxton modulation and local transients
    • V-F curves match worst-scaling paths on chip
  – Core/Uncore interfaces asynchronous
Voltage-to-Frequency Conversion (VFC) Per Core

Foxton-managed VDD from VR

Local Blocks

RVD8

RVD9

RVD10

RVD11

~2400um

Utility Clocks

L1 Clock Route To SLCBS

RVD4

RVD5

RVD6

RVD7

DOWN[11:8], HOLD[11:8]

Utility Clocks

L1 Clock Route To SLCBS

RVD0

RVD1

RVD2

RVD3

DOWN[3:0], HOLD[3:0]

Utility Clocks

L1 Clock Route To SLCBS

Local Blocks

VDD

di/dt noise

RVD8 local environment

Process, Temp

VDD

L0 Clock Route from PLL

RVD8 local environment

~2400um
Example VFC Supply Droop Response

- Increased delay asserts period "UP" for two cycles
- Clock period increased
- No Adjust needed this cycle
- Droop increases RVD delay line delay
- Increased delay asserts period "UP" for two cycles
Digital Frequency Divider (DFD) Block Diagram

PLL CLOCK DIFFERENTIAL INPUT

16-PHASE DLL AND INTERPOLATION

64 PHASES

STATE MACHINE

DIVIDE BY 2

STARTUP CONTROL

½ FREQUENCY QUADRATURE DIFFERENTIAL CLOCK ROUTES TO SLCBS

FULL FREQUENCY DIFFERENTIAL "UTILITY" CLOCK ROUTES TO CLOCK SYSTEM

PCSMS

RVD UP / DOWN REQUESTS

TO / FROM SAME-CORE PCSMS

ODCS CONTROL

SCAN AND TRIGGERS

DIVIDE BY 2

16-PHASE DLL AND INTERPOLATION

PERIOD ADJUST +2 TO -1

PCSMS

PCSMS
DFD Phase Selection Datapath

FROM PCSM
- adj0
- adj3
- psel0
- psel3

FROM S/M

FROM DLL

4:1 PHASE ADJUST

16:1 PHASE SELECTION

4:1 PHASE OR & CLOCK DRIVE
VFC/RVD Voltage Tracking and CMOS Critical Path Scaling

![Graph showing delay as a function of supply voltage for five different circuits.](image)
RVD Block Diagram

RVD FSM

- dly0in
- eval0
- dly1in
- eval1
- clk

Delay Line 0A
Delay Line 0B
Delay Line 1A
Delay Line 1B

dly0out

eval0
eval1

dly1out

additional delay CVDs create deadzone

HOLD

DOWN
RVD Delay Line

Coarse Delay Incremental Curves

Fine Delay Incremental Curves

4 Coarse Elements

3 Coarse Elements
RVD Coarse Delay Element

Metal 1 Serpentine Resistor

in

config_fet

VDD

VDD

run

run

GND

GND

nfet

fet

nrun

VDD

nfet

fbp

nrun

out

run

fbn

nrun

nout

run

VDD
RVD Phase Comparator
VFM Performance vs. Supply Noise
FFM/VFM Core/Bus Clock Oscilloscope Traces

FFM, 1.2V
Core clock
1.6GHz

Bus Logic clock
1.6GHz

VFM, 1.2V
Core clock
2.14GHz

Bus Logic clock
1.6GHz
Core Clock Spectral Content

FFM
Fmax=2GHz, Ffixed=1.6GHz, 1.2Vcore

VFM
Fmax=2GHz, 1.2Vcore +/- 100mV, slow RVD curve
Summary

- Clock system enables a dynamic voltage-scaling power management system (Foxton)
  - Generates low-skew fixed- and variable- frequency clocks
- High-BW Voltage-to-Frequency conversion (VFC)
  - Regional Voltage Detectors
  - Synchronized Digital Frequency Dividers
  - VFC follows programmed V/F response
  - VFC lock onto and tracks local supply voltage
    - Tracks high-BW switching transients: 1 cycle VFC loop response
    - Tracks low-BW Foxton-based supply modulation
- Performance benefits through reduced guardband:
  - Fast response to switching transients (3-8%, path dependent)
  - Tracks process, temperature (3%)
- VFM operation demonstrated above 2GHz
Acknowledgements