A Versatile Low-Jitter PLL in 90nm CMOS for SerDes Transmitter Clocking


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Outline

- **Objective**
- **Dual-Path PLL Architecture**
- **Design Considerations**
- **Measurements**
- **Performance Summary**
- **Conclusions**
Objective

- Tx clocking for embedded wireline SerDes applications (Ethernet, FibreChannel, PCIe, SAS/SATA, XFI, SONET, ...)
- Support of multiple rates, protocols & reference clock frequencies per Tx-Rx channel
- Backward compatibility with existing serial links
- Strategy: flexible loop dynamics, wide tuning range, versatile divider configurations & small size
Dual-Path PLL Architecture

Proportional Path

Integrating Path

LC-VCO

Programmable Divider (÷N)

PLL OUTPUT CLOCK

Coarse Tuning

Calibration Logic
PLL Closed-Loop Dynamics

Transfer function has 1 zero \((z)\) & 2 poles \((p_1 & p_2)\)

\[
H(s) \approx \frac{\omega_n^2}{z} \cdot \frac{s + z}{s^2 + 2\zeta \omega_n s + \omega_n^2}
\]

\[
\zeta = \frac{K_{pp} K_{vpp}}{2N \sqrt{K_{ip} K_{vip} C_{ip}}}
\]

\[
\omega_n = \sqrt{\frac{K_{ip} K_{vip}}{C_{ip} N}}
\]

For overdamped case \((\zeta > 1)\), \(z\) cancels \(p_1\)

\[
\omega_{-3dB} \approx -p_2 \approx 2\zeta \omega_n = \frac{K_{pp} K_{vpp}}{N}
\]

\[
\zeta \propto \frac{K_{pp}}{\sqrt{K_{ip}}}
\]

bandwidth

inverse peaking
Outline

• Objective
• Dual-Path PLL Architecture
• Design Considerations
  – Loop Filter Proportional Path
  – Mismatch in Loop Filter Phase Offsets
  – LC-VCO Architecture
  – Inversion-Mode nFET Varactors
  – Tuning Range Factors
• Measurements
• Performance Summary
• Conclusions
Loop Filter Proportional Path

- Stretch $V_{OUT}$ pulse in time to reduce reference spur
- $V_{OUT}$ pulse $\sim$50% duty cycle, independent of divider ratio
- Resistorless $\rightarrow$ area-efficient
Proportional Path Implementation

W/2 switch feedthrough & charge cancellation FETs
Effect of Mismatched Loop Filter Phase Offsets

- Minimize $\phi_{os}$ mismatch between all loop filter paths to reduce PLL jitter
- Charge pump dynamic range issue: need big switches for large $I_{cp}$ but may compromise $\phi_{os}$ at small $I_{cp}$
LC-VCO Architecture

- Calibration Setting (CS)
- Proportional Path Tuning
- Integrating Path Tuning

- multilevel helical inductors
- PVT-insensitive capacitance averaging during calibration
- Amplitude Control

- differential outputs

- analog, digital
- 10, 12, 127
Inversion-Mode nFET Varactors

C-V flatness for supply noise rejection

• Critical for integration with digital systems
Tuning Range Factors

- Large tuning range $\rightarrow$ maximize $C_{\text{max}}:C_{\text{min}}$ ratio
- Large $C_{\text{max}}$ $\rightarrow$ large $W \times L$
- Small $C_{\text{min}}$ $\rightarrow$ long $L$ to reduce $C_{\text{ov}}$ & $C_{\text{sub}}$, reduced $Q_C$
  $\rightarrow$ minimize wiring parasitics (contact-to-poly)
- Reduce channel mechanical stress $\rightarrow$ increase $Q_C$

![Diagram of transistor with labels for contact, nitride spacer, poly gate, source, drain, halo/pocket implants, and p-Si layers. The diagram also indicates low and high doping areas.](image)
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• Objective
• Dual-Path PLL Architecture
• Design Considerations
• Measurements
  – PLL Closed-Loop Dynamics
  – PLL Output Jitter
  – VCO Tuning
  – VDD & Temperature Sensitivities
  – Die Micrograph
• Performance Summary
• Conclusions
PLL Closed-Loop Dynamics

-3dB BW (MHz)

Proportional Path Gain

Integrating Path Gain

Modeled

Measured

Peaking (dB)

Proportional Path Gain

Integrating Path Gain
PLL Output Spectrum @ 10Gb/s

- 101010... data pattern (no ISI), $N=50$
- Extracted RMS Jitter = 0.81ps
VCO Coarse Frequency Tuning

- CS = coarse-tuning varactor inputs tied to $V_{DD}$
- 7 VCO variants shown, each with 45% tuning range
- Coverage of practical SerDes protocols
- Loop filter outputs mid-railed during calibration
VCO Post-Calibration Tuning

course tuning curves across $V_{DD}$ & Temp corners

VCO has ±10 varactors of tuning to correct for VCO sensitivities to $V_{DD}$ & Temp drifts after calibration

$\Rightarrow$ Measure CS Range (A–B)

0.9-1.1V, 0-110°C

0.9-1.1V @ 85°C

0-110°C @ 1.0V

VCO variants
VCO Temperature Sensitivities

Resonance for lossy LC tank:

\[
\omega^2 = \frac{1}{LC} \cdot \frac{1 - R_L^2 C}{1 - R_C^2 C} \equiv \frac{1}{LC} \cdot \frac{1 + \frac{1}{Q_C^2}}{1 + \frac{1}{Q_L^2}}
\]

For \( Q_L \ll Q_C \):

\[
\frac{d\omega}{dT} \bigg|_{C,L} \approx -\frac{R_L^2}{\omega L^2} \cdot TCR
\]

\[
\frac{dC}{dT} \bigg|_{C,L} \approx \frac{2R_L^2 C^2}{L} \cdot TCR
\]

0-110°C @ 1.0V

CS Range

Frequency (GHz)
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Conclusions

- Presented PLL offers significant versatility to meet variety of SerDes Tx applications
- Resistorless dual-path loop filter provides area-efficient & flexible control of PLL dynamics
- Phase offsets in multiple-path loop filters must be reduced to suppress reference spurs
- Process considerations are critical for VCO tuning range optimization
- VCO inductor loss & varactor C-V flatness determine post-calibration tuning & jitter sensitivity