IEEE Distinguished Lectures
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Nanometer CMOS: an analog challenge!

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1 km$^2$ = 4 months of production = 70,000,000,000 $
**Small dimensions on large wafers**

**Wafer Size History**

- 200mm/1990
- 300mm/2001
- **450mm/2012**
- 675mm/2021?

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**IC industry: Quo vadis?**

- 90 nm
- 65 nm
- 45 nm
- 32 nm
- 22 nm

*Intel*
Moore’s law: Cost per IC function

Reference point: 30 mm² in CMOS12, Dataquest: monitor of wafer price per unit area 1998-2005 Dataquest mask cost: 1998-2010

Economy dictates large series of products:
memories,
processors,
multi-system ICs, with a multitude of functions
More on a chip: the power crisis

Power = activity x frequency x capacitance x voltage^2

Power crisis:

Need to reduce power supply voltage limited by:

- sub-threshold leakage
  (can be avoided by switching functional blocks)

- variability
Outline

• Introduction

• Variability

• Measuring for signal integrity

• Outlook

Variability:

**Deterministic** effects, but difficult to predict and control:
- NBTI
- Lithographical deviations
- Signal integrity
- Stress (by wiring or STI)
- Temperature gradient
- Substrate noise

**Stochastic (random) processes:**
- Component mismatch
- Jitter
Variability:
90 nm CMOS
Frequency distribution of free-running oscillators
16x7 per reticule

Center donut
boundary
Reticule
Random deviations

Litho: printability for different pitches

- Deep sub-micron means: working on sub-half wavelength features
- Features cannot be printed in forbidden pitch zones!

Printing quality (Cpk)

Pitch

NA=1.05
NA=1.2
Trend: fixed-pitch layout

- Sub half-wavelength feature printing requires uniformity in layout design.

Limits to accuracy

Basic limit to accuracy are the limits to reproduce exact copies.
Accuracy in 0.25 μm CMOS

Granularity on molecular level is reached:
0.25/0.25 transistor = 1200 doping atoms

\[ V_T \propto 1200 \]
\[ \sigma_{\Delta V_T} \propto \sqrt{1200} \approx 3\% V_T \]

Atoms don’t scale in 65 nm CMOS

Granularity on molecular level is reached:
0.1/0.065 transistor = 60-80 doping atoms in depletion region

\[ V_T \propto 80 \]
\[ \sigma_{\Delta V_T} \propto \sqrt{80} \approx 11\% V_T \]
The mean variation is a matter of good engineering. The standard deviation is inverse proportional to the square root of area.

\[ \Delta V_T = V_{T1} - V_{T2} \text{ in mV} \]

\[ \sigma_{\Delta V_T} = \frac{A_{VT}}{\sqrt{WL}} \text{ in mV} \]

Ref: M. Pelgrom IEEE JSSC 1989 p. 1433
Matching: CMOS 90nm, W/L=10/5

Matching: CMOS 90nm, W/L=1/0.5
**Matching: CMOS 90nm, W/L=0.2/0.1**

- Mismatch dominates process tolerances

**Yield in full-flash ADCs**

- 1.6Gsps 6b ADC
  - Scholtens/Vertegt
  - ISSCC2002

- Probability of monotonicity
  - 7-bit, 8 bit, 9 bit, 10 bit

- Yield
  - 0 mV, 2 mV, 4 mV, 6 mV
**Analog and digital**

Diff pair

\[ V_{\text{in}} \rightarrow \sigma_{\Delta V_T} \rightarrow W,L \rightarrow V_{\text{ref}} \]

Latch

\[ E_{\text{gate}} = C_{\text{gate}} \times \sigma_{\Delta V_T}^2 = C_{\text{ox}} A_{VT}^2 \approx 100kT \]

Transistor mismatch dominates thermal noise:
- Major issue in many analog components
- Requires extensive measures in multiplexed systems
- Starts bothering digital designers

**Transistor mismatch**

\[ \sigma_{\Delta V_T} = \frac{A_{VT}}{\sqrt{W \times L}}, C_{\text{gate}} = WLC_{\text{ox}} \]

**SRAM has problems...**

Static Noise Margin: size of “eye” defines robustness

SRAM cells now move from 6T to 7,8 and 10T implementations
SRAM moving to 10 transistor cell

Ref: B. Calhoun, MIT, ISSCC2006

...getting worse for new generations.

\[ W_p = 2W_n = 8L_{\text{min}} \]

<table>
<thead>
<tr>
<th></th>
<th>0.25 (\mu m)</th>
<th>0.18 (\mu m)</th>
<th>0.13 (\mu m)</th>
<th>0.1 (\mu m)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(\sigma_{\Delta T_2}) (C_{\text{load}}=50\text{fF})</td>
<td>16 ps</td>
<td>21 ps</td>
<td>38 ps</td>
<td>68 ps</td>
</tr>
<tr>
<td>(\sigma_{\Delta T_2}) (50,35,25,20\text{fF})</td>
<td>16 ps</td>
<td>16 ps</td>
<td>22 ps</td>
<td>33 ps</td>
</tr>
</tbody>
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Variability, random component mismatch:

• Mismatch in analog circuits is a well-known problem, some interesting correction algorithms allow to fight this problem.

• In nanometer CMOS mismatch dominates over process corner variation.

• Memory designers spend more transistors to overcome the problems.

• Stochastic nature requires new approaches and more analog way of thinking in digital.

Variability:

**Deterministic** effects, but difficult to predict and control:
  - NBTI
  - Lithographical deviations
  - Signal integrity
  - Stress (by wiring or STI)
  - Temperature gradient
  - Substrate noise

**Stochastic (random)** processes:
  - Component mismatch
  - Jitter
**Substrate Noise:**

A designers view

**The problem:**

0.0000000000001 Watt sensitivity

0.1-5 Watt
The problem:

Interference generator:
every node of the circuit is contributing, depending on frequency components, capacitor, undershoot

Interference channel:
mostly through substrate, but may take short-cuts!

Interference receiver:
every node picks up interference, many (canceling) paths

A simple experiment

V_{DD}

N-well

0.18 um CMOS
High-ohmic substrate

Courtesy: AMoS/G. Vogels
A simple experiment
8 variants in x, y, guard ring silicon compared to simulation

A simple experiment
0.18 um CMOS
High-ohmic substrate
Substrate model extracted by commercial tool:
5487R’s and 6765 C’s

Courtesy: AMoS/G.Vogels
A simple experiment
8 variants in x,y, guard ring
silicon compared to simulation

70 dB between different layout implementations !
(interferer: 1 MHz sine wave at 100 mV amplitude)

Courtesy: AMoS/G.Vogels

Power rail $R$ determines net effect!

$Z_{ring} = 10 \, \Omega$

$R_{GND}$
A simple experiment!?  

injection through digital logic

Commercial tool:
- From 456403 into 11 internal nodes
- CPU 2h:7m:28s!
- Memory: 1.7G
- Sub circuit spice file: 260MB

Too complex substrate description for interpretation

Variability, substrate noise:

- Still a problem hardly realized by digital designers.
- Major limitation for integration possibilities for connectivity.
- Complex due to interaction between power wiring and substrate.
- No real CAD solution available.
Variability: What to do?

- Actual values from stochastic distributions cannot be predicted.
- Circumstances can be measured
- More optimum setting can then be achieved

Measuring of analog parameters in VLSI ICs

Signal Integrity Self Test (SIST) architecture
SIST Monitor Specification

• Power Supply Sensor: overshoot, dips, average value
  – 20mV resolution @ 100ps pulse width

• Temperature Sensor
  – 0-150°C with 10°C resolution, untrimmed

• MOS threshold voltage sensor
  – 10mV resolution

• Timing sensor
  – $T_{clock}/16$ resolution

In design
Analog challenges

- No impact on the digital design flow, library and specification
- No additional Vdd and Vss
- Matches standard cell layout style
- Area penalty around 0.1%
- No analog interfaces
- Switched off during non monitoring
- Control algorithm complies to IEEE 1149.1 std. (keeps compatibility to present test equipment)

Supply noise monitor: circuit diagram
Trend of the usable Beta

Usable Beta behaviour: background

- **Short channel**
  - high dope level
  - impaired mobility
  - threshold variability

- **Long channel**
  - low dope level
  - better device behaviour
  - poor output impedance
Supply noise monitor: lay-out

The supply noise monitor in standard-cell style (tiling patterns removed).

Area: 4 pitches high, 124 μm wide

Test set-up

Functional block
Activity programmable Shift register
2000 flipflops + 25,000 gates

Monitor 1
Register/TPR
Monitor 2
Register/TPR

SIST controller
TAP

IN/OUT SIST
### Functional Core Layout

- Test settings:
  - Switching activity
  - Vary frequency
  - Different decap

### Silicon

- Four identical functional cores
  - A: No decap
  - B: Half decap
  - C: Nominal decap 500pF
  - D: Double decap
- With different test settings
- In 90nm CMOS process
Simulation Results

![Simulation Results Graph]

Measurements Results

![Measurements Results Graph]
Temperature Monitor and Reference

\[ V_{\text{ref}} = 0.8V \]

Temperature range: 1.05-1.4 V

Measurement Results:

- **temperature sensor 90 nm CMOS**
- \( \sigma = 4.5mV \)
- Resolution: \( 11^0C \)
SIST Monitor Locations on 65 nm test chip

65 nm test chip
What can be done with SIST info?

Phase 1, today:
- Debug, check for local disturbances
- Compare CAD predictions to real life

Phase 2:
- Improve performance based on actual status.
- Switch between power supply levels
- Control refresh cycle of dynamic memory/logic to the actual temperature (leakage doubles every 6°C)
- Adapt error protection to expected bit-error rate.
- etc.
**Outlook**

- Economical efficiency, (low) power and variability will determine the future choices and options in IC design.
- More digital design decisions will be determined by physical (analog) effects.
- The stochastic nature of variability will force some dramatic changes in design and CAD tools.
- Major adaptations of standard digital cells will be needed to improve variability sensitivity.
- Measuring effects within the digital cores is the first step towards mastering this problem.