

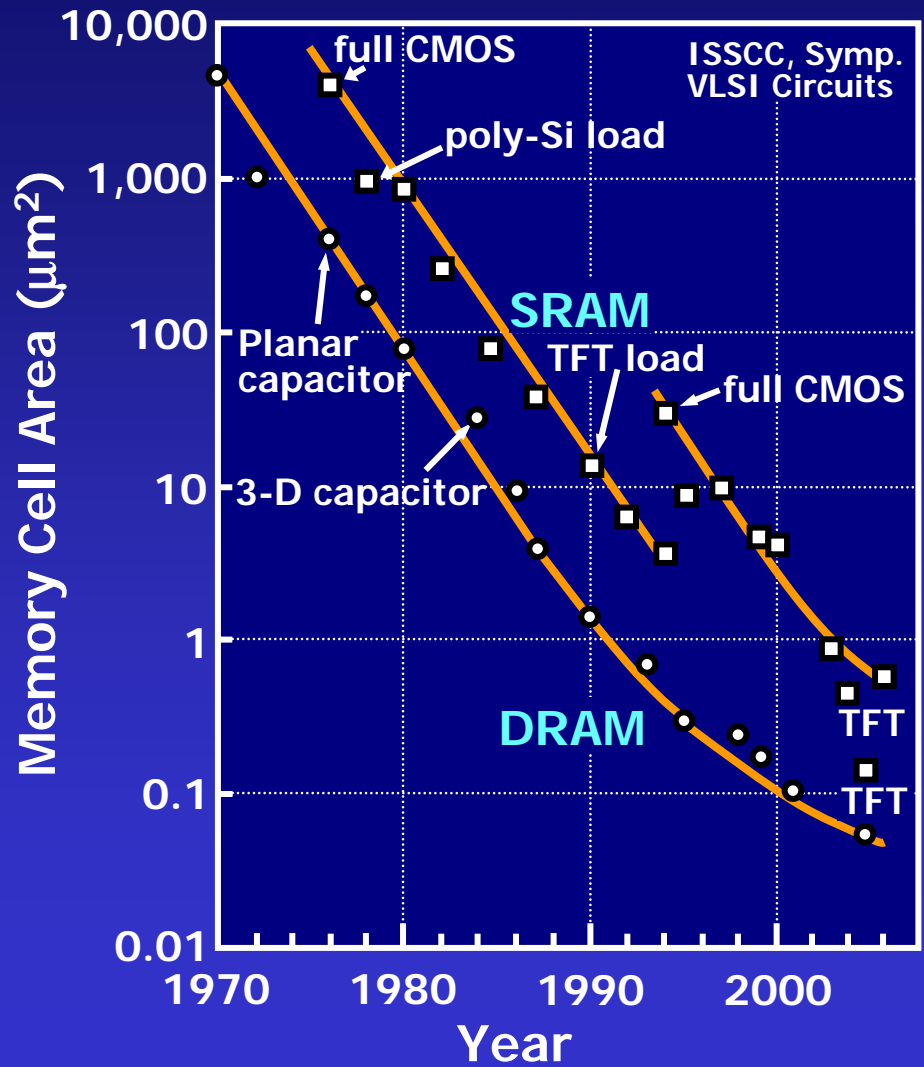
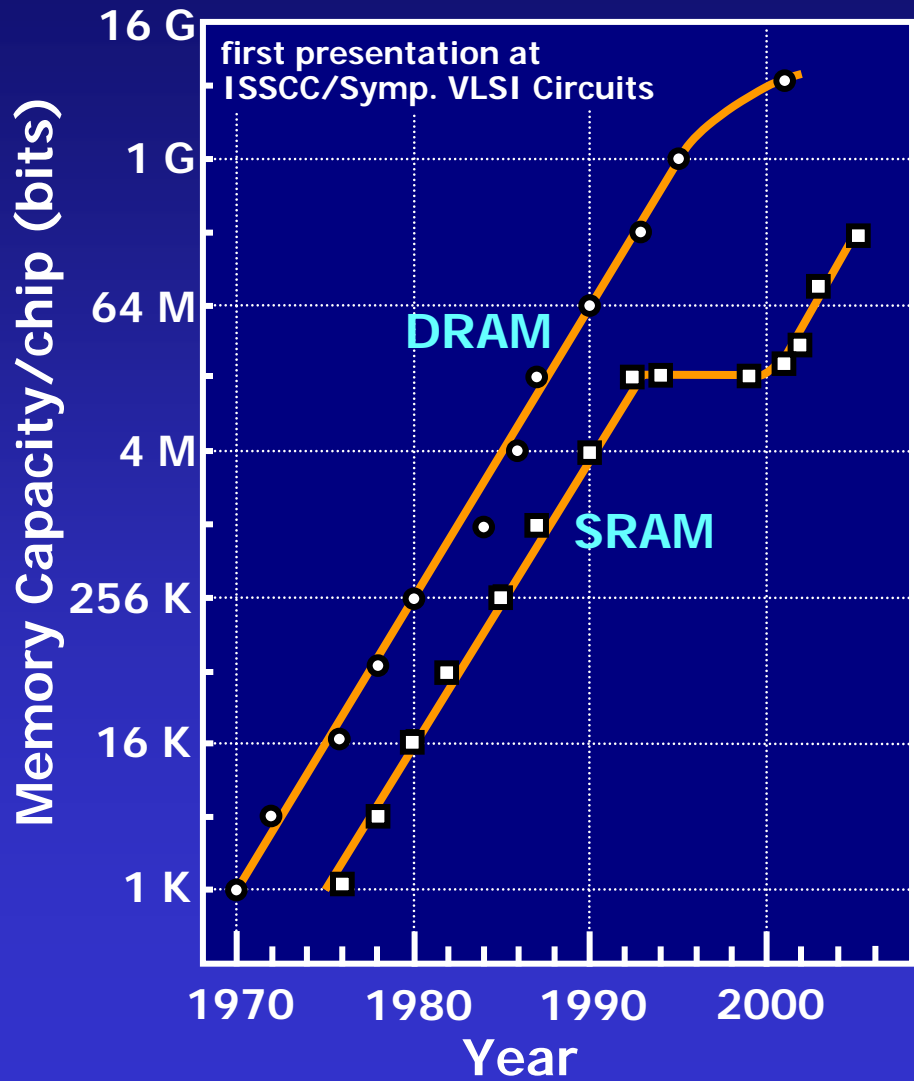
# Ultra-Low Voltage Nano-Scale Embedded RAMs

Kiyoo Itoh, Hitachi Ltd.

## OUTLINE

1. Introduction
2. Trends & Challenges
3. Low-Voltage Limitation of RAMs
4. Leakage & Speed Variation of Peripheral Logic Circuits
5. Memory Cell Size
6. Future Prospects
7. Conclusion

# Trends in RAM Developments (R&D)



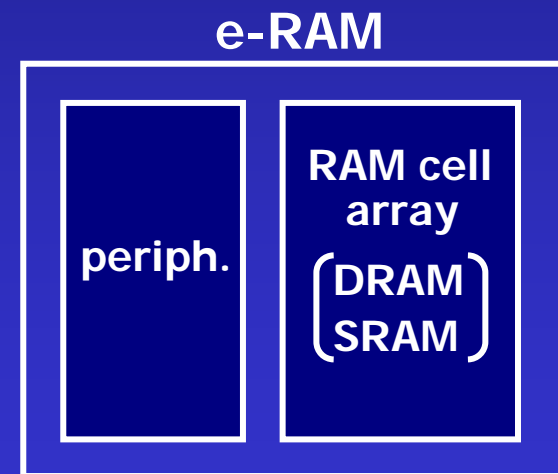
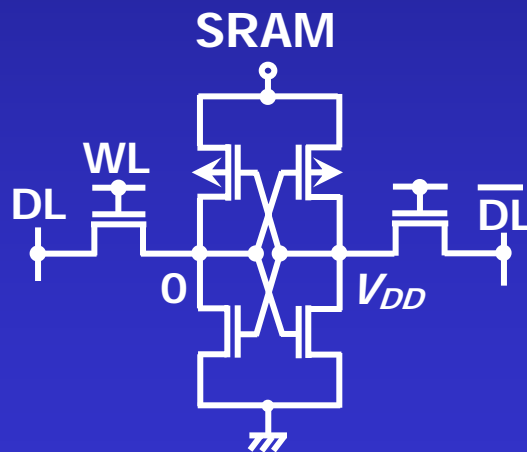
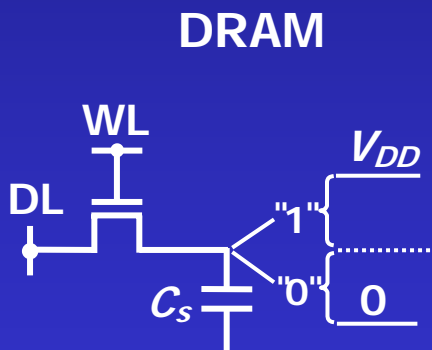
# Challenges to LV e-RAMs

## RAM Cells

- Extend low-voltage limitation to sub-1 V
  - Degraded S/N
  - Increased leakage
- Reduce cell size

## Peripheral Circuits

- Reduce leakage
  - Increased  $I_{STB}$  &  $I_{ACT}$
- Reduce speed variation
  - Unreliable operations



# Low-Voltage Limitation of RAMs

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1. It is governed by soft-error of cells, or S/N of cells and cell-relevant circuits.
2. As long as ECC is used, it is governed by S/N.  
ECC: Error Checking and Correcting circuit
3. S/N is determined by
  - Signal charge & signal voltage of cells,
  - **Flip-flop circuits** that DRAMs use for sense amps, while SRAMs use for cells themselves.

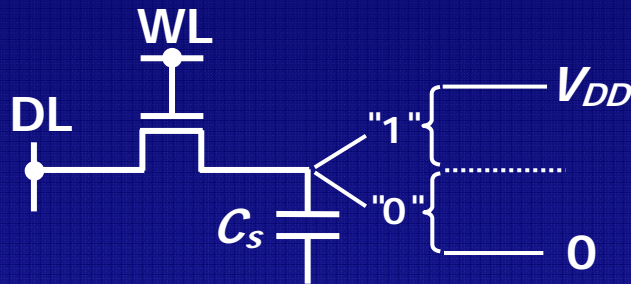
# Comparisons of Flip-Flop Circuits

	DRAM SA	SRAM Cell
Circuit		
Standby	Off with all nodes at $V_{DD}/2$	On with static of all MOSTs
Active	Dynamic sensing of $v_s$ (SN on, then SP on)	$i$ by ratio of $M_1$ & $M_5$ Static of other MOSTs
Margin	Sensitive to $V_T$ & $\Delta V_T$ of only two MOSTs, $M_1$ & $M_2$	Sensitive to $V_T$ & $\Delta V_T$ of all MOSTs → <b>Narrow margin</b>

# Signal Charge $Q_S$ of RAM Cells

$Q_S \cong$  Soft-Error  $Q_{crt}$ . The larger the  $Q_S$ , the smaller the SER.  
 $Q_S$  decreases with device and voltage scaling.

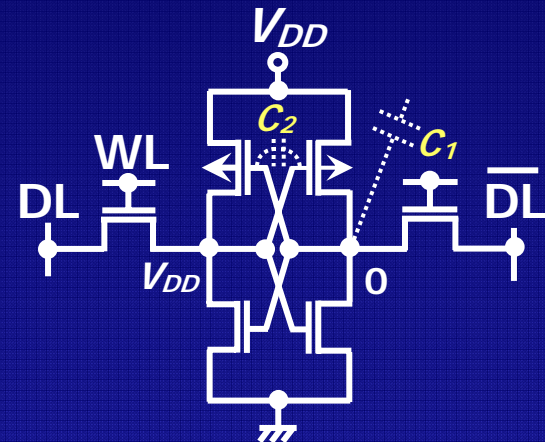
## DRAM



$$Q_S = C_S V_{DD} / 2$$

$C_S$ ; Intentionally added, large, and needs to be gradually decreased with device scaling for maintaining large  $V_{SIG}$ .

## SRAM



$$Q_S = C_S V_{DD}, \quad C_S = (C_1 + 2C_2)$$

$C_1, C_2$ ; parasitic, small, and rapidly decrease with device scaling.

SER is always larger than for DRAM.

# Signal Charge ( $Q_s$ ) of RAM Cells

■  $Q_s$  reduced with capacity due to  $V_{DD}$  & device scaling

Smaller  $Q_s$  of SRAM cell

■ SER depends on  $Q_s$

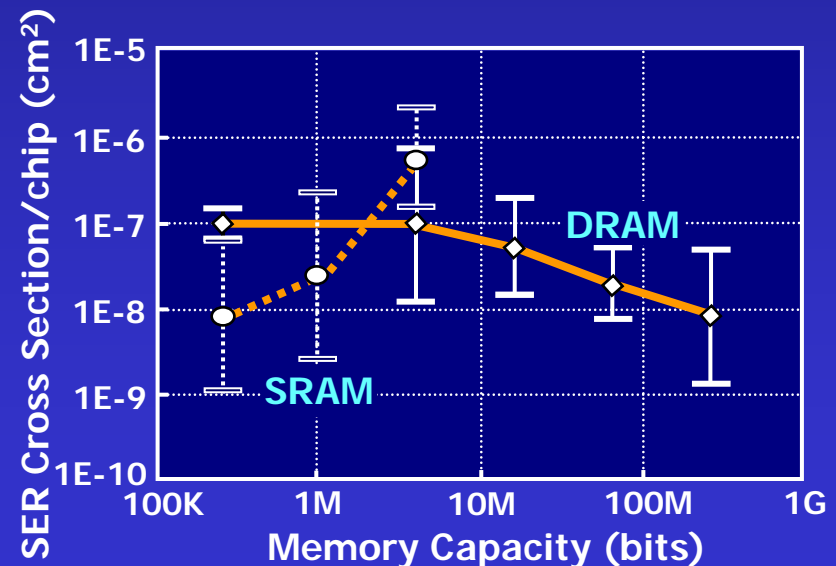
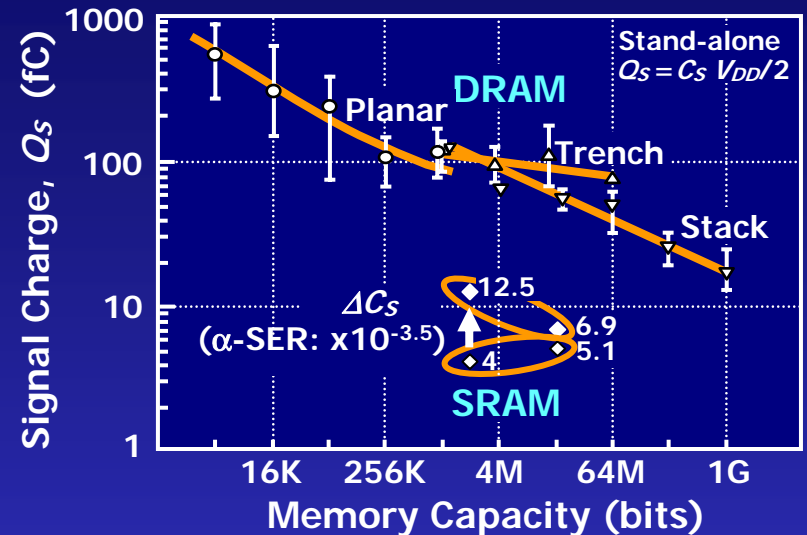
**DRAM**; decreases with memory capacity due to large intentionally-added  $C_s$  & spatial scaling that reduces charge collection.

**SRAM**; increases with memory capacity due to rapidly-decreasing parasitic  $C_s$  despite spatial scaling.

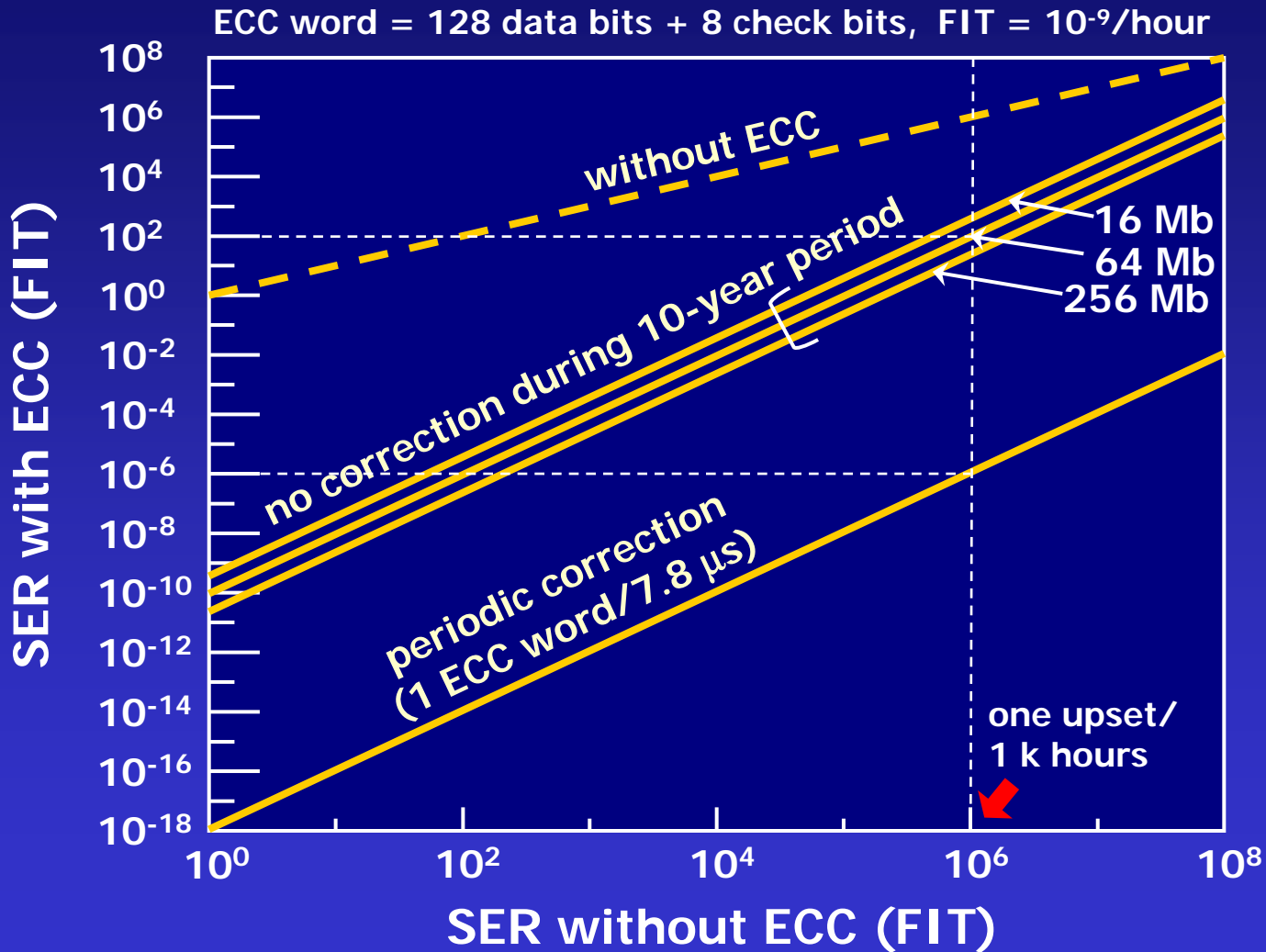
**Solutions:**

- Increase in  $C_s$  (SRAM cells)
- Uses of triple well, redundancy, ECC etc.

Y. Nakagome et al., IBM J. R&D, Vol.47, No.5/6, Sep./Nov. 2003  
E. Ibe, The Svedberg Laboratory Workshop on Applied Physics, Uppsala, May 3, 2001



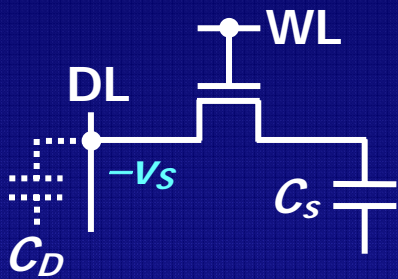
# Error Checking & Correcting (ECC)



# Minimum $V_{DD}$ ( $V_{min}$ ) of RAMs

## DRAM

### Cell



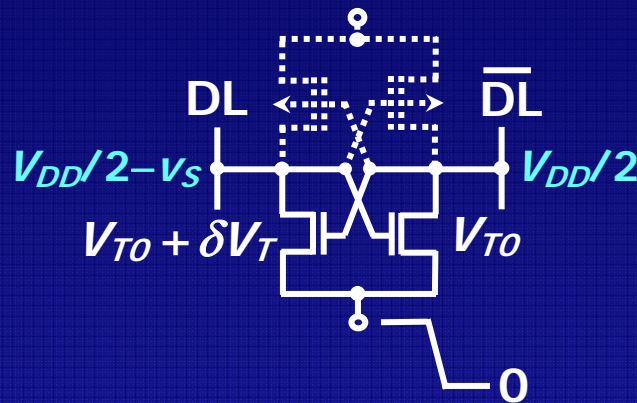
$$V_S > \delta V_T$$

$$V_S \cong (V_{DD}/2) C_S / C_D$$

$$\therefore V_{min} = 2 \delta V_T C_D / C_S$$

$$= 10 \delta V_T (C_D / C_S \cong 5)$$

### SA

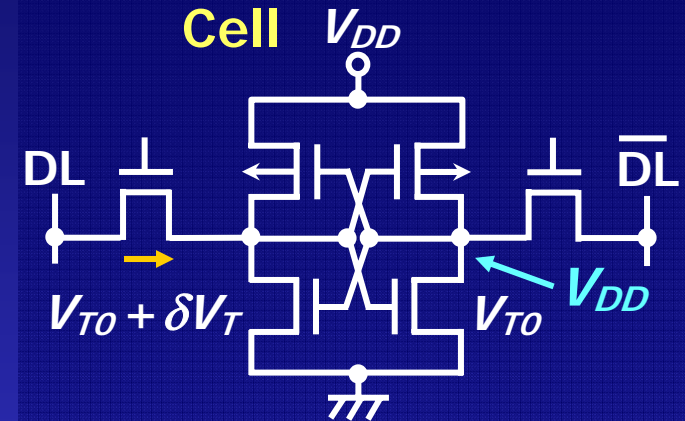


$$V_G = V_{DD}/2 - (V_{T0} + \delta V_T) > 0$$

$$\therefore V_{min} = 2 (V_{T0} + \delta V_T)$$

## SRAM

### Cell



If only cross-coupled nMOSTs determine the voltage margin during read,

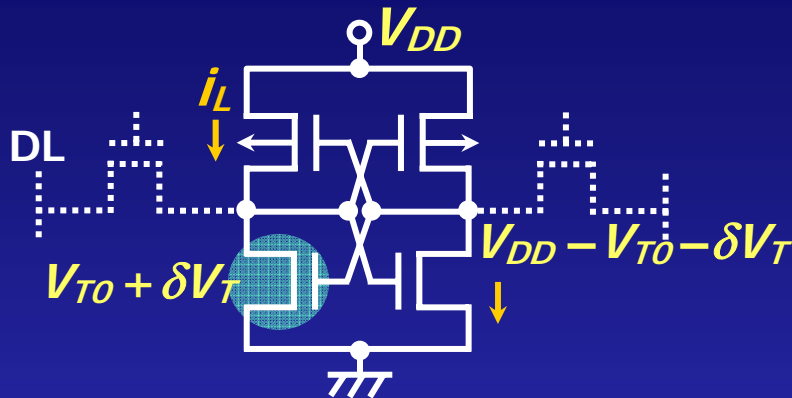
$$V_G = V_{DD} - V_{T0} - \delta V_T \geq 0,$$

$$\therefore V_{min} = V_{T0} + \delta V_T$$

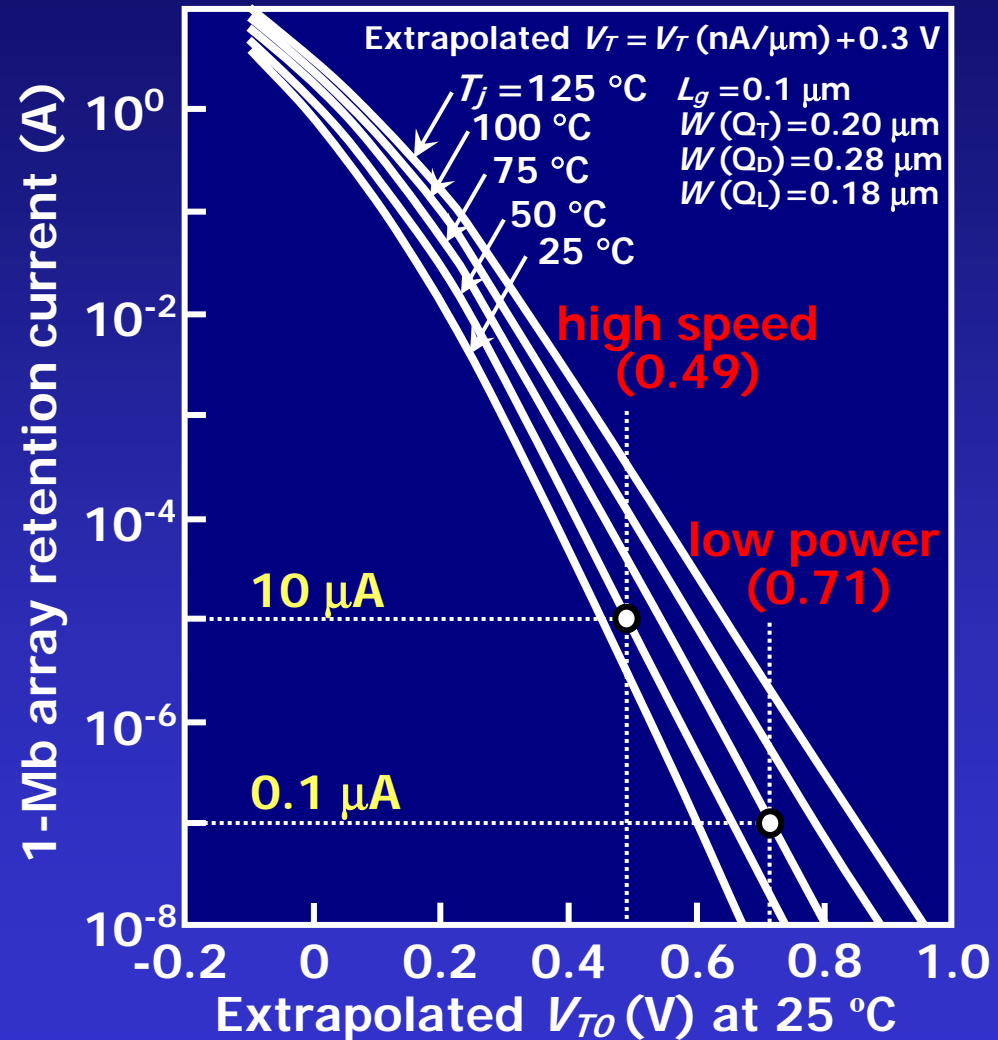
$\delta V_T$ :  $V_T$ -mismatch between paired MOSTs,  $V_{T0}$ : Average  $V_T$



# Lowest Necessary $V_{T0}$ for SRAM Cell



- Cross-coupled MOSTs need a high  $V_T$  to ensure a small retention current through reducing  $i_L$ .
- $V_{T0}$  is the average in a chip, because it is the average that determines retention current of the chip.
- $V_{T0}$  must be quite high and unscalable.



# $V_T$ -Mismatch ( $\delta V_T$ )

## 1. $V_T$ Variation ( $\Delta V_T$ ) as source of $\delta V_T$

- **Extrinsic**  $\Delta V_T$  due to implant non-uniformities &  $\Delta(L, W)$
- **Intrinsic**  $\Delta V_T$  due to random microscopic fluctuations of dopant atoms in the channel area.

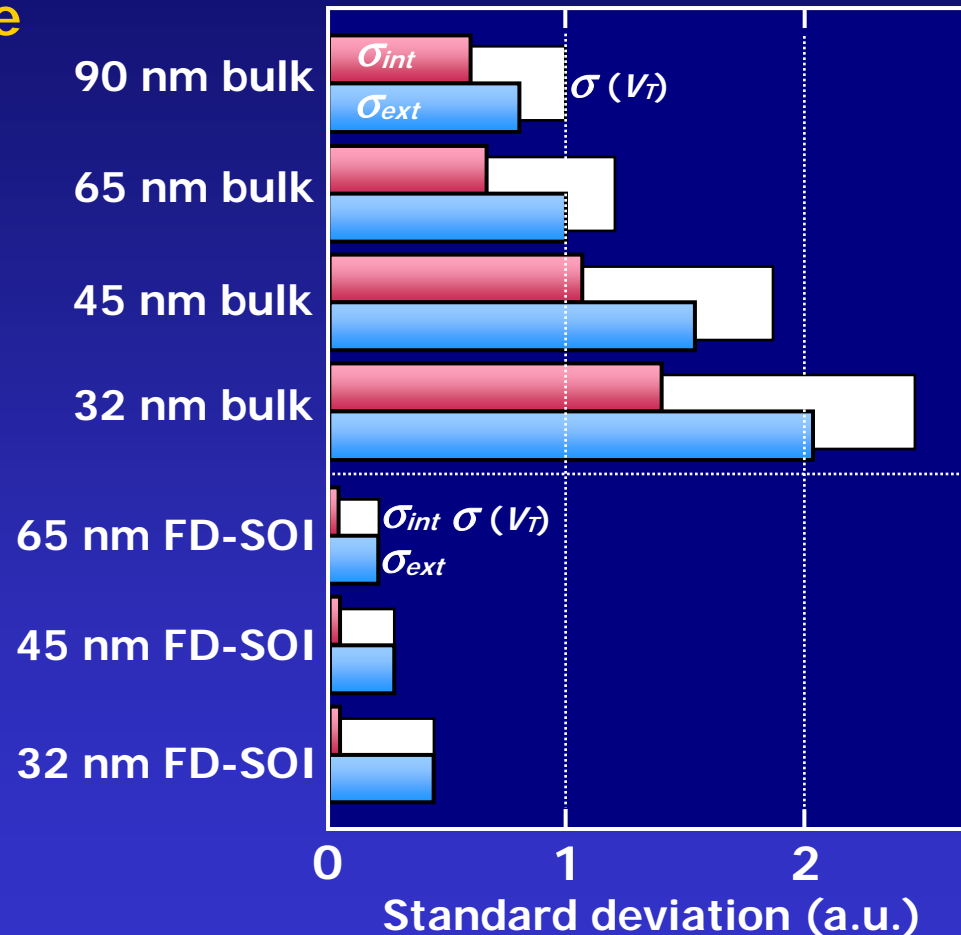
## 2. $\Delta V_T$ & $\delta V_T$ increase with reducing MOST size even for a fixed generation.

$$\sigma_{int} \propto 1/\sqrt{LW}$$

$$\sigma(\delta V_T) \cong \sqrt{2} \sigma_{int}$$

## 3. $\Delta V_T$ & $\delta V_T$ increase with device scaling.

$\Delta V_T$  in a chip has no room in time & area to be compensated for.



M. Yamaoka et al., Symp. VLSI Circuits 2004

# Larger $\delta V_T$ of SRAM cell

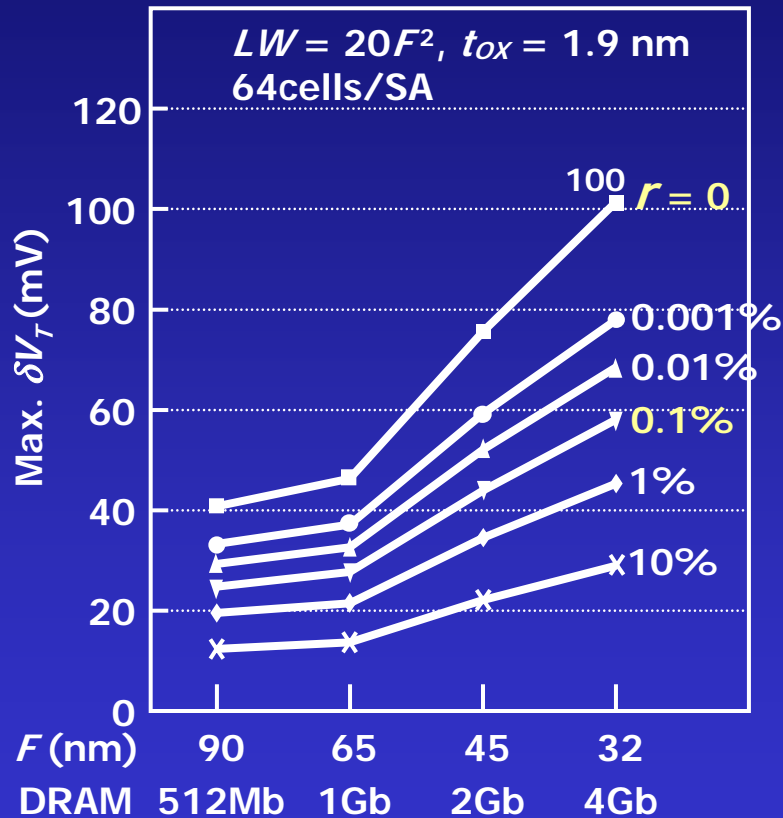
	DRAM SA	SRAM Cell
<b>Circuit</b>		
<b>MOS Size</b>	10 – 20 $F^2$	1.8 – 2.8 $F^2$
<b>Circuit Count in a chip</b>	<p><math>M/(64 - 1024)</math></p> <p>64-1024</p> <p>Relaxed SA layout</p>	<p><math>M</math></p> <p>Array</p>
<b><math>\delta V_T</math></b>	Small	Large

$M$ : memory capacity

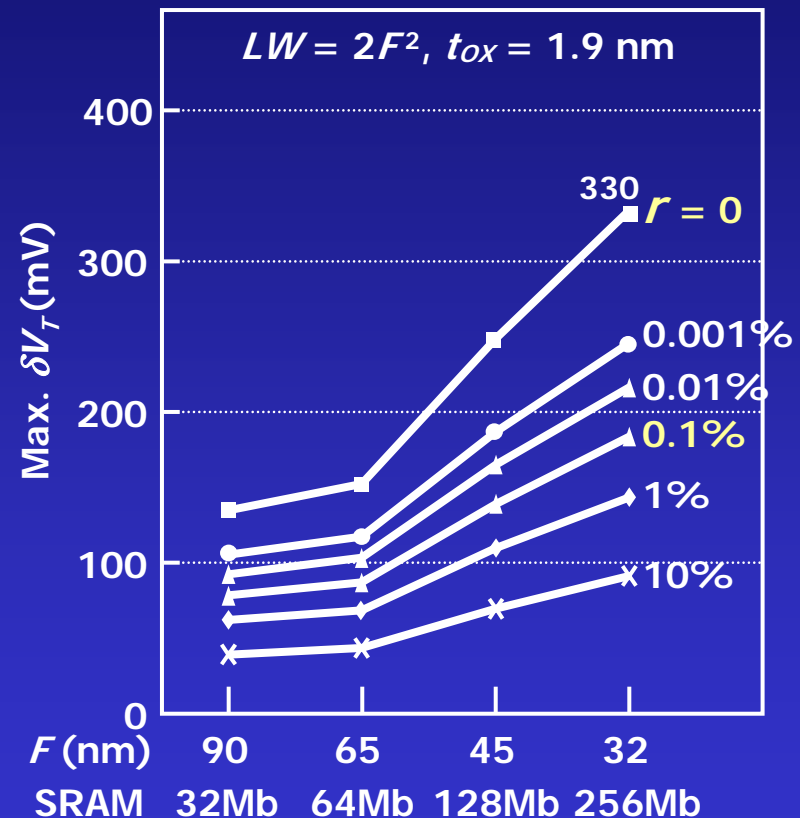
# Maximum $\delta V_T$ in a chip

$r$ : repairable percentage

## DRAM SA

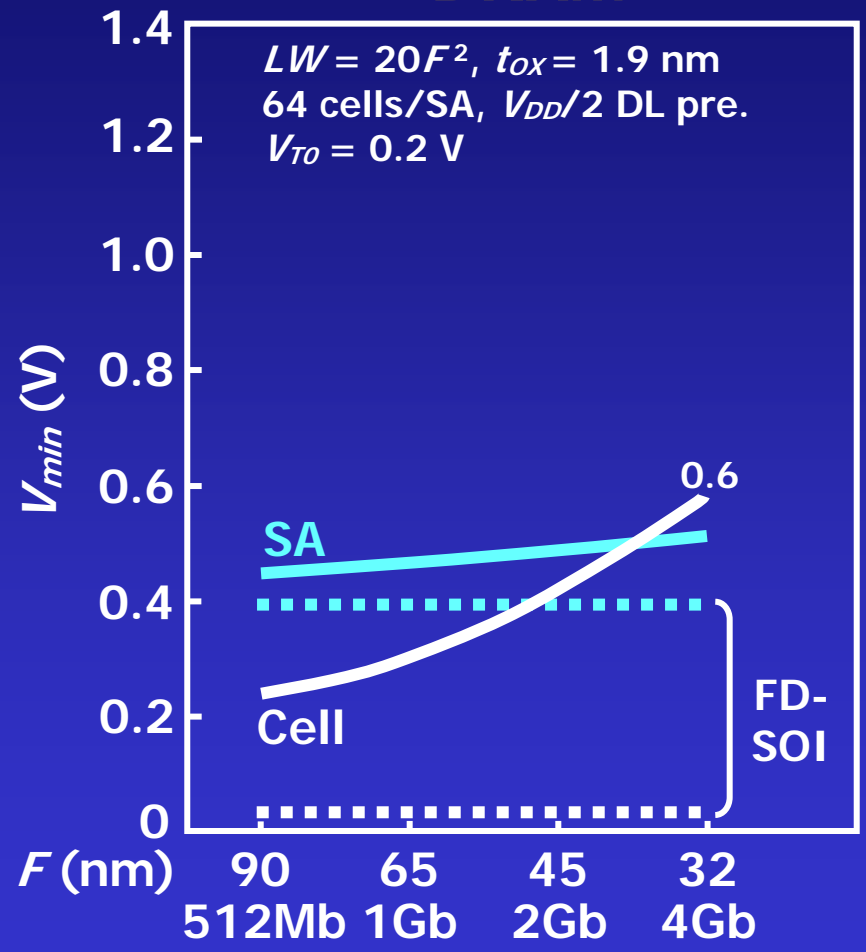


## SRAM Cell

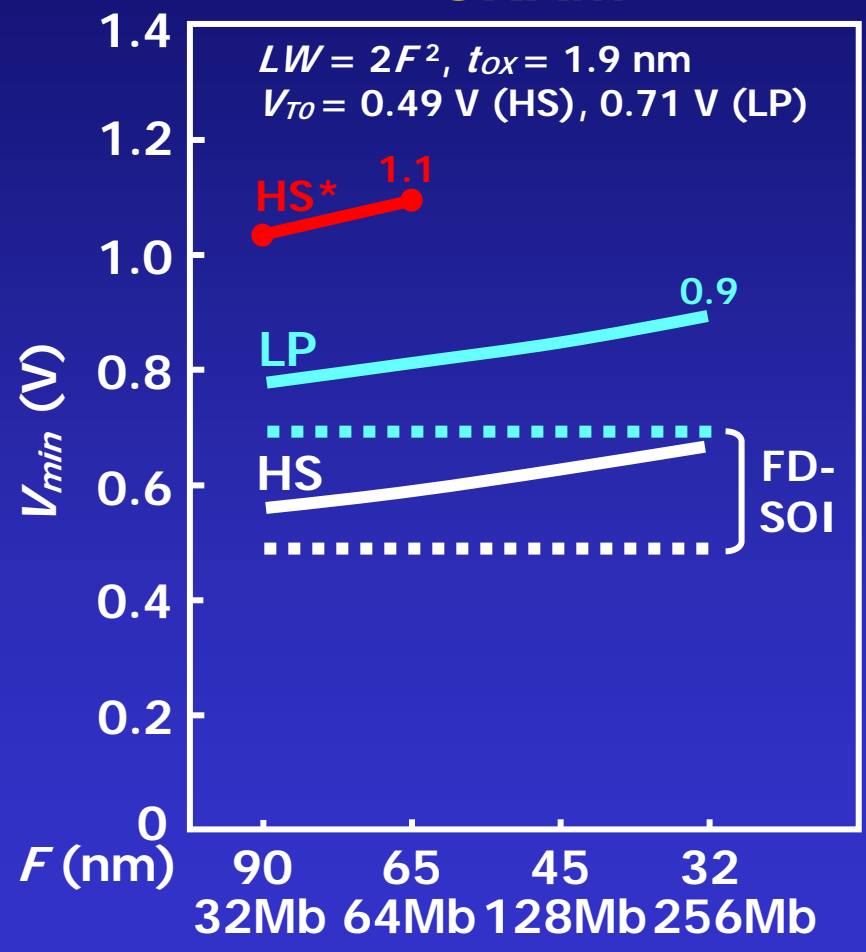


# $V_{min} (r = 0.1 \%)$

## DRAM



## SRAM



\*Actual  $V_{min}$  determined by all MOSTs in a cell.

# Approaches to LV SRAMs

1. Use ECC & Redundancy.

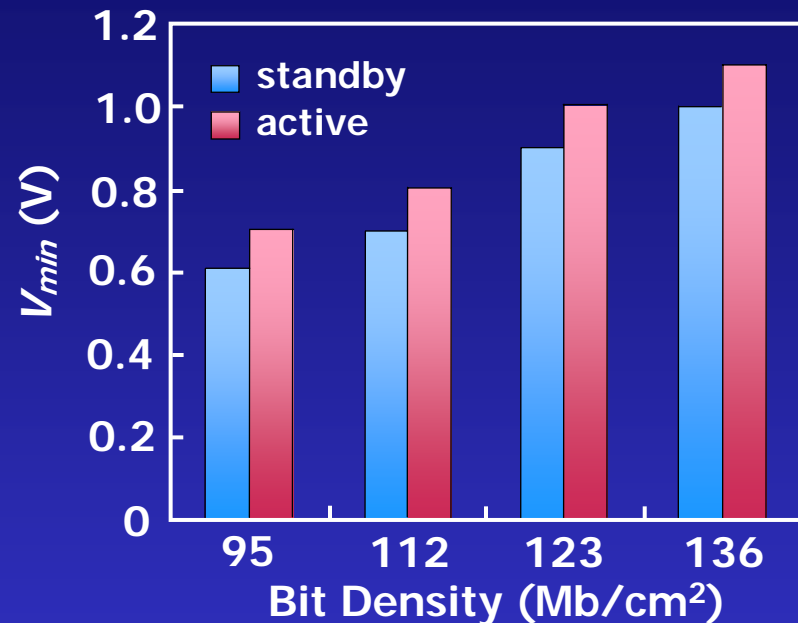
2. Minimize  $\Delta V_T$  &  $\delta V_T$ .

- Large cells with large MOSTs despite losing bit density
- Symmetric cell layout

3. Stay at a high  $V_{DD}$  ( $\geq 1$  V) due to its still large  $\Delta V_T$  &  $\delta V_T$  of **bulk CMOS**.

Even so, power-supply control cells needed for small subthreshold current.

4. Extend low- $V_{DD}$  limitation to sub-1-V with **FD-SOI**.



M. Khellah, et al., ISSCC Dig., pp. 624-625, 2006

# Symmetric Layout for Small $\delta V_T$

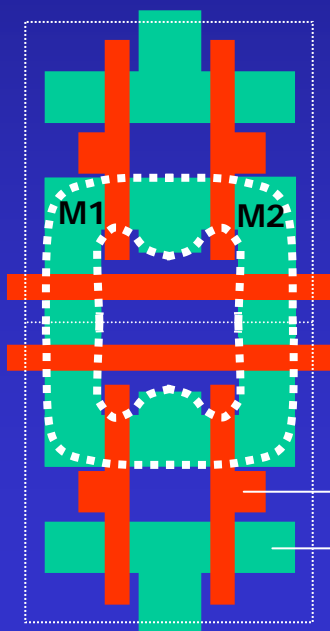
## Sources of extrinsic $\delta V_T$ in the conventional cell:

- Pattern deformation after processing
- Mask misalignment
- Local size fluctuation

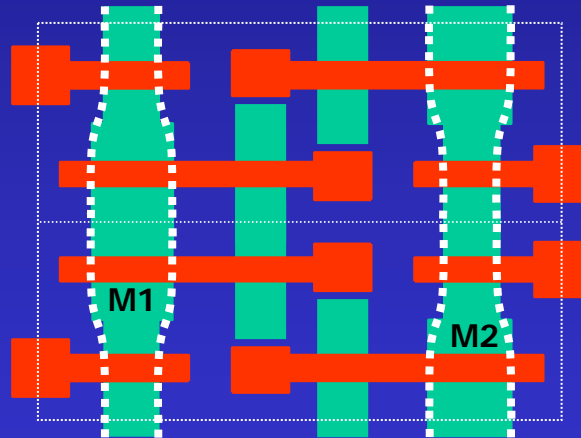
## Solution: Lithographical symmetric cell ("Thin" Cell)

- Reduced  $\delta V_T$  by simple patterns suitable for OPC
- DLs shielded by power lines

Conv. (2 cells)

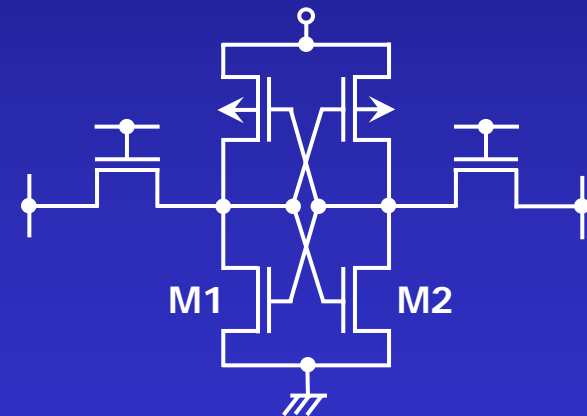


LS cell (2 cells)



poly gate  
diffused

Dotted area:  
after processing



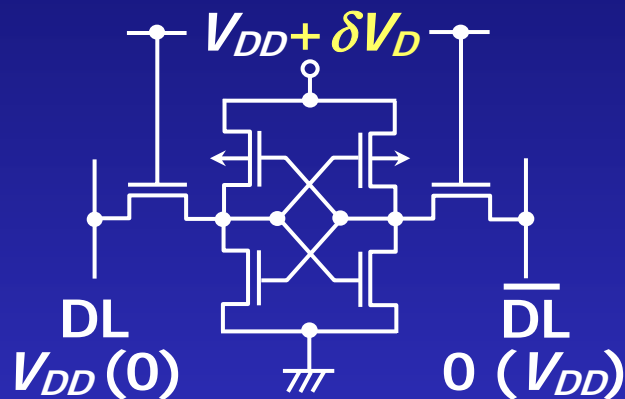
OPC: optical proximity correction

K. Osada et al., IEEE J. SSC, vol. 36, No. 11, pp. 1738-1744, Nov. 2001.  
M. Kanda et al., Symp. VLSI Tech. Dig. Tech. Papers, pp. 13-14, June 2003.  
F. Arnaud et al., Symp. VLSI Tech. Dig. Tech. Papers, pp. 65-66, June 2003.

# Power-Supply Control Cells

for small subthreshold currents

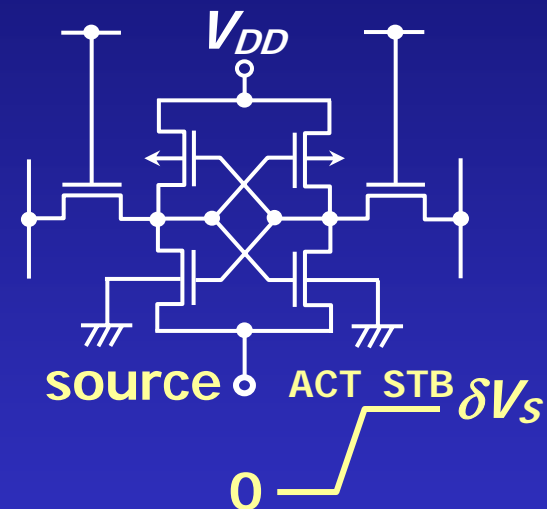
## Boosted Power Supply



- High  $V_T$  to reduce  $i_L$
- $\delta V_D$  to offset a high  $V_T$  &  $\delta V_T$

Low leak, wide margin & low power with low- $V_{DD}$  DL.  
**Unscalable MOSTs needed.**

## Source-Line Driving

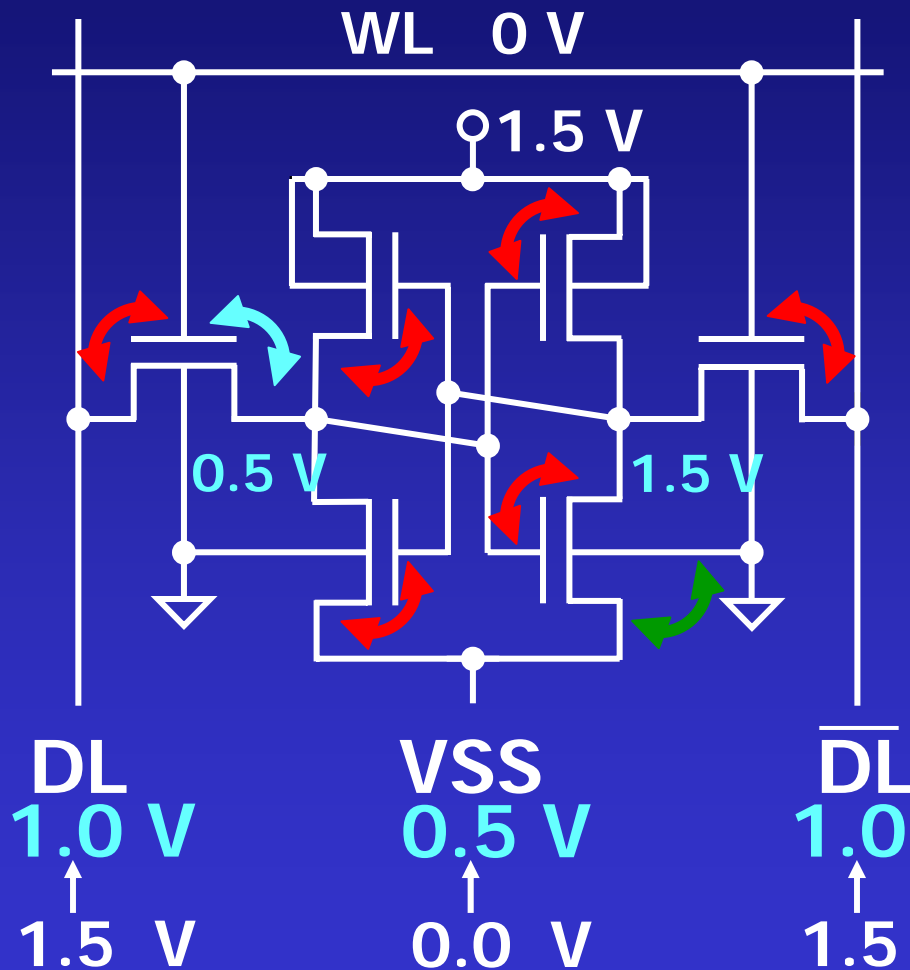


- Raised source during STB to reduce  $i_L$  with increased  $V_T$  of off-MOST

**Reduced margin during STB by  $\delta V_S (>0.3 \text{ V})$**

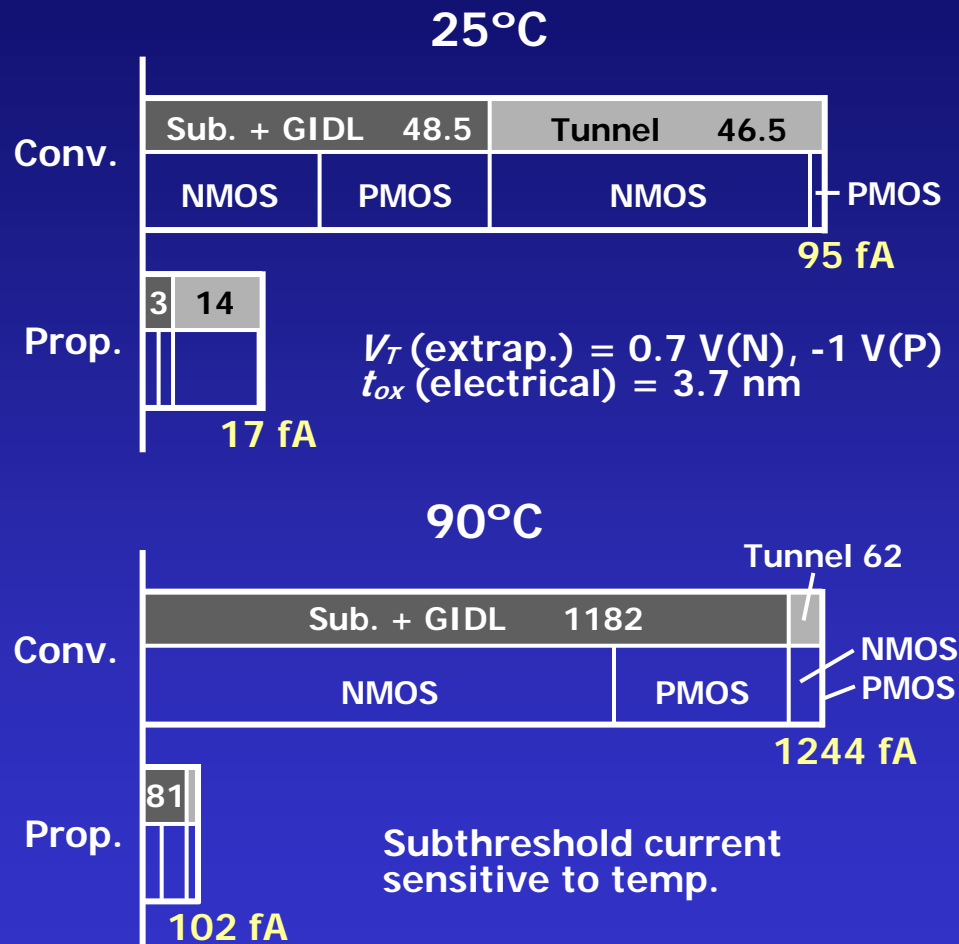
# Source-Line Driving

Along with reduced DL voltage at active-standby transition



- ↪ **Sub-S backbias**  
 90% reduction in subthreshold leakage
- ↪ **G-S backbias**  
 100% reduction in subthreshold leakage
- ↪ **Electric-field relaxation**  
 90% reduction in gate leakage & GIDL

# Measured Retention Current of Cell



## Successful Application

1.5-V 27-ns 6.42 x 8.76 mm<sup>2</sup> 16-Mb using ECC with 3.2-ns/9.7% speed/area penalties.

## Limitations and Challenges

(1) Leakage still large

1.6  $\mu$ A for 16 Mb despite high  $V_T$ , thick  $t_{ox}$ , and S-driving.

(2) **Reduced  $Q_S$  in standby mode**

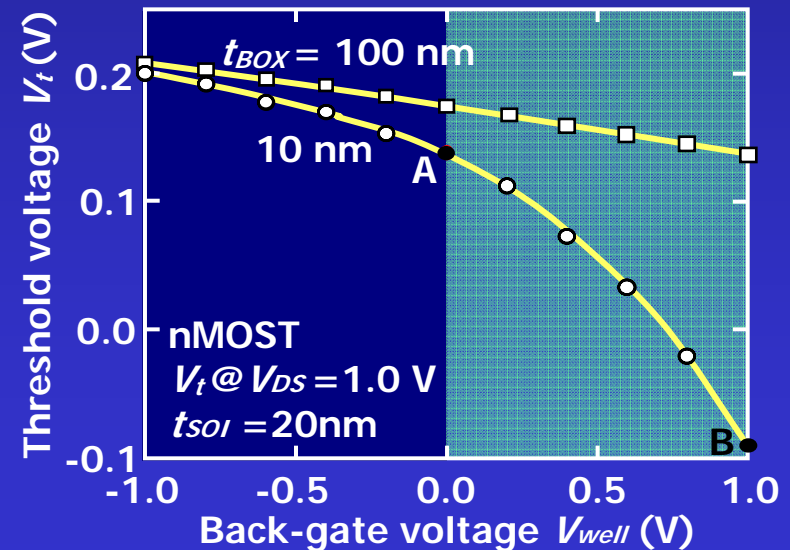
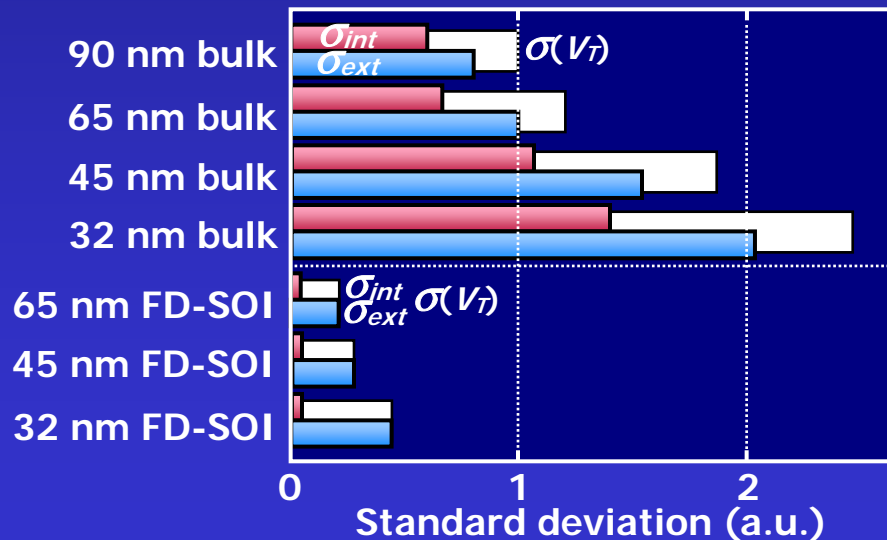
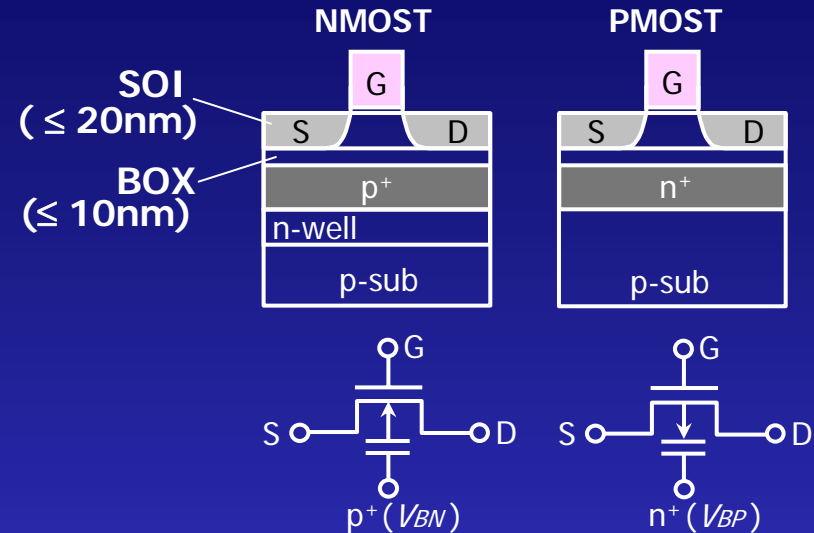
The cell power-supply decreases by the raised source voltage.

Further low- $V_{DD}$  operation may be hazardous, even if ECC is used.



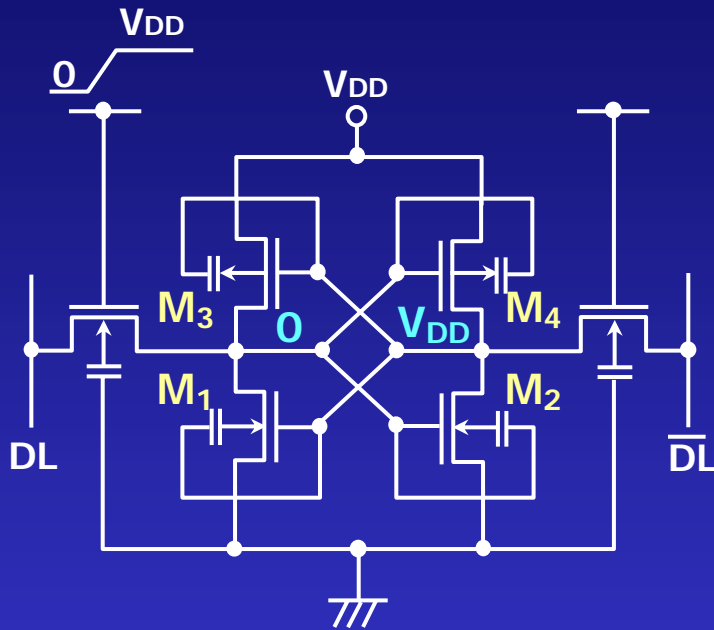
# Double-Gate FD-SOI

- **Small  $\Delta V_T$  & negligible  $\delta V_T$**   
(ultra-thin & lightly-doped channel)
- **Adjustable  $V_T \rightarrow$  multi- $V_T$**
- **Large  $V_T$  change**  
(wide-range well-bias control)
- **Reduced SER & small  $i_{pn}$**
- **Dynamic  $V_T$  MOST**  
(e.g., G-well connection)

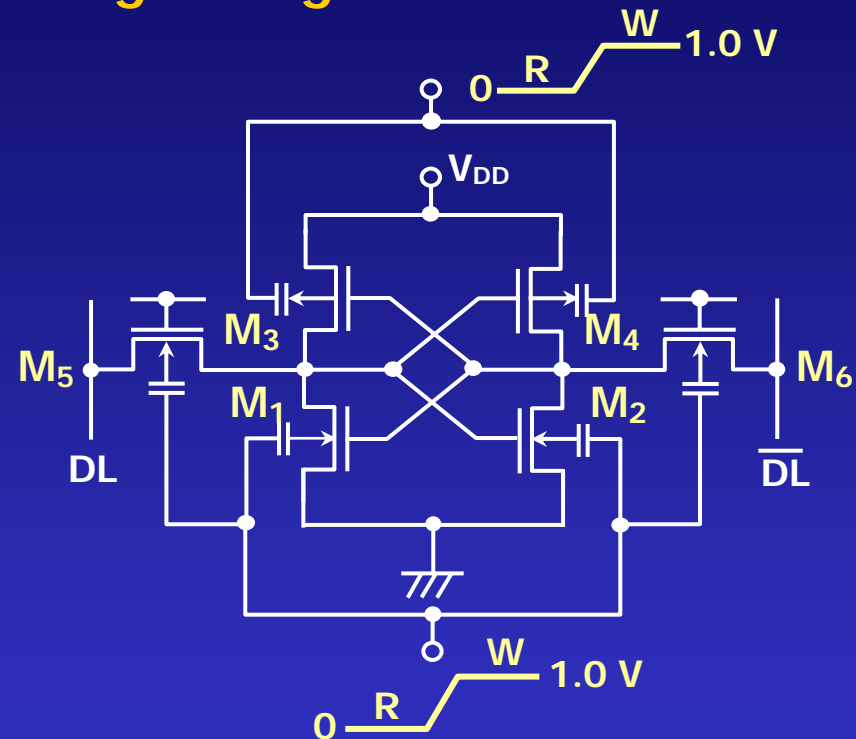


# SRAM Cells with Dynamic- $V_T$ MOSTs

to widen the voltage margin



$M_1$ : decreased  $V_T$      $M_2$ : increased  $V_T$   
 $M_3$ : increased  $V_T$      $M_4$ : decreased  $V_T$



Write margin improved with decreased  $V_T$  for driver/transfer MOSTs & increased  $V_T$  for load MOSTs.

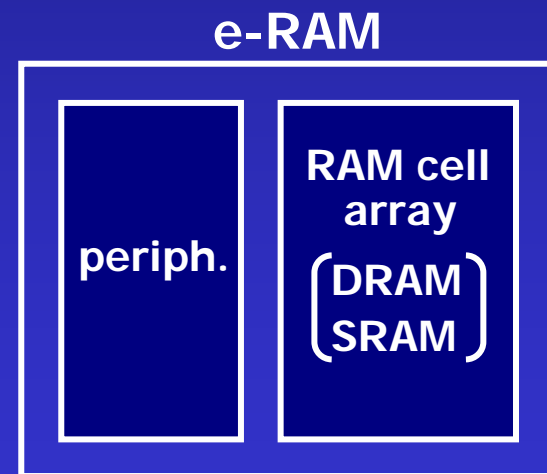
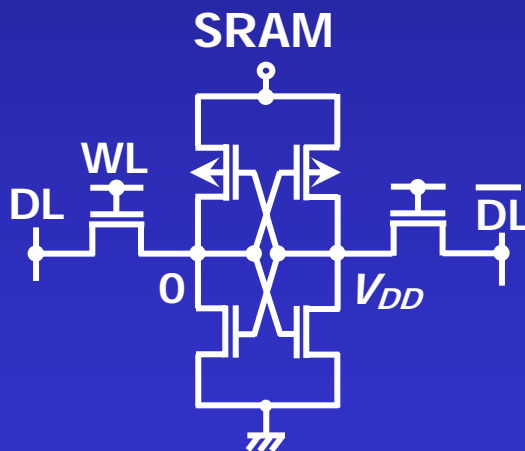
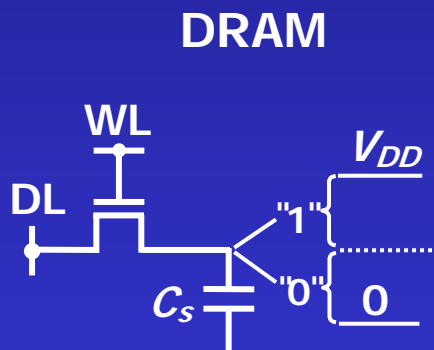
# Challenges to LV e-RAMs

## RAM Cells

- Extend low-voltage limitation to sub-1 V
- Degraded S/N
- Increased leakage
- Reduce cell size

## Peripheral Circuits

- Reduce leakage
- Increased  $I_{STB}$  &  $I_{ACT}$
- Reduce speed variation
- Unreliable operations



# Leakage Currents of Periphery

## ■ Gate tunneling current ( $i_G$ )

- Insensitive to  $V_G$  & temp.
- Sensitive to  $t_{ox}$

1/10  $i_G$ -reduction with  $t_{ox}$ -increment of **only 2-3 Å** for  $\text{SiO}_2$ , while the same reduction with  $V_G$ -decrement of as much as **0.5 V**.

Such a large  $V_G$  control in low- $V_{DD}$  region is risky.

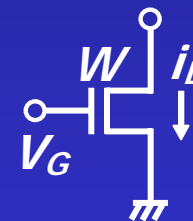
→ Device designers are responsible for the reduction. (High- $k$ )

## ■ Subthreshold current ( $i_L$ )

- Insensitive to device structures
- Sensitive to  $V_G$ ,  $V_T$  & temp that can be controlled by circuits.

1/10  $i_L$ -reduction with  $V_T$ -increment, or  $V_G$ -decrement of **only 100 mV**.

→ Circuit designers are responsible for the reduction.



$$i_L \propto W 10^{(V_G - V_T)/S}$$

$$S \sim 100\text{mV/dec.}@100^\circ\text{C}$$

$$1/10 \text{ with } \Delta V_T = 100\text{mV} \\ \text{or } \Delta V_G = -100\text{mV}$$

# Subthreshold Current ( $i_L$ ) of Periphery

## Features of RAM Periphery

### 1. Input-Predictable Logic

Designers can prepare the schemes in advance.

### 2. Slow Cycle ( $t_{RC} = 25, 60$ ns)

Each circuit is active for only a short period within "long" cycle, enabling additional time for  $i_L$ -control.

### 3. Iterative-Circuit Blocks

Major  $i_L$  sources.

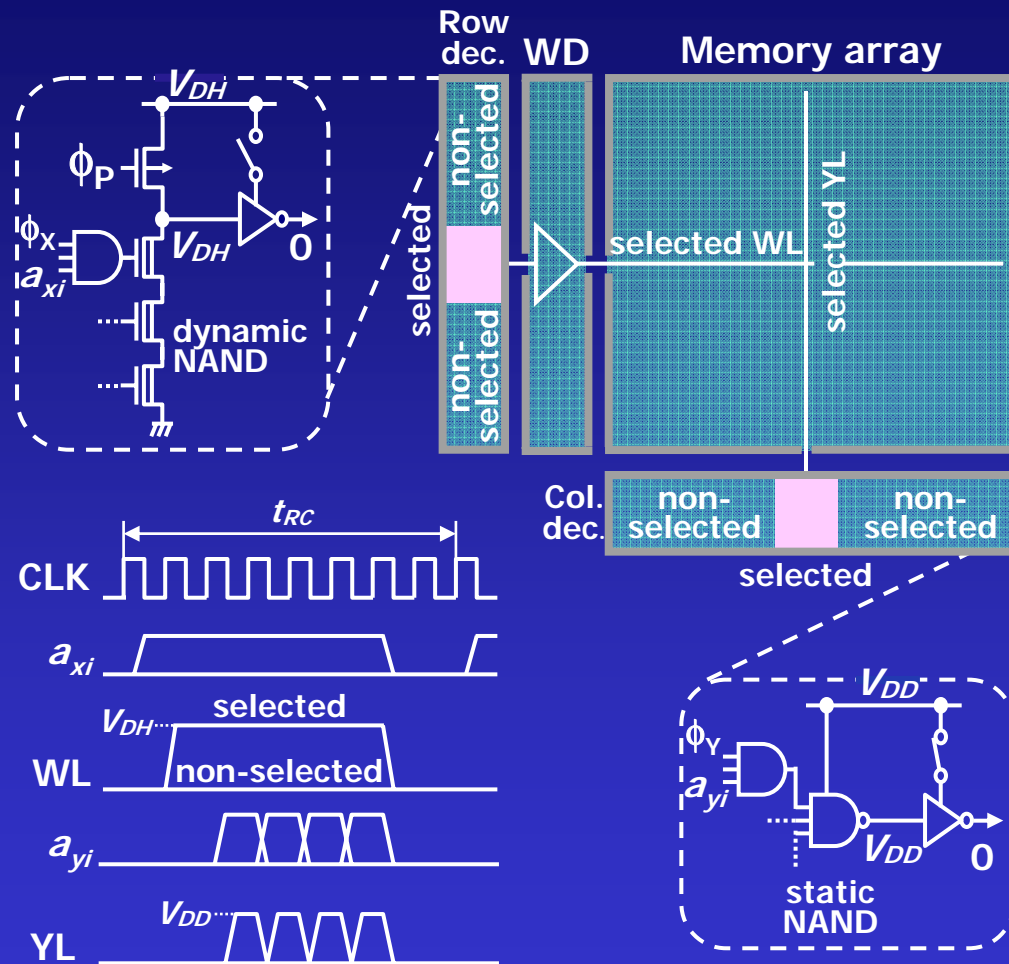
All circuits in each block are inactive, except selected one.

### 4. Robust Circuits

$i_L$ -immune NAND dec.  
(w/o  $i_L$ -sensitive NOR dec.)

### 5. On-Chip Power Supplies

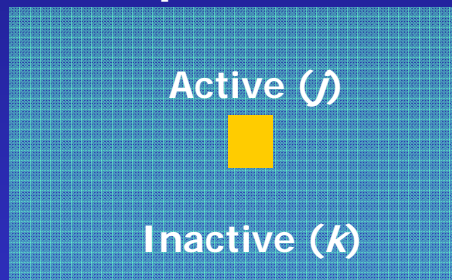
$V_{DH}$  &  $V_{BB}$  utilized for dual-static  $V_T$ .



# $i_L$ -Increase in Periphery

- At present,  $V_T$  is still so high that  $i_L$  is small in active mode, though  $i_L$  dominates in standby mode.
- In the future, with further reducing  $V_T$ ,  $i_L$  will dominate even in active mode. Leakage reduction for active mode is the key.

chip (active)



$$I_{ACT} = I_{AC} + I_{DC}$$

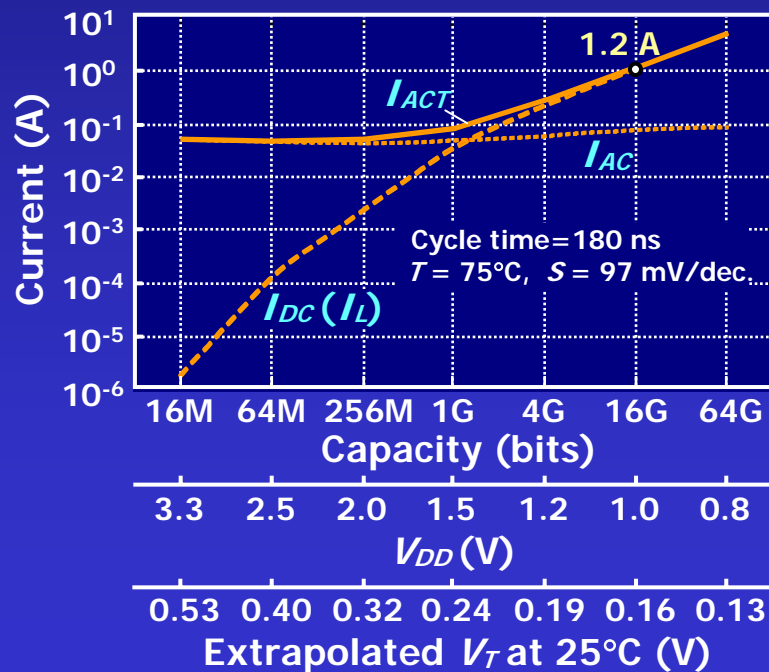
$$I_{AC} = \sum C_j V_{DD} f$$

$$I_{DC} = \sum i_{LK} \propto \sum W_k 10^{-V_T/S}$$

$$V_T = aV_{DD}$$

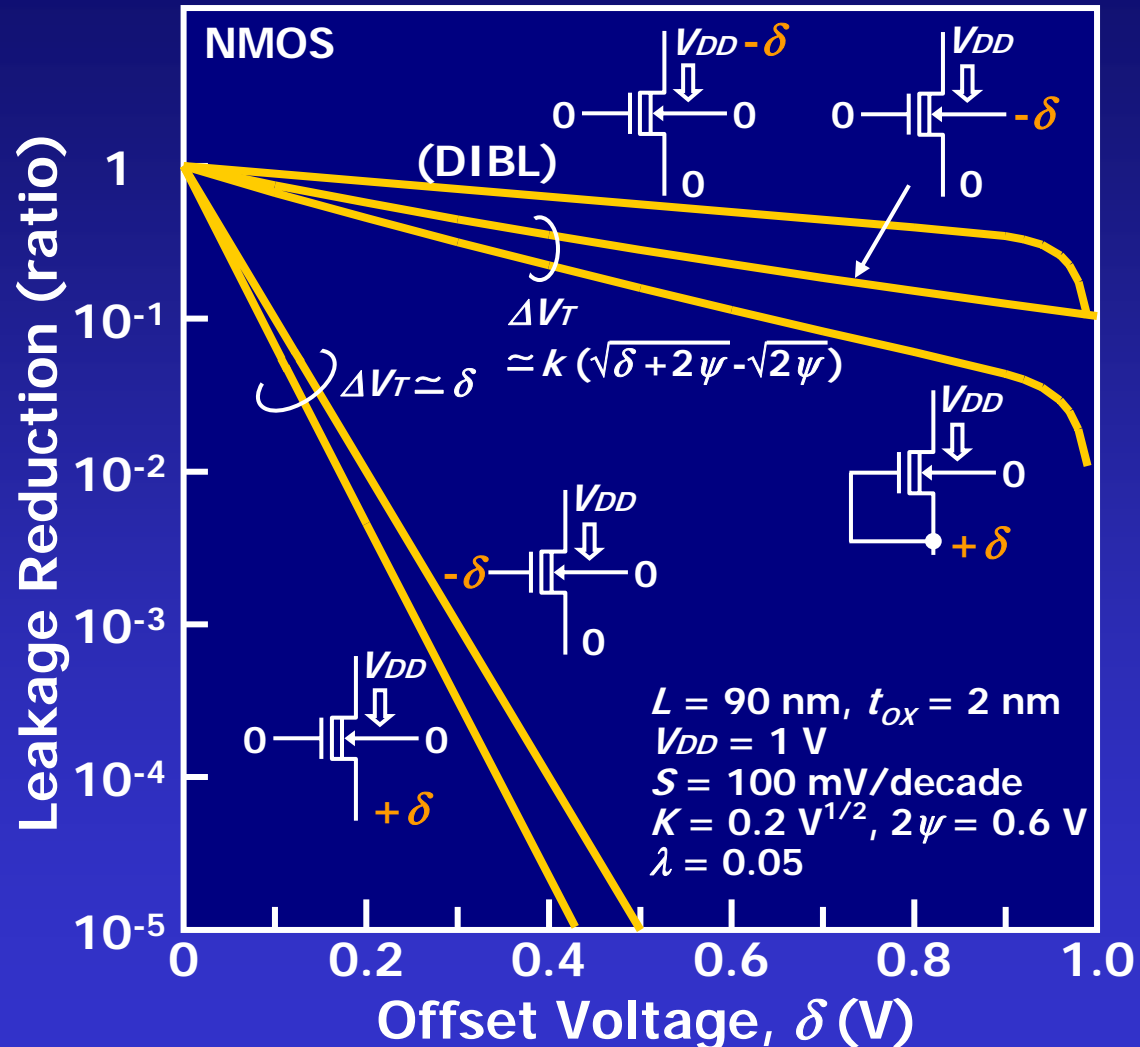
$$k \gg j$$

Trends in DRAM Peripheral Current



# Basic Concept of $i_L$ -Reduction

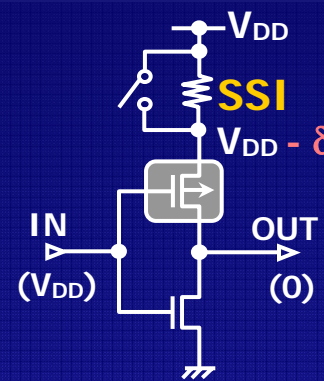
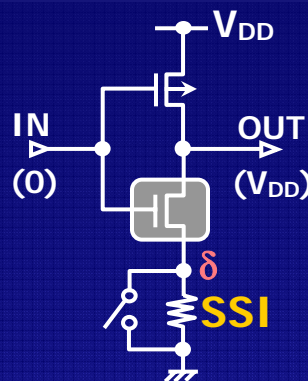
- Use high- $V_T$  MOST achieved statically or dynamically with  $V_{Th} = V_{TI} + \Delta V_T$
- For static high- $V_T$   $\Delta V_T$  by ion impla. or static- $V_{BB}$  application.
- For dynamic high- $V_T$   $\Delta V_T$  by dynamic back-biasing schemes  
**G-S back-bias is best due to large  $\Delta i_L / \Delta \delta$ , applicable even to active mode.**



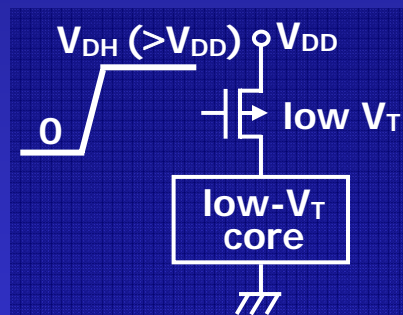
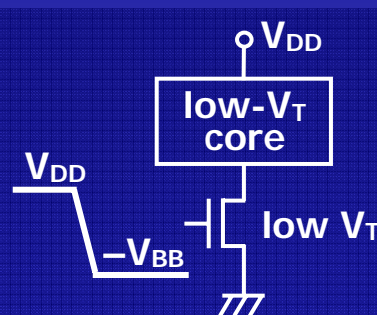
# Three Practical Reduction Circuits

Applicable even to Active Mode

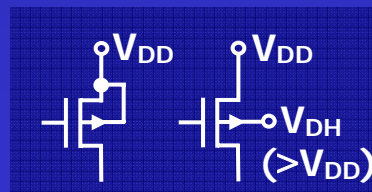
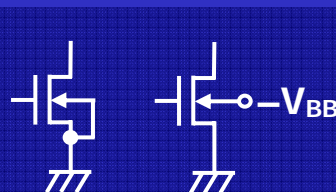
**Switched-Source Imp.**  
(G-S Self-Backbiasing)



**Power Switch utilizing internal power supply (G-S Offset Driving)**



**Dual-Static  $V_T$  utilizing internal power supply**



# SSI (G-S Self-Backbias)

for fast  $i_L$ -control of input predictable logic

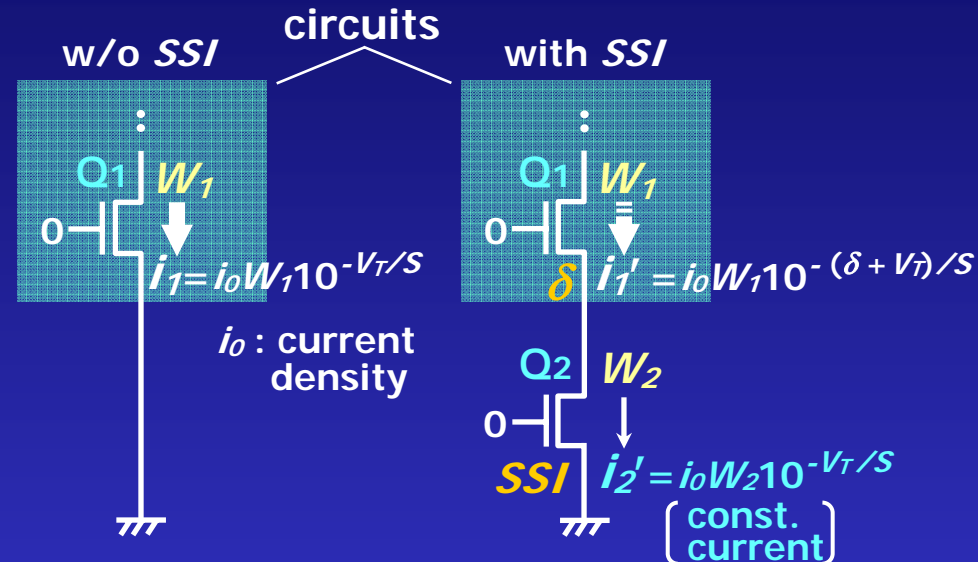
No matter how large  $i_1$  is, it is confined to **const. current**  $i_2'$  with self-adjusting  $\delta$ .

**Stacking effects** ( $\delta = 0.2 \text{ V}$ )

- G-S backbias of Q1 (1/100)
- Sub-S backbias of Q1 (1/1.5)
- DIBL effect of Q2 (1/2)

**Applicable even to active mode**

- Fast  $i_L$ -control capability with small  $\delta$  &  $C_L$  and self-reduction
- Small area penalty if applied to iterative circuit blocks
- Capability of confining to min. active circuitry



$$i_1' = i_2'$$

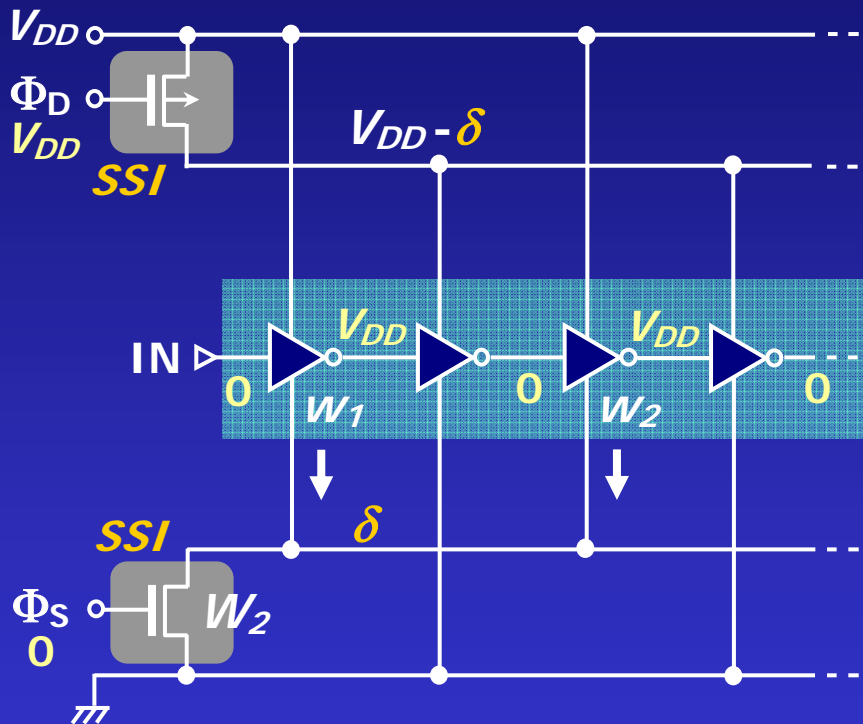
$$\therefore \delta = (S/\ln 10) \ln(W_1/W_2)$$

$$\text{Reduction Ratio } \gamma = i_1'/i_1 = 10^{-\delta/S} = W_2/W_1$$

- Smaller  $i_L$  ( $= i_2'$ ) & larger  $\delta$  with smaller  $W_2$
- $\gamma = 1$  (no reduction) for  $W_2 = W_1$
- Other secondary effects reduce  $i_L$ . (Sub-S backbias & DIBL)

# Small Area Penalty with *SSI* Sharing

## Inverter Chain

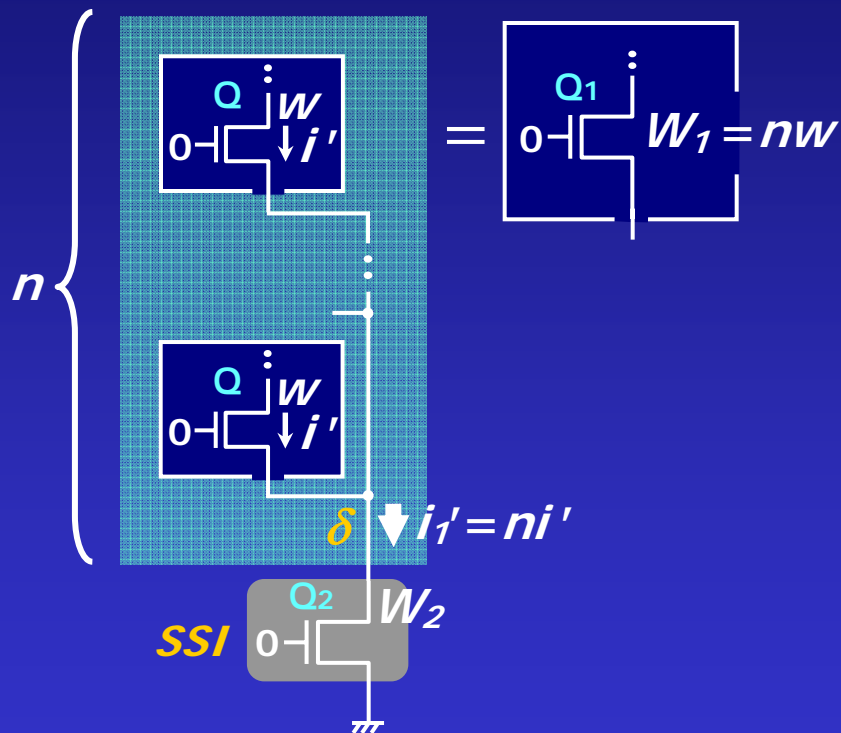


- For 0-V input,  $i_L$  flows from an n-MOST in each 0-V input inverter, and accumulates into *SSI*.
- *SSI* confines to its constant current ( $= i_0 W_2 10^{-V_T/S}$ ).
- $W_2 \cong W_1 \cong \dots \cong W_n$  without speed penalty because each inverter switches at different timing.
- Area penalty is negligible with increasing the number of inverters because  $W_2 \ll \sum W_i$ .

Such is the case for p-MOST *SSI*.

# Small Area Penalty with *SSI* Sharing

## Iterative Circuit Block (non-selected/standby)



- During non-selected periods  $i_L (= i')$  flows from each circuit, and accumulates into *SSI*.
- *SSI* confines to its constant current ( $= i_0 W_2 10^{-V_T/S}$ ).
- $W_2 \cong W$  without speed penalty because **only one MOST is activated with *SSI* on.**
- Area penalty is negligible with  $n \gg 1$  because  $W_2 \ll nw$ .



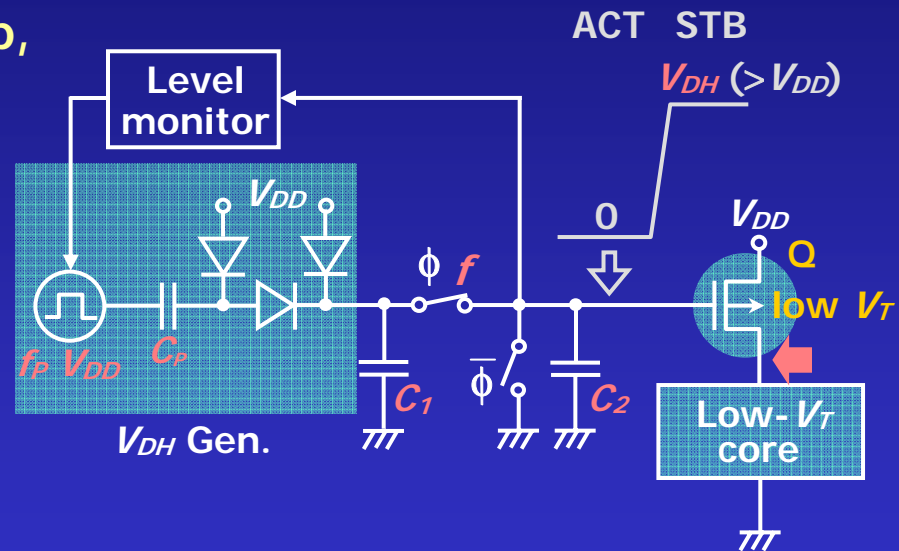
# Power Switch (G-S Offset Drive)

Low- $V_T$  switch (Q) shuts off the supply of low- $V_T$  core during standby. A raised  $V_{DH}$  needed to cut off Q with G-S backbias.

## Problems:

### 1. If $V_{DH}$ generated by charge pump,

- Unregulated floating  $V_{DH}$   
For well-regulated  $V_{DH}$ ,  
 $C_2 V_{DH} f < C_P V_{DD} f_P$ ,  $C_1 \gg C_P$ ,  
 $C_1 \gg C_2$ , level monitor.
- Increased pump power  
For low pump power with  
keeping the  $V_{DH}$  level,  
 $C_P V_{DD} f_P$  &  $C_2 V_{DH} f$  reduced.  
-> Smaller  $C_2$  & slower  $f$



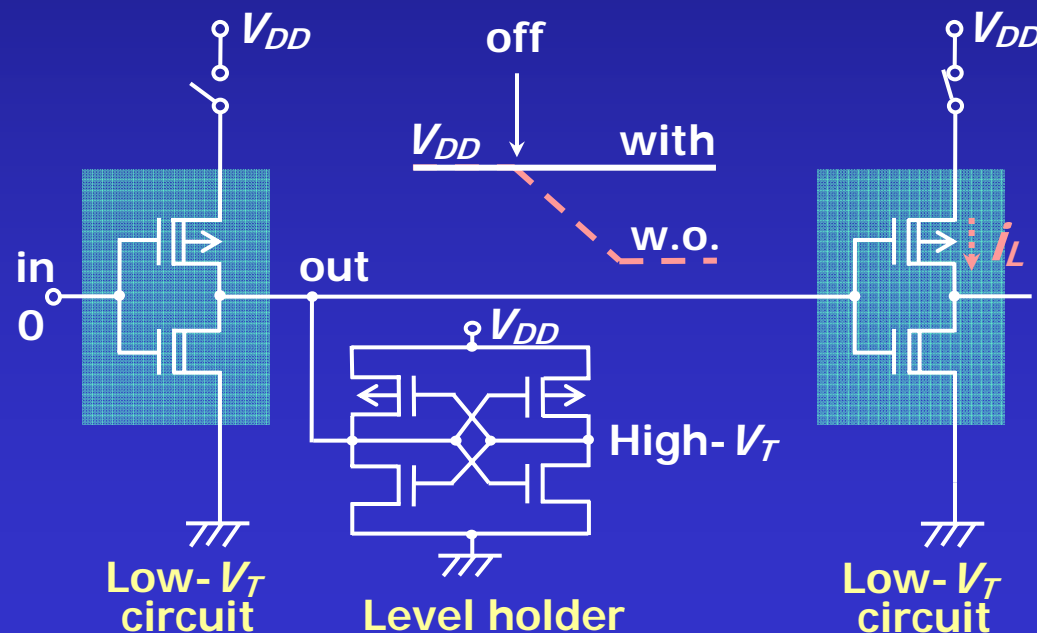
### 2. Area penalty by large Q

### 3. Slow recovery of internal power node (↔)

# Power Switch with Level Holder

Applicable even to active mode, if the switch itself operates fast enough. After evaluating the input, the output level continues to be held by high- $V_T$  holder without leakage. Otherwise

- Floating output discharges, causing a large  $i_L$  at pMOST in the succeeding circuit, in which the switch is still on.
- Unnecessary discharging prevents the output from quick recovery.



# Dual Static $V_T$

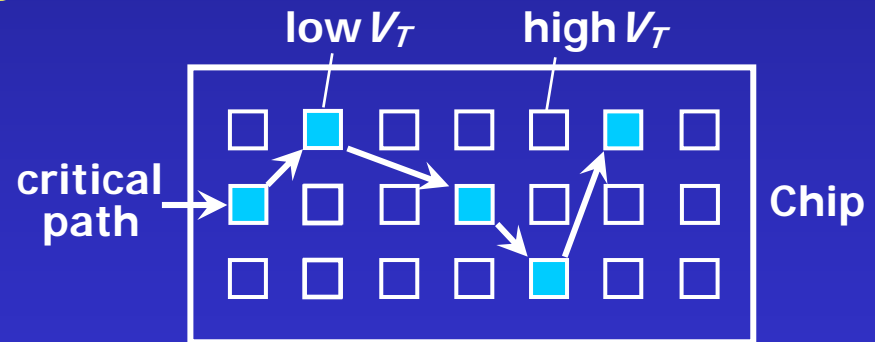
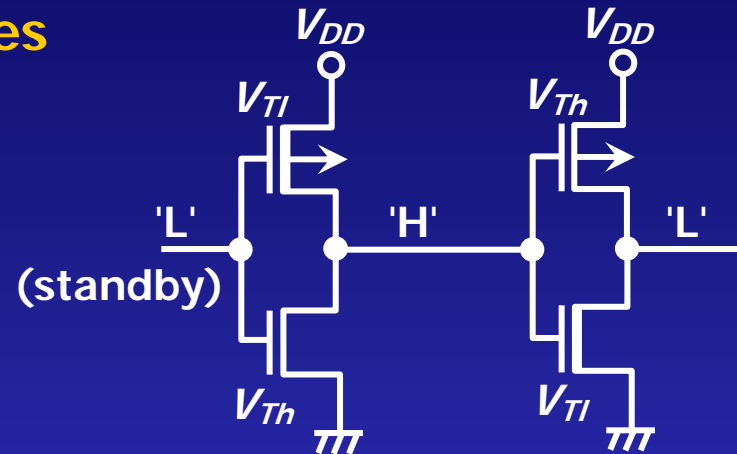
## Useful for active & standby modes

### Selective use of a high $V_T$ to

- Off-MOSTs during standby
  - Non-critical path, while using low  $V_T$  to critical path.
- > Low  $i_L$  & high speed chip

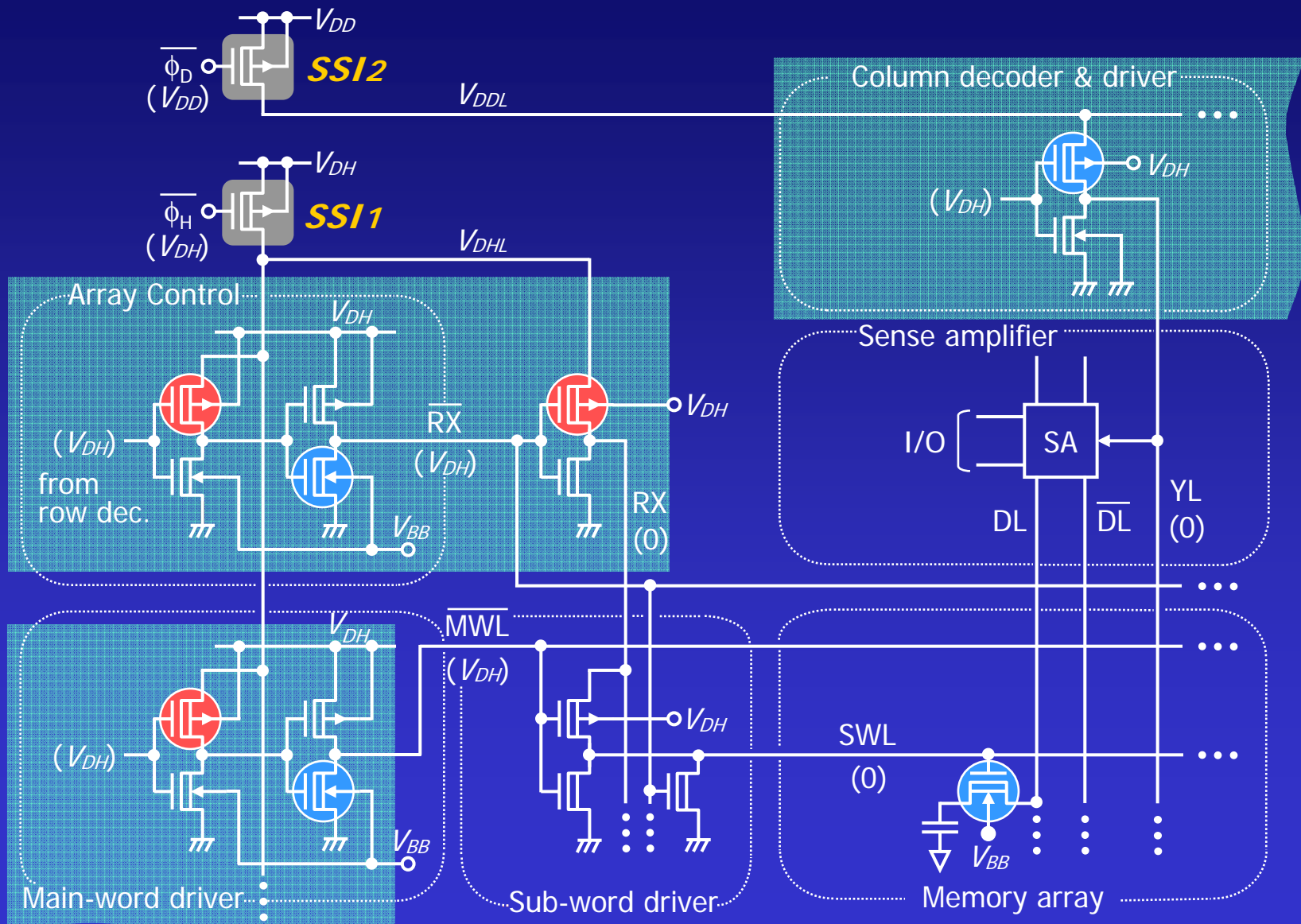
The reduction is not remarkable because  $V_T$  difference must be small.

A large  $V_T$  difference may cause a racing problem: a pulse-timing imbalance between  $V_{TI}$  -&  $V_{Th}$ -circuits.

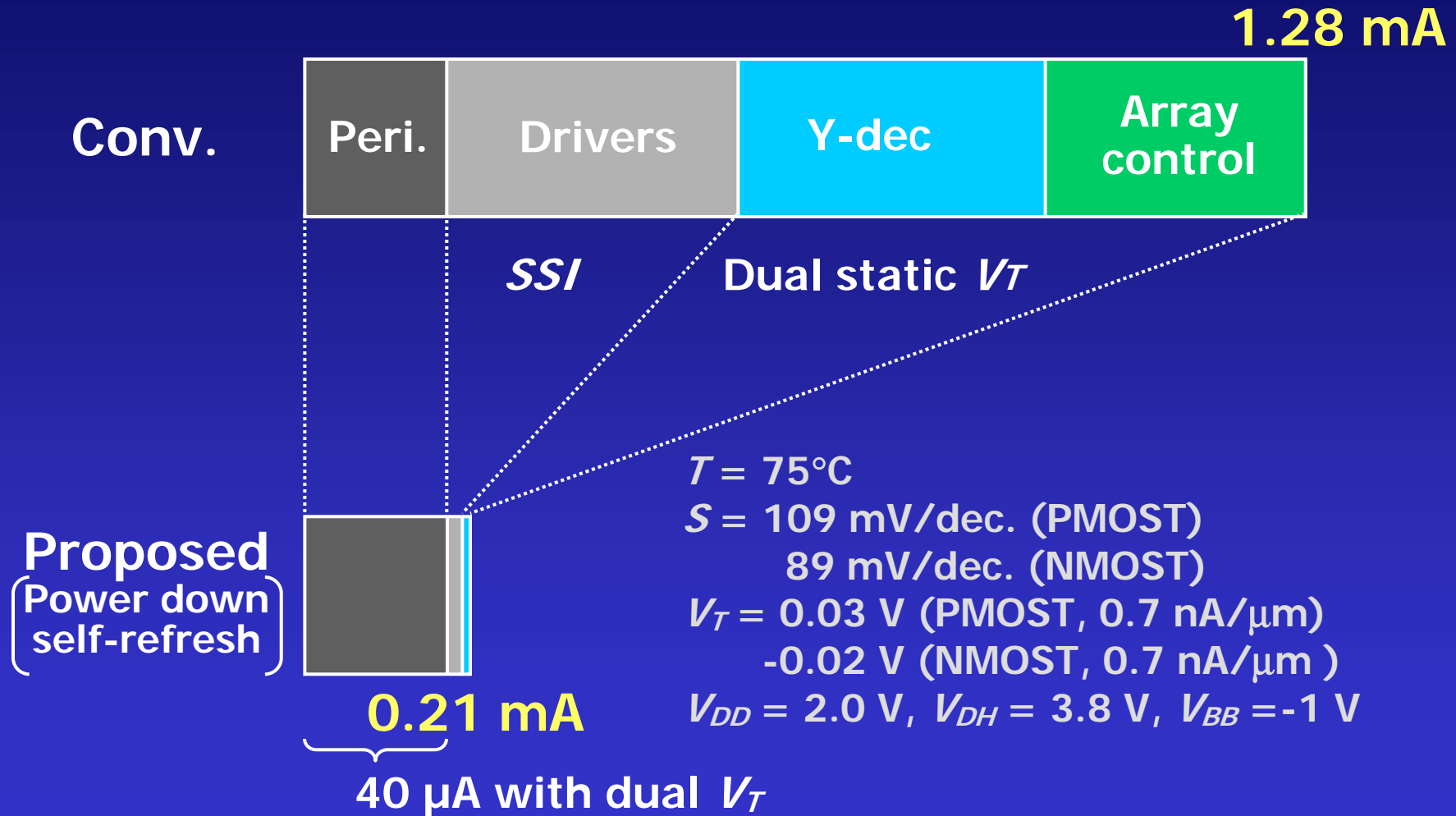


$i_L$  reduced to 1/5 for uniform use of  $V_{TI}$  with assumptions:  
 $W_{total}(\text{critical path}) = 10\%$  of  $W_{total}(\text{chip})$ ,  
 $V_{TI} = 0.21 \text{ V}$ ,  $V_{Th} = 0.31 \text{ V}$ ,  $S = 0.1 \text{ V/dec}$ .

# 256-Mb DRAM (Standby)

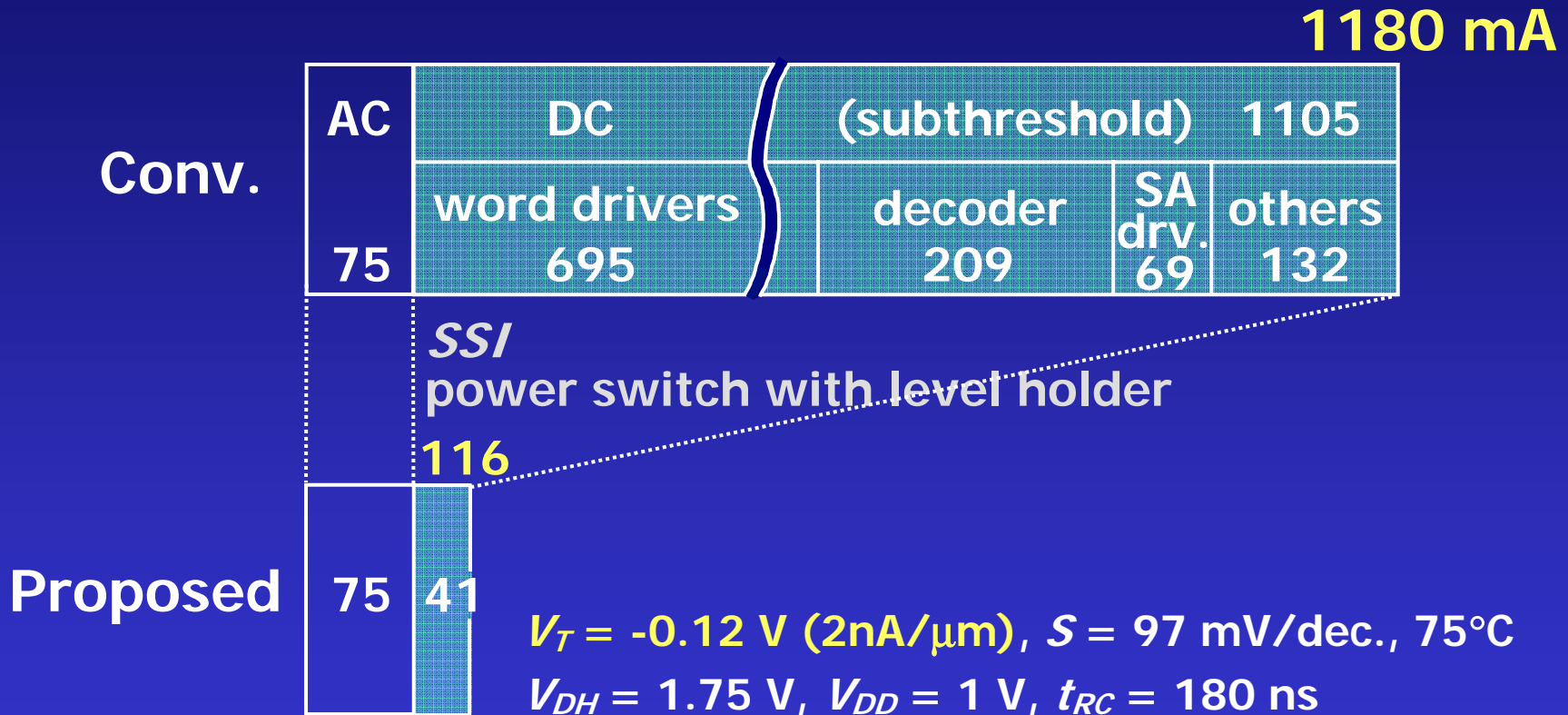


# Standby Current Reduction (256 Mb)



# 1-V 16-Gb DRAM

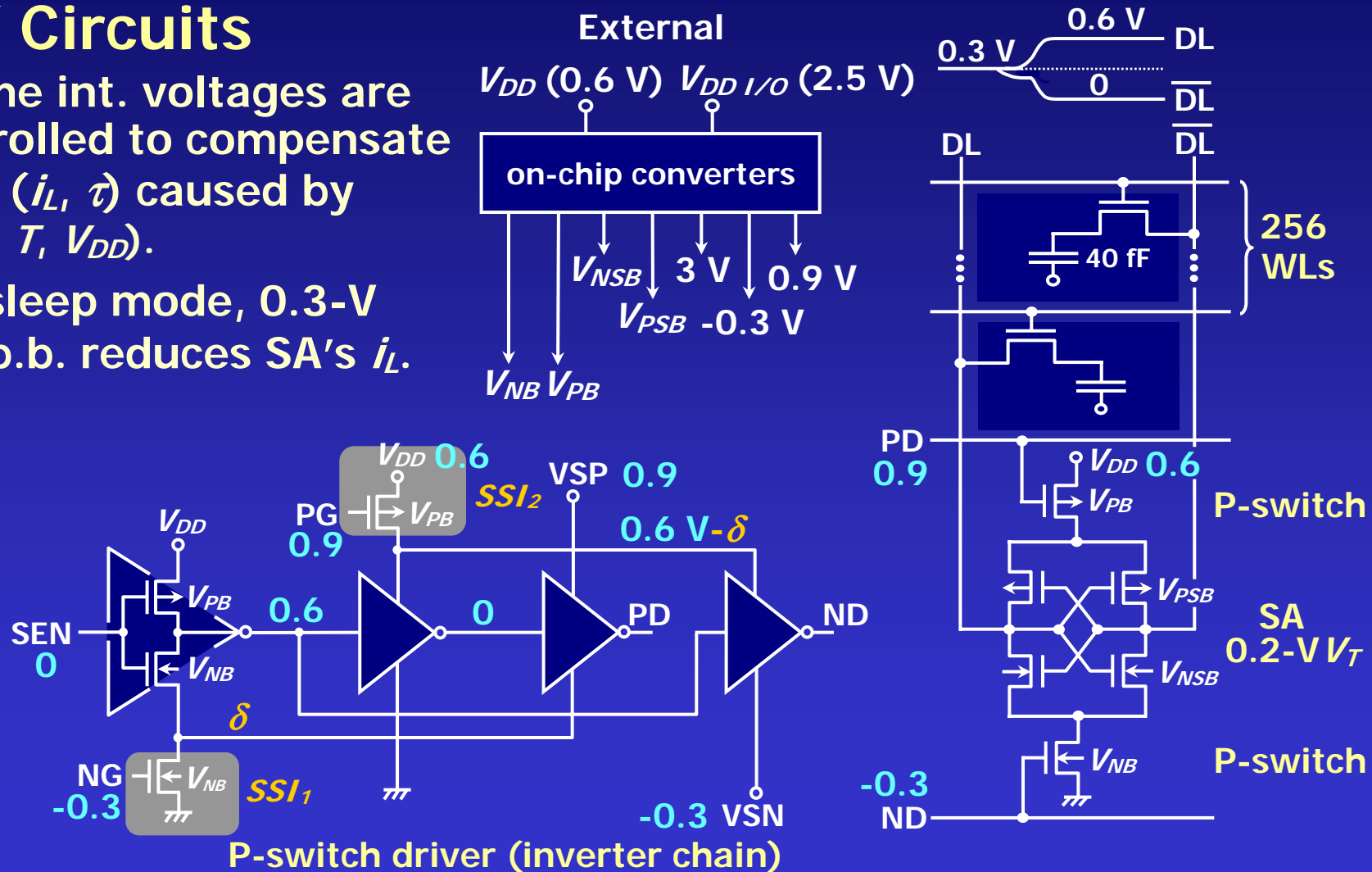
## Active Current Reduction



# 0.6-V 16-Mb e-DRAM

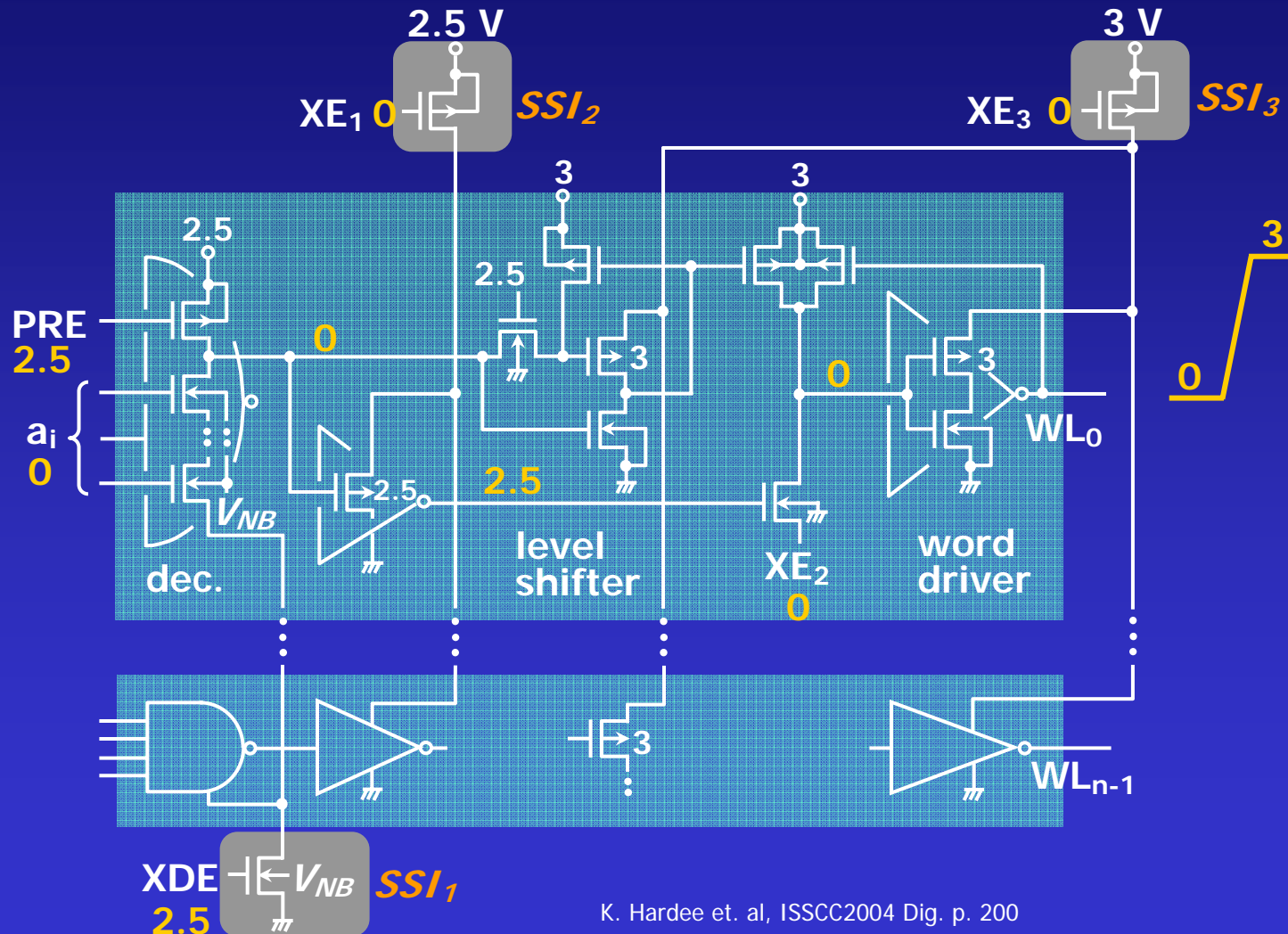
## Y Circuits

- Some int. voltages are controlled to compensate for  $\Delta (i_L, \tau)$  caused by  $\Delta (V_{T_i}, T_i, V_{DD})$ .
- In sleep mode, 0.3-V G-S b.b. reduces SA's  $i_L$ .



# 0.6-V 16-Mb e-DRAM

## X Circuits (Active)

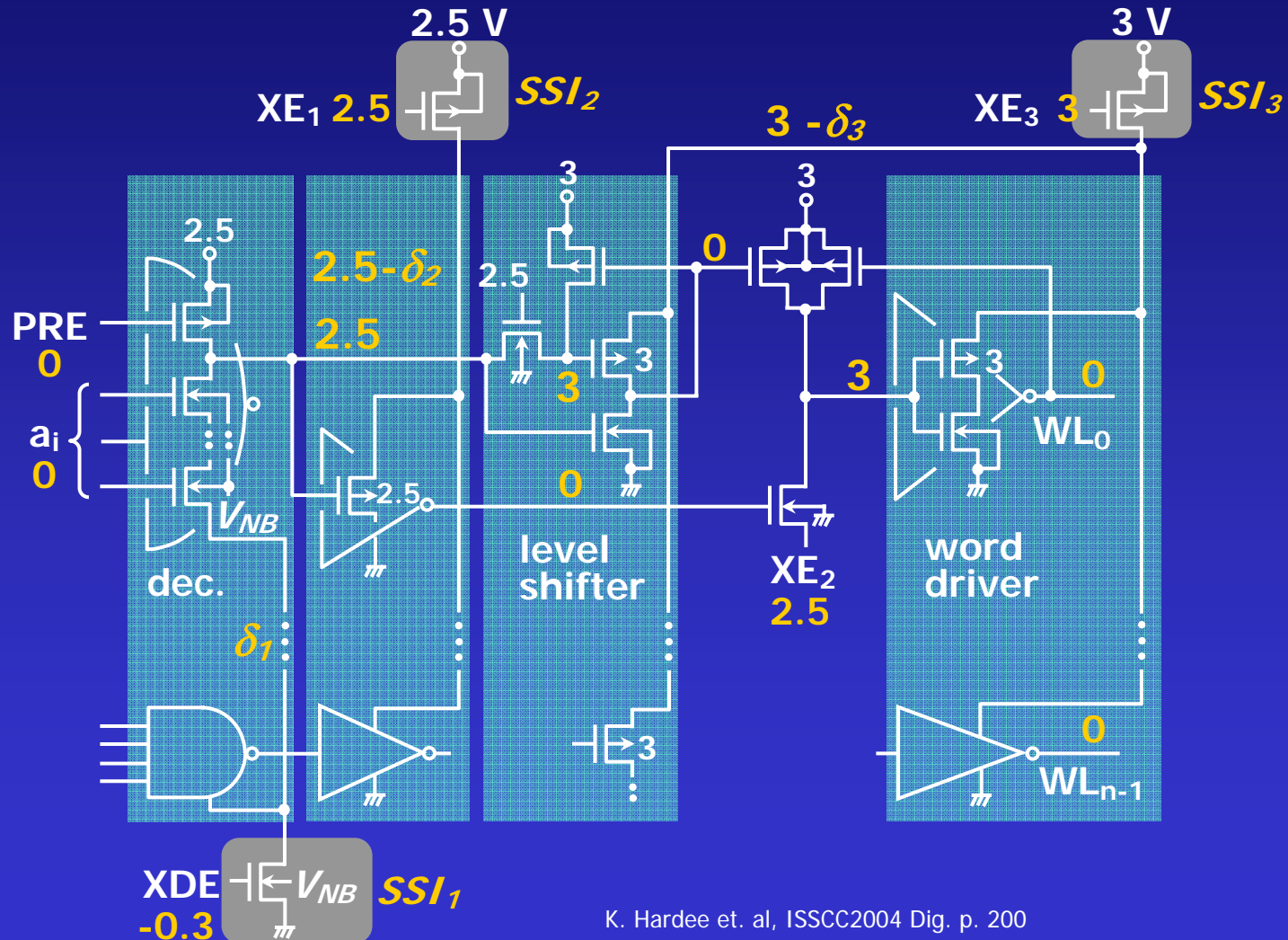


K. Hardee et. al, ISSCC2004 Dig. p. 200

K. Itoh et al., CICC 2004 Dig. Tech. Papers, pp. 339-344, Oct. 2004

# 0.6-V 16-Mb e-DRAM

## X Circuits (Sleep)



K. Hardee et. al, ISSCC2004 Dig. p. 200

K. Itoh et al., CICC 2004 Dig. Tech. Papers, pp. 339-344, Oct. 2004

# 1.2-V 1-Mb e-SRAM

## Multi-Bank Architecture

### Active Mode

4-bank arch. with one-bank activation confines active circuitry to 1/4, and reduces

- AC power of cont. signals
- $i_L$  in inactive banks if  $SSI$  is applied to WD & cells.

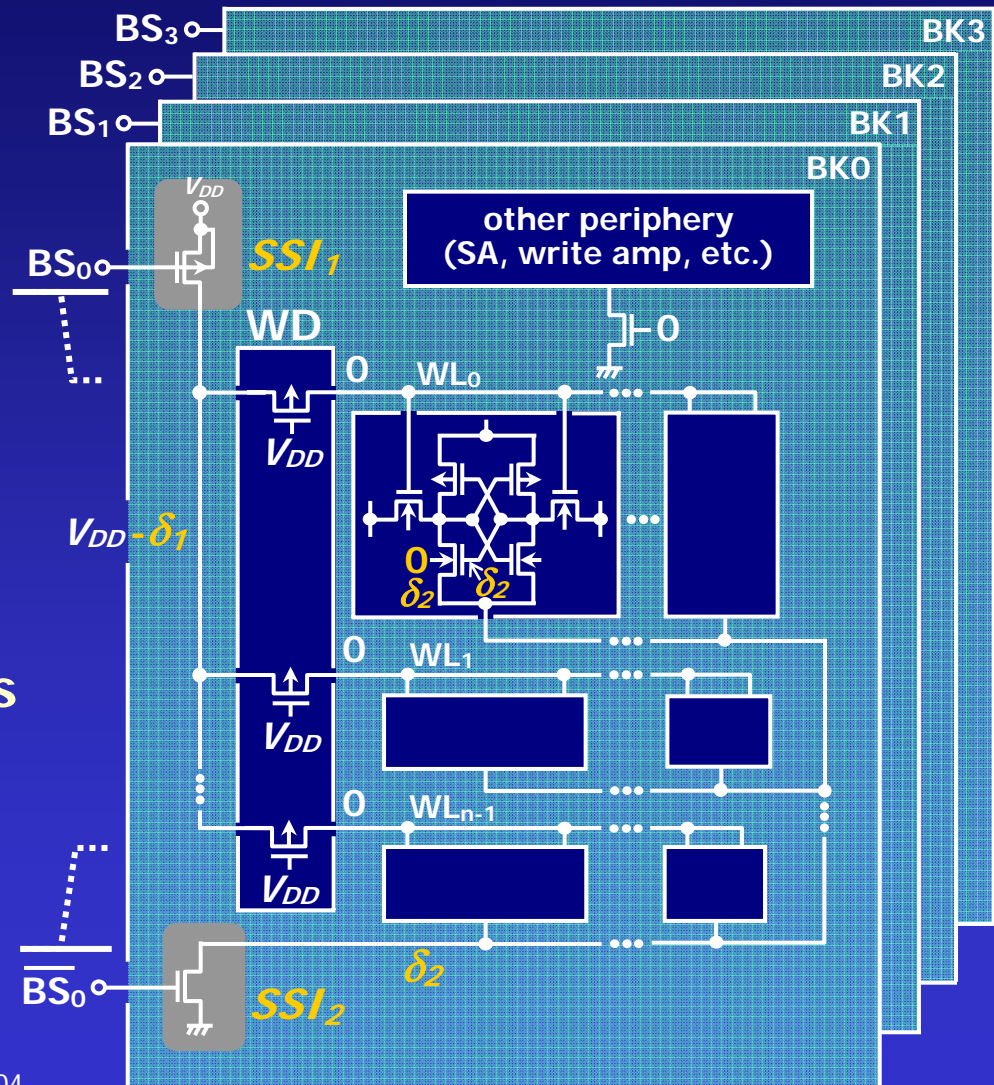
$SSI_1$ : Small  $\delta_1$  &  $C_L \rightarrow 0.3$  ns

$SSI_2$ : Drawbacks;

Large  $\delta_2$  (0.4 V) &  $C_L \rightarrow 3$  ns  
Cell-supply reduced by  $\delta_2$

### Sleep Mode

Periphery off with power switch off  $\rightarrow 3$ ns

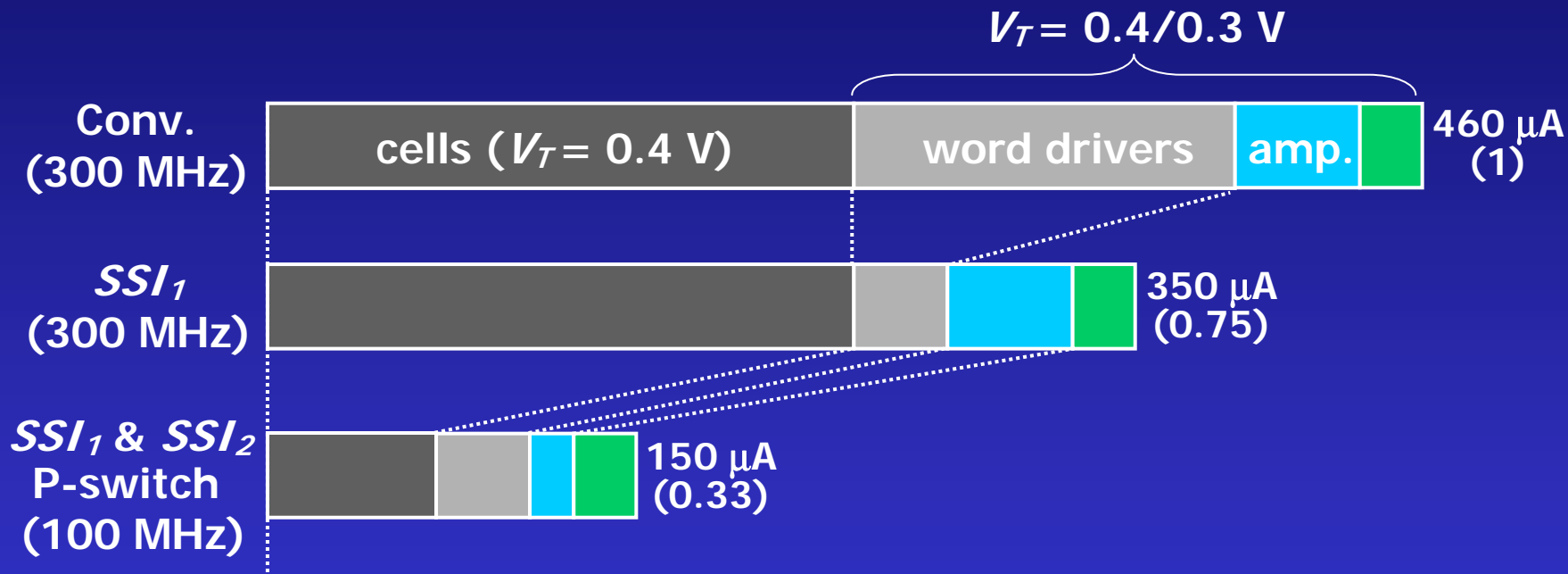


M. Yamaoka et. al., ISSCC2004 Dig. p. 494

K. Itoh et al., CICC 2004 Dig. Tech. Papers, pp. 339-344, Oct. 2004

# Leakage of 1-Mb e-SRAM (Active)

1.2 V, room temp.



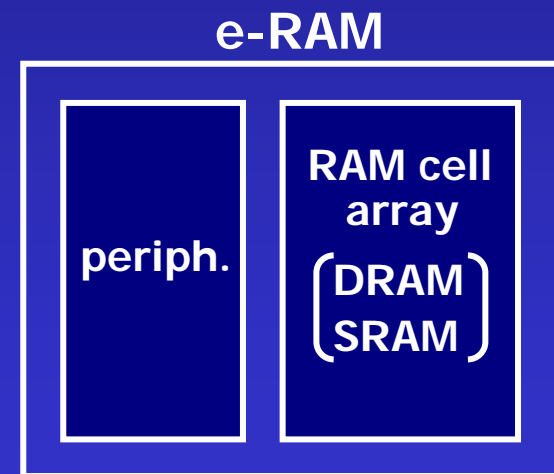
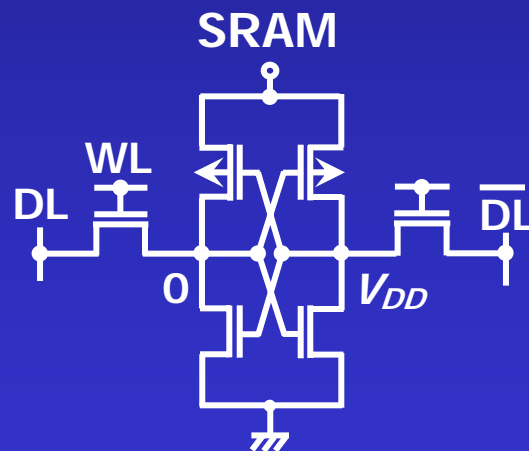
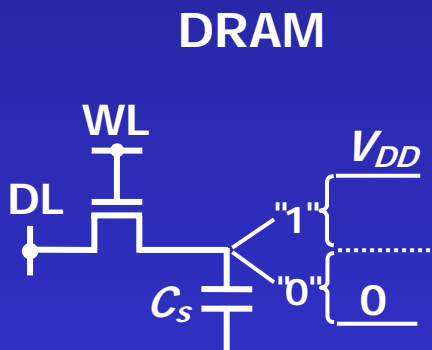
# Challenges to LV e-RAMs

## RAM Cells

- Extend low-voltage limitation to sub-1 V
- Degraded S/N
- Increased leakage
- Reduce cell size

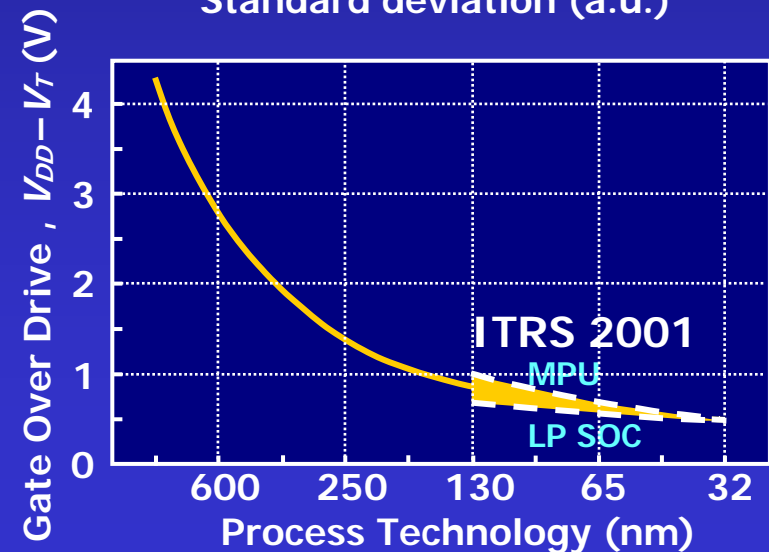
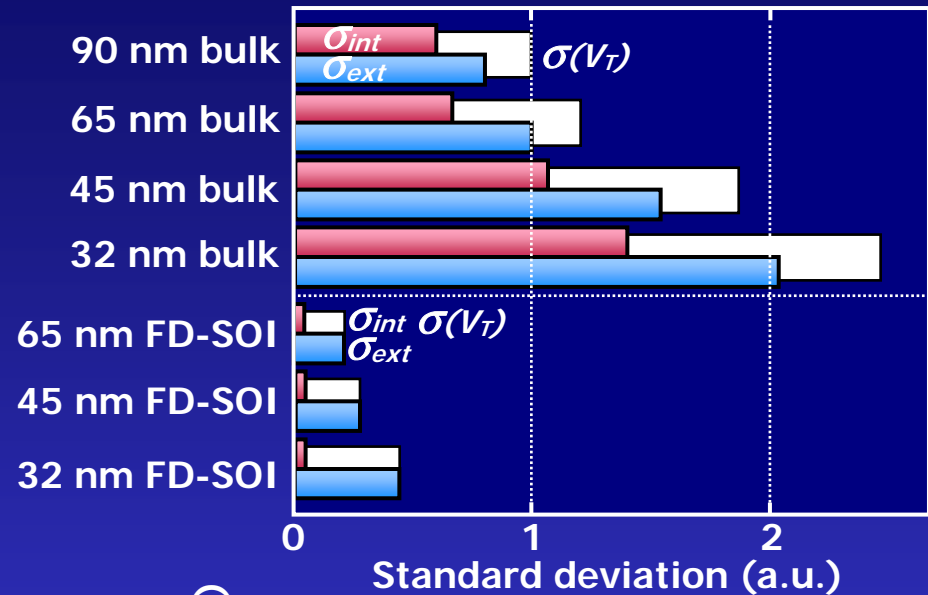
## Peripheral Circuits

- Reduce leakage
- Increased  $I_{STB}$  &  $I_{ACT}$
- Reduce speed variation
- Unreliable operations



# Speed Variation

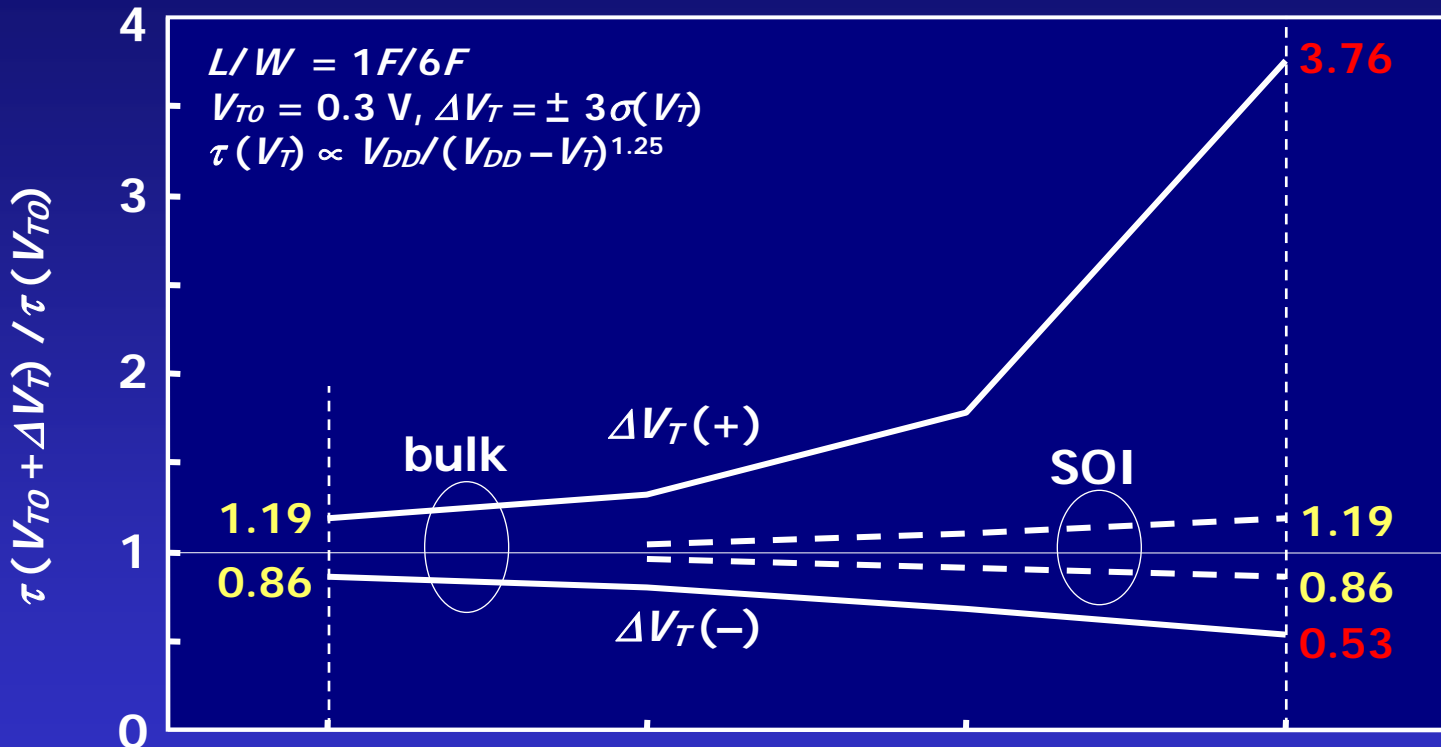
- Ever-increasing  $\Delta V_T$ , and rapidly-lowering gate-over drive with device scaling.
- They enhance speed variation of periphery  
 $\Delta\tau/\tau \propto \Delta V_T/(V_{DD}-V_T)$
- Solutions
  - For inter-die  $\Delta\tau$ , Compensation with  $V_{BB}$  generator. e.g., Speed improvement by 63%
  - For intra-die  $\Delta\tau$ , FD-SOI





# Intra-Die Speed Variation

## Low-Power CMOS LSIs



$F$ (nm)	90	65	45	32
$V_{DD}$ (V) (ITRS'03)	0.9	0.8	0.7	0.6
$\sigma(V_T)$ bulk (ratio)	1	1.29	1.89	2.51
$\sigma(V_T)$ SOI (ratio)	—	0.23	0.38	0.50

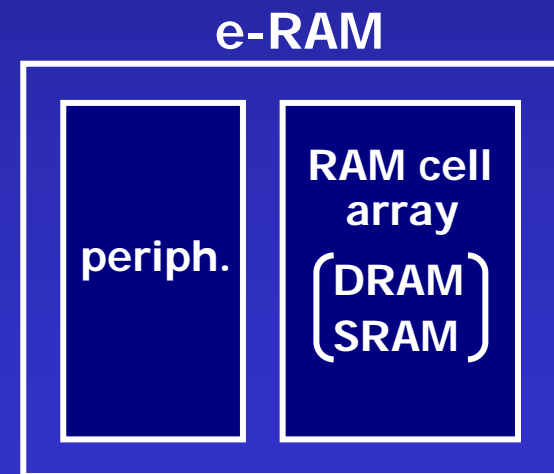
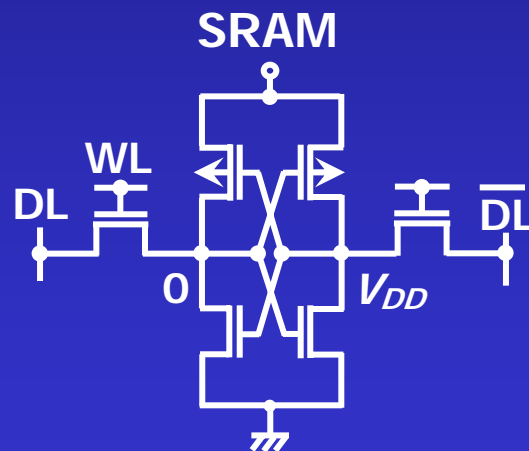
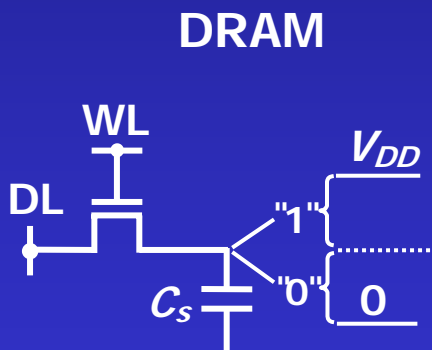
# Challenges to LV e-RAMs

## RAM Cells

- Extend low-voltage limitation to sub-1 V
- Degraded S/N
- Increased leakage
- Reduce cell size

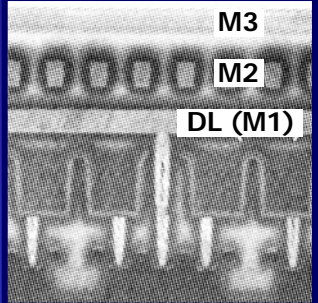
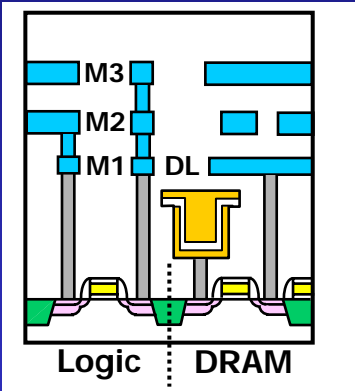
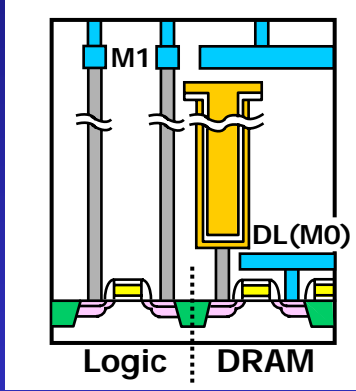
## Peripheral Circuits

- Reduce leakage
- Increased  $I_{STB}$  &  $I_{ACT}$
- Reduce speed variation
- Unreliable operations



# RAM Cells (DRAM)

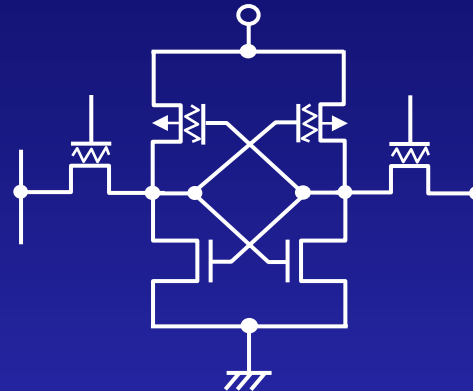
**Short DL** allows a small  $C_S$  & simple  $C_S$ -structure with small  $C_D$ .  
**Planar- $C_S$  cell might replace e-SRAM cells.**  $V_{sig} \cong C_S / C_D \cdot V_{DD} / 2$ .  
 In addition, short DL enables low- $V_{DD}$  fast operation.

	proposed (ISSCC2005)	conventional
		
Cells/DL $C_S$ Additional wire Thermal budget Cell $RC$ delay Cell contact $R$	<b>32</b> <b>5 fF</b> ( $Ta_2O_5$ ; MIM) No no impact on logic W storage cont. Co-salicyded S/D 10 $\Omega$	128 $\geq 15$ fF (MIS) local wire (M0) intolerable impact Non-metalized cell 10 k $\Omega$

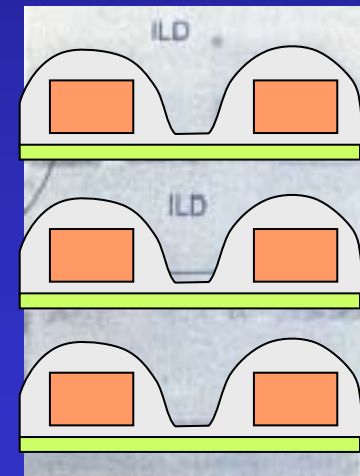
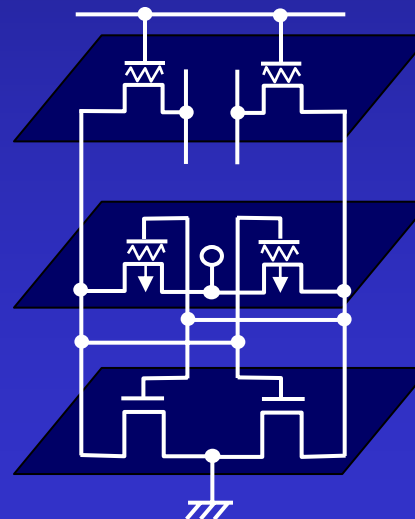
# Cell Size Reduction (6-T SRAM Cell)

## Stacked TFT SRAM Cells

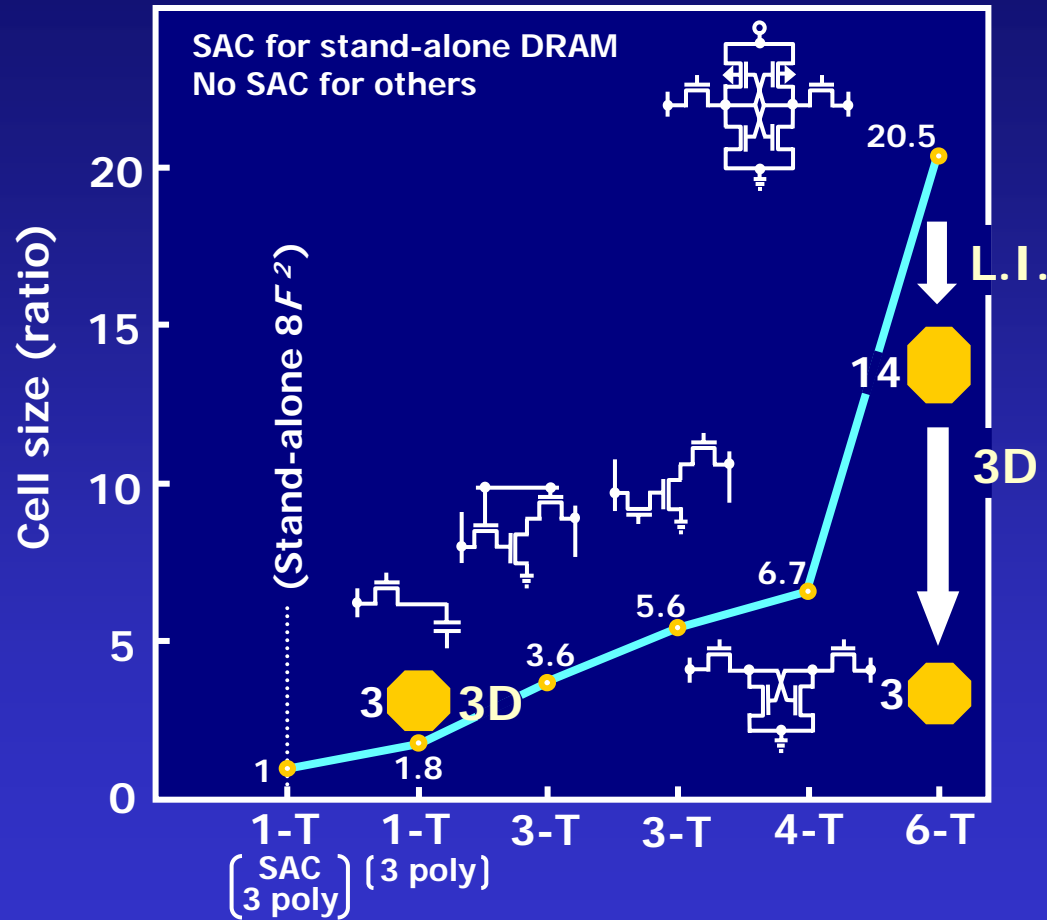
- **Single-crystal TFT**  
The highest density cell ( $25F^2$ ) comparable to DRAM cells.  
1.8-V 61.1- $\mu\text{m}^2$  144-MHz  
256-Mb SRAM.
- **Drawbacks as e-SRAMs**  
Sophisticated process,  
High- $V_{DD}$  operation  
due to TFT PMOST of  
 $S = 140 \text{ mV/dec.}$ ,  
 $I_{DS} = 2/3$  of the bulk.



Load p-TFTs & transfer n-TFTs double-stacked over bulk driver n-MOSTs in different levels of layers.



# Cell-Size Comparisons



# Future Prospects for RAMs

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**6-T SRAM Cell:** Due to high necessary  $V_T$  & large  $\Delta V_T$

- Not suitable for sub-1-V  $V_{DD}$ ,
- Continue to be used for a high  $V_{DD}$  ( $\geq 1$  V).

Challenge; Small- $\Delta V_T$  MOSTs. TFT cells for stand-alone SRAMs.

**1-T DRAM Cell:** • Suitable even for sub-1-V  $V_{DD}$ .

Challenges; Planar capacitors, Small- $\Delta V_T$  MOSTs.

**Peripheral Circuits:**

- Subthreshold-currents will be reduced sufficiently with existing techniques even for active mode.
- Speed variations will continue to be serious.

Challenges;  $V_{BB}$  control, Small- $\Delta V_T$  MOSTs.

**Two Approaches:**

High- $V_{DD}$  bulk-CMOS for low-cost RAMs,

Low- $V_{DD}$  FD-SOI for high-speed low-power RAMs.

# Conclusion

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1. I discussed challenges and trends in LV RAMs.
2. I reviewed state-of-the-art LV RAM circuits.
3. I gave prospects of RAMs with emphasis on further needs for
  - Ultra-low voltage RAM cells,
  - Advanced devices & circuits to reduce speed variations.