Loopback Architecture for Wafer-Level At-Speed Testing of Embedded HyperTransport™ Processor Links

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Outline

- Motivation
- HyperTransport™ Overview
- Loopback Implementation
  - Architecture
  - Loopback Channel
  - Transmitter
  - Receiver
- Silicon Results
- Conclusion
Motivation

- Processor dies now talk with each other using full-duplex, bidirectional point-to-point links
  - High-bandwidth, low-latency communication
  - Scalable vs. common FSB architecture
  - e.g., HyperTransport™ (HT) in AMD products

- I/O ports per die is increasing
  - Higher socket counts → more board connectivity
  - MCM embedded links → more package connectivity

- Cost benefit is increasing to sort for functional I/O before packaging, especially for MCMs

- Implement on-chip I/O loopback for low-cost at-speed wafer-level testing
Die-to-Die Processor Communication

- PCB – max 30” trace + 2 connectors
- MCM substrate – 4” trace
HyperTransport™ (HT) Overview

- **Source synchronous**
  - Forward half-rate clock for RX data retiming
  - Common-mode jitter rejection, low latency

- **0.4 to 6.4Gb/s (0.4Gb/s steps) – NRZ PAM-2**

- **20 lanes per direction (split into 2 sublinks)**
  - 1 CLK & 9 data (CAD/CTL) lanes per sublink

- **HT1 (0.4–2.0Gb/s)**
  - CDR bypassed, data RX simply retimed by CLK RX

- **HT3 (2.4–6.4Gb/s)**
  - DLL-based CDR aligns received forwarded CLK to received data transitions for lower BER retiming
HT Link Training (Handshaking)

- Coordinated by NB-IOC in both dies
- Each NB-IOC sends predefined training pattern to the other die
- Training arms CDR to align clock to data & signals start of data transfer
- # data lanes enabled depends on link traffic
HT Data Transfer

- Data transfer starts immediately after last bit of training

- Once data transfer is completed, HT port is disabled into one of several possible sleep states for power saving

- Data is scrambled by XOR or by 8b/10b to reduce ISI
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Enabling Internal Serial Loopback

- TX→RX serial loopback via on-chip channel
- No external channel required, hence test can be performed at wafer-level sort
- NB-IOC initiates link by sending training bits, then user-specified test pattern
- RX is *self-trained* using bits sent by own TX
- Controlled by JTAG
Sublink0 Loopback

Training Pattern & Test Pattern (NB-IOC)

TX Sublink Select

RX Sublink Select

Bit Error Counters (NB-IOC)

HT Port

On-Chip Loopback Channels

RX Sublink

Select

TX Sublink

Select

RX-CLK0
RX-CLK1
RX-CLK0
RX-CLK1
TX-CLK0
TX-CLK1
TX-CLK0
TX-CLK1
TX-CTL0
TX-CTL1
TX-CTL0
TX-CTL1
TX-CAD0
TX-CAD8
TX-CAD0
TX-CAD8
TX-CAD1
TX-CAD9
TX-CAD1
TX-CAD9
TX-CAD2
TX-CAD10
TX-CAD2
TX-CAD10
TX-CAD3
TX-CAD11
TX-CAD3
TX-CAD11
TX-CAD4
TX-CAD12
TX-CAD4
TX-CAD12
TX-CAD5
TX-CAD13
TX-CAD5
TX-CAD13
TX-CAD6
TX-CAD14
TX-CAD6
TX-CAD14
TX-CAD7
TX-CAD15
TX-CAD7
TX-CAD15
RX-CAD0
RX-CAD8
RX-CAD0
RX-CAD8
RX-CAD1
RX-CAD9
RX-CAD1
RX-CAD9
RX-CAD2
RX-CAD10
RX-CAD2
RX-CAD10
RX-CAD3
RX-CAD11
RX-CAD3
RX-CAD11
RX-CAD4
RX-CAD12
RX-CAD4
RX-CAD12
RX-CAD5
RX-CAD13
RX-CAD5
RX-CAD13
RX-CAD6
RX-CAD14
RX-CAD6
RX-CAD14
RX-CAD7
RX-CAD15
RX-CAD7
RX-CAD15
Sublink1 Loopback

Training Pattern & Test Pattern (NB-IOC)

TX Sublink Select

RX Sublink Select

Bit Error Counters (NB-IOC)

TX-CLK0  RX-CLK0
TX-CLK1  RX-CLK1
TX-CTL0  RX-CTL0
TX-CTL1  RX-CTL1
TX-CAD0  RX-CAD0
TX-CAD8  RX-CAD8
TX-CAD1  RX-CAD1
TX-CAD9  RX-CAD9
TX-CAD2  RX-CAD2
TX-CAD3  RX-CAD3
TX-CAD10 RX-CAD10
TX-CAD11 RX-CAD11
TX-CAD4  RX-CAD4
TX-CAD12 RX-CAD12
TX-CAD5  RX-CAD5
TX-CAD13 RX-CAD13
TX-CAD6  RX-CAD6
TX-CAD14 RX-CAD14
TX-CAD7  RX-CAD7
TX-CAD15 RX-CAD15

HT Port

On-Chip Loopback Channels
Transceiver Loopback Floorplan

Sublink 0 (CLK0, CTL0, CAD0–7)
Sublink 1 (CLK1, CTL1, CAD8–15)

On-Chip Loopback Channel

Horizontal HT Port shown
Wafer-Level Testing

LTX Sapphire platform

probe tower

probe card

pogo interposer

contact bumped wafer
Wafer-Level Test Supply Noise

- Comes primarily from TX driver switching high currents through probe card pin inductance
- Can disable any TX driver per sublink during loopback

 Probe Card Pin Model

\[
\begin{align*}
0.05\Omega & \quad 0.05\text{pF} \\
3.2\text{nH} & \quad 
\end{align*}
\]

Simulated with 1, 8 & 16 TX drivers enabled

Bump Supply Voltage (V)

Time (µs)

6.00 6.02 6.04 6.06 6.08 6.10

1.4 1.3 1.2 1.1 1.0
- 4-tap FFE
- Hybrid V-/I-mode output driver
RX Loopback Implementation

- Full-rate architecture
- Equalization: 1-bit speculative DFE + analog DFR filter
External Serial Loopback

- Package-level sort test
- Provides test coverage not exercised by internal serial loopback
  - TX output driver
  - RX analog front end
  - TX & RX equalization
- Can inject jitter into external channel for eye margining
Parallel Loopback Modes

- Package-level sort test
- RX→TX parallel loopback in HT or in NB-IOC
- Requires another HT port or BERT to initialize link & provide test pattern to RX
- Enables fault isolation
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Loopback Test Description

- **Wafers**
  - 12” bumped AMD Opteron™ 6000 processors (45nm SOI-CMOS)

- **Test conditions**
  - 1.1V, 1.3V
  - 5.2Gb/s, 6.4Gb/s

- **Test pattern**
  - $10^8$ cycles of alternating $+K_{28.5}$ & $-K_{28.5}$
  - Passing test $\Rightarrow$ BER $< 5 \times 10^{-10}$

Conway et al., Hot Chips 2009
# Early Example of Test Sort Results

<table>
<thead>
<tr>
<th>Die No.</th>
<th>HT Loopback Fail Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Port3 Sublink0 @ 6.4Gb/s – 1.1V&lt;br&gt;CAD2 bit error count = 63 (saturated)</td>
</tr>
<tr>
<td>2</td>
<td>Port0 Sublink0 @ 6.4Gb/s – 1.1V&lt;br&gt;CAD2 bit error count = 2</td>
</tr>
<tr>
<td>3</td>
<td>Port0 Sublink0/Sublink1 @ 5.2,6.4Gb/s – 1.1,1.3V&lt;br&gt;Training failure in all CTL/CAD lanes</td>
</tr>
<tr>
<td>4</td>
<td>Port0 Sublink0 @ 6.4Gb/s – 1.1,1.3V&lt;br&gt;CAD2 bit error count = 63 (saturated)</td>
</tr>
<tr>
<td>5</td>
<td>Port3 Sublink0 @ 6.4Gb/s – 1.1V&lt;br&gt;CAD4 bit error count = 63 (saturated)</td>
</tr>
<tr>
<td>6</td>
<td>Port0 Sublink0 @ 6.4Gb/s – 1.1V&lt;br&gt;CAD0 bit error count = 2</td>
</tr>
<tr>
<td>7</td>
<td>Port2 Sublink0 @ 6.4Gb/s – 1.1V&lt;br&gt;CAD4 bit error count = 63 (saturated)</td>
</tr>
</tbody>
</table>
Conclusion

- Transceiver loopback enables wafer-level at-speed testing of HyperTransport I/O
- Demonstrated 6.4Gb/s test functionality
- Entirely digital architecture for simple implementation & verification
- Significantly improves package-level yield, especially for more expensive MCM packages
- Adds no extra sort infrastructure cost
- Established test for wafer-level screen of AMD 45nm products
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