Radiation Hardened Electronics for Space Systems

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The Aerospace Corporation
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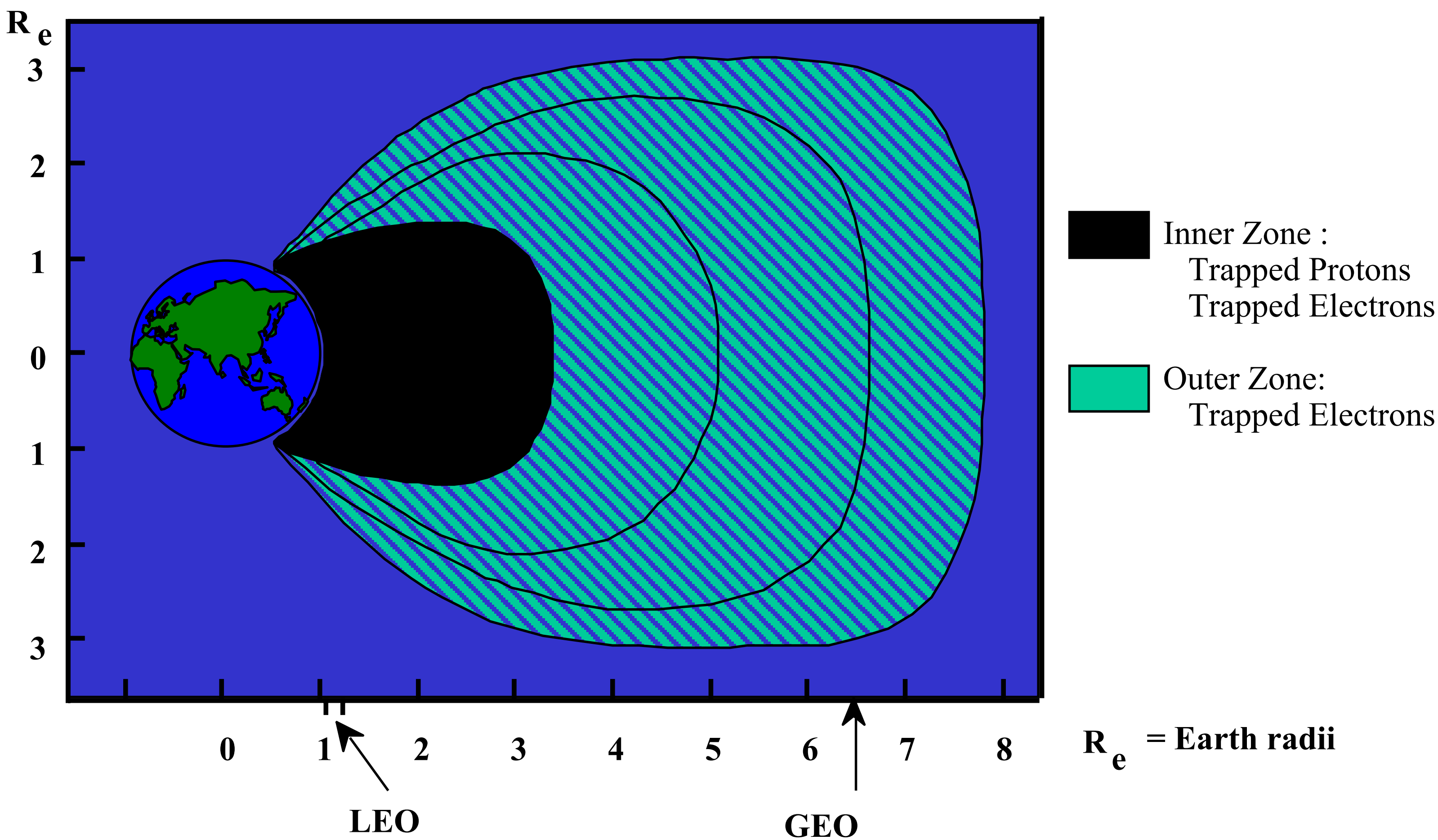
- Don Mayer, Aerospace

Outline

- Introduction to Radiation Environments
- Radiation Effects and Hardening Methods
  - on Electronics
  - of Satellites
- Radiation Hardened Electronics
  - Past
  - Present
  - Efforts by the Government to Support Radiation Hardened Electronics
- Radiation Hardened Electronics Oversight Council (RHOC) Technology Roadmaps
- Summary

RADIATION ENVIRONMENT



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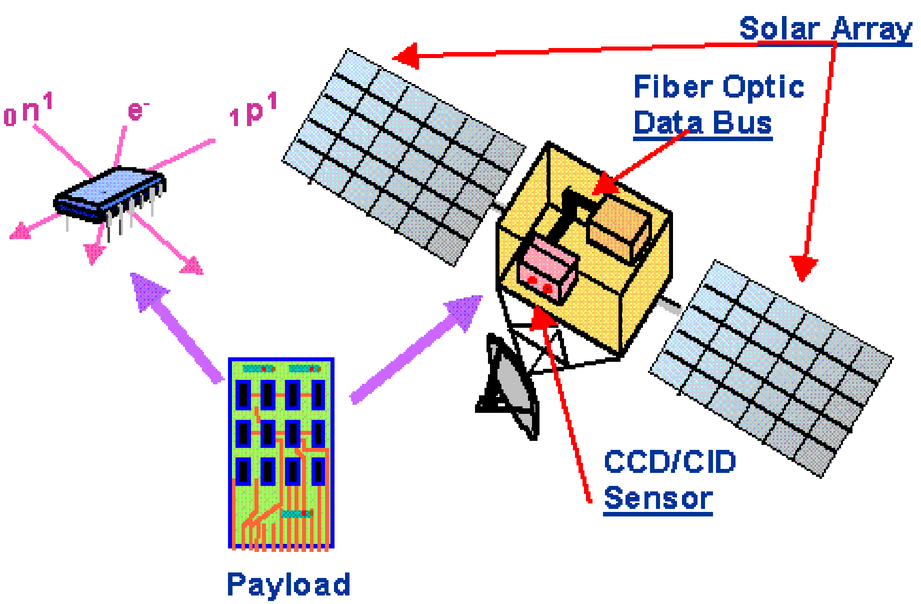
DoD Has Unique Radiation and Electrical Performance Requirements

(Dose Rate Survival, Launch Detect, Missile Intercept, etc. are DoD Unique)

Natural Space Radiation

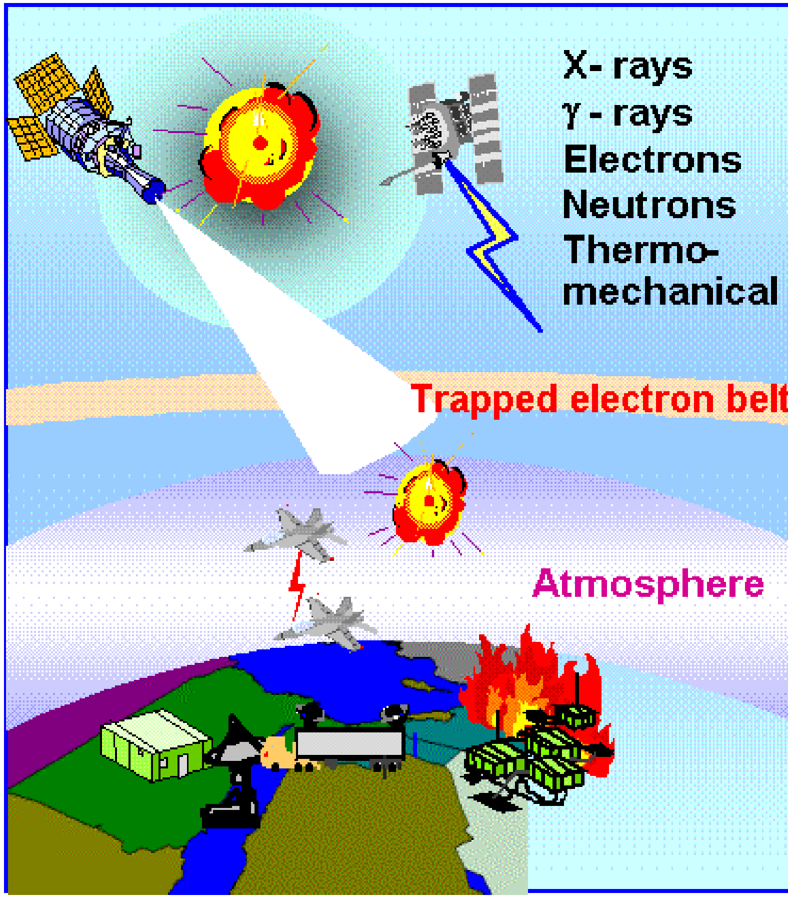


Total Ionizing Dose
- Trapped Electrons
- Trapped Protons

Single Event Effects (SEE)
- Galactic Cosmic Rays
- Solar Enhanced Particles
- Energetic Protons & Neutrons

Displacement Damage
- Energetic Protons & Neutrons

Nuclear Detonations



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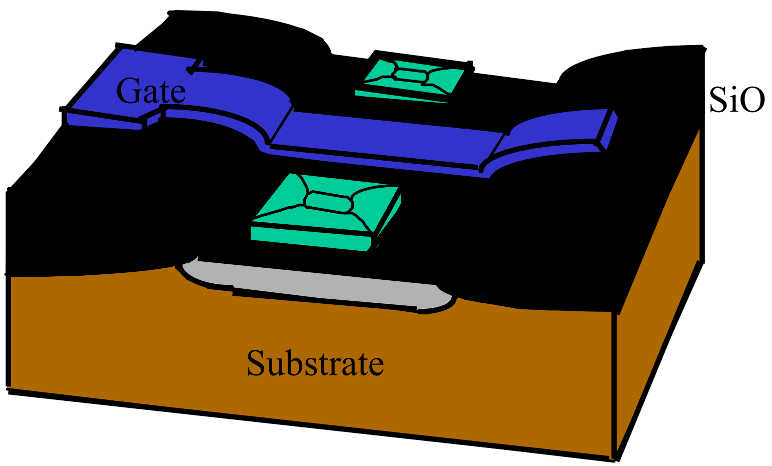
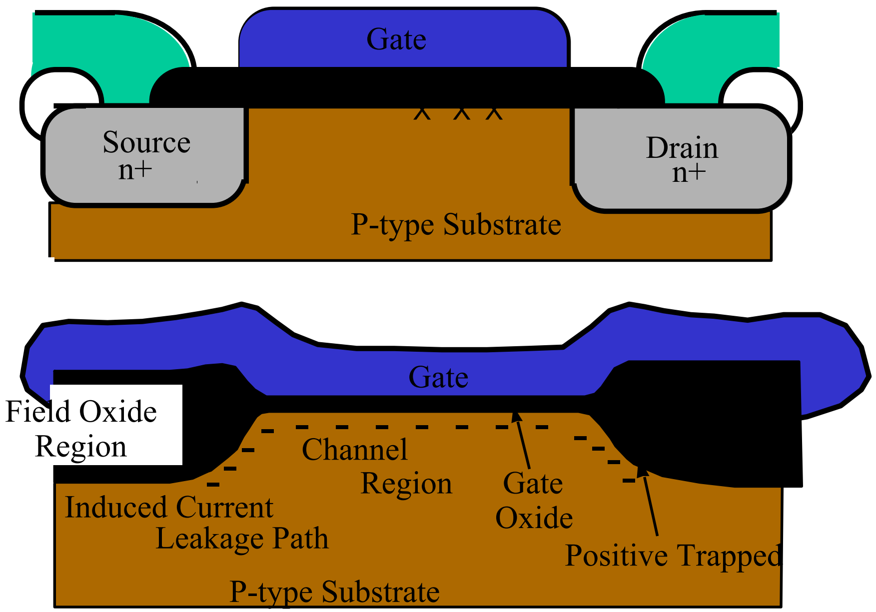
TOTAL DOSE

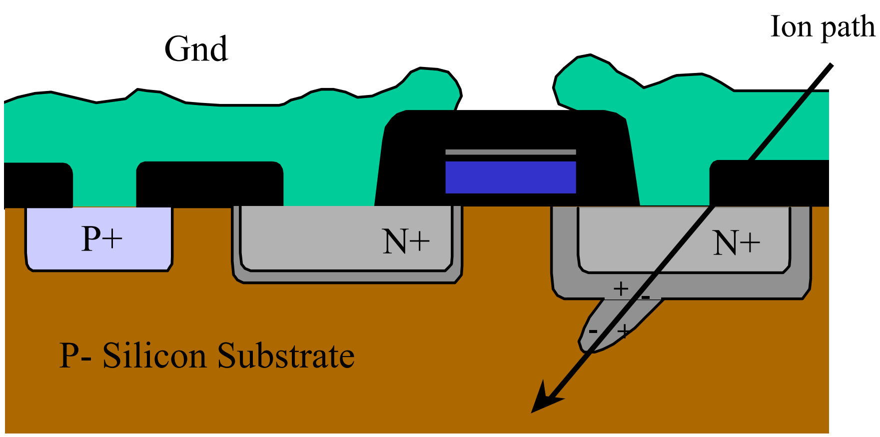
- Accumulated damage due to ionizing radiation
- Result of trapped protons and electrons, solar energetic particles, and weapon generated x-rays and γ-rays
- Degrades circuit performance and will eventually lead to functional failure

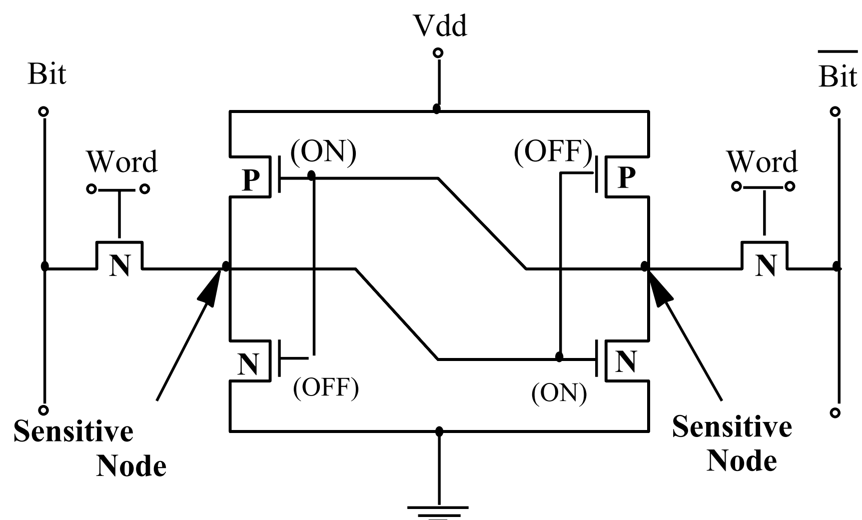




SINGLE EVENT UPSET

- Result of naturally occurring cosmic rays, trapped protons and solar energetic particles
- Soft errors generated within logic (typically associated with memory bit and storage elements)
- Undetected errors can propagate throughout the system





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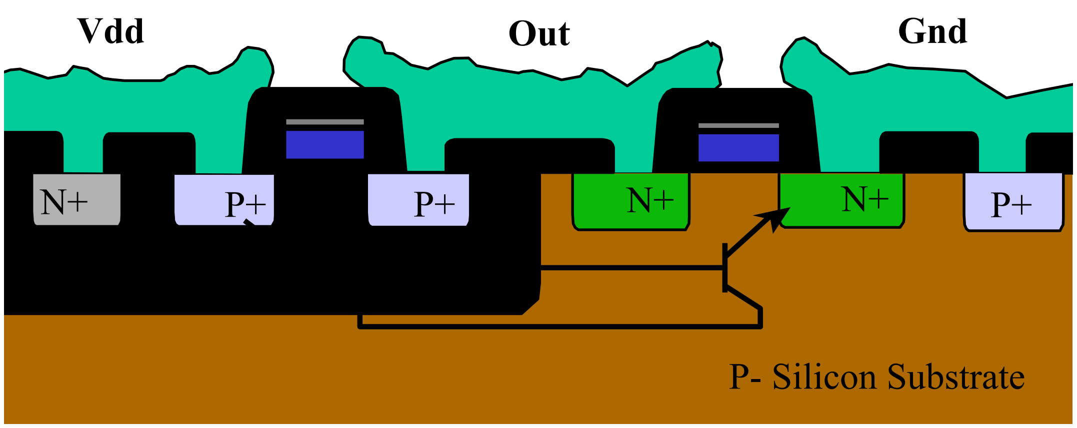
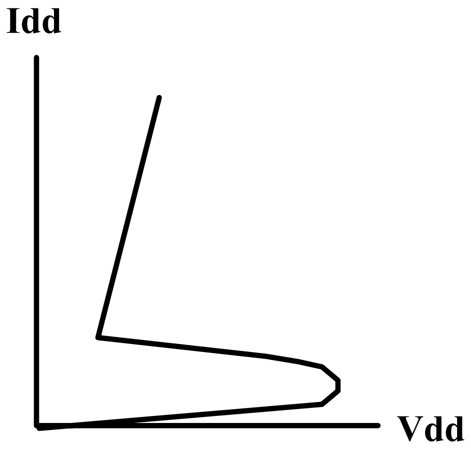
SINGLE EVENT LATCHUP

- Energetic particle turns on parasitic elements resulting in a high current path
- Circuit becomes inoperable
- Self-sustaining - recovery only through removal of power supply
- Can induce burnout (catastrophic failure)





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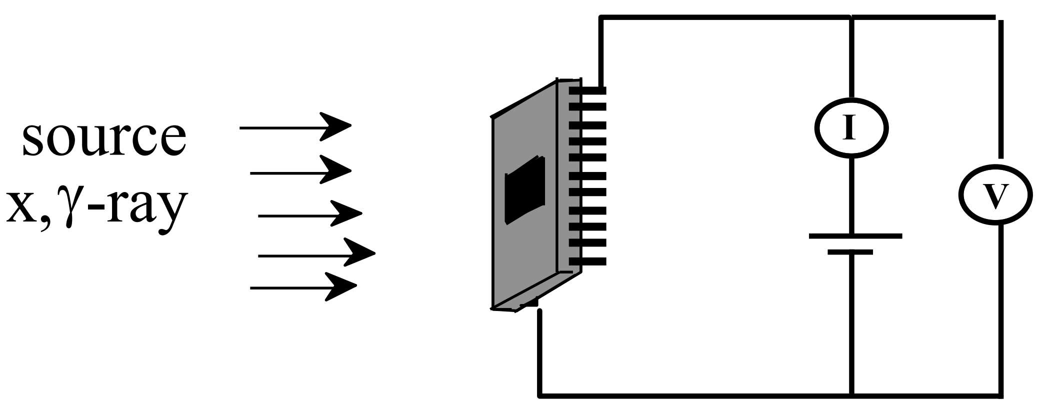
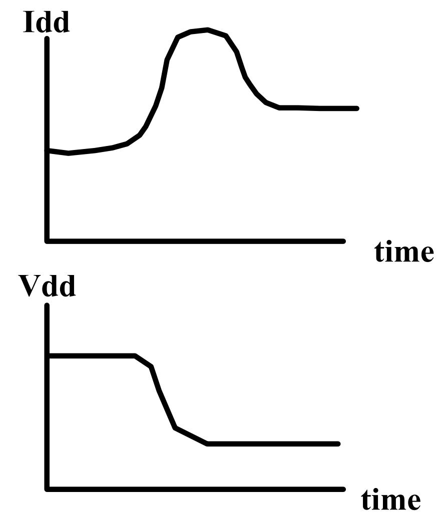
PROMPT DOSE

- Time dependent effects of ionizing radiation
- Result of high current surges generated within an integrated circuit due to weapon generated x-rays and γ-rays
- Divided into transient upset (soft errors) and survivability (catastrophic failure)





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Impact of Space Environment on Microelectronics - Summary

Effect	Source	Circuit Impact
• Total Ionizing Dose (TID)	• Trapped electrons • Trapped protons • Solar flares	• Parametric shifts • Gain degradation • Leakage current • Speed reduction
• Single Event Effects (SEE)	• Cosmic particles • Trapped protons • Solar flares	• Single event upset (SEU) • Single event latchup (SEL) • Single event gate rupture (SEGR)
• Prompt Dose	• Nuclear weapon	• Rail span collapse • Transient upset • Latchup • Transient burn-out

Effect on electronics is technology dependent

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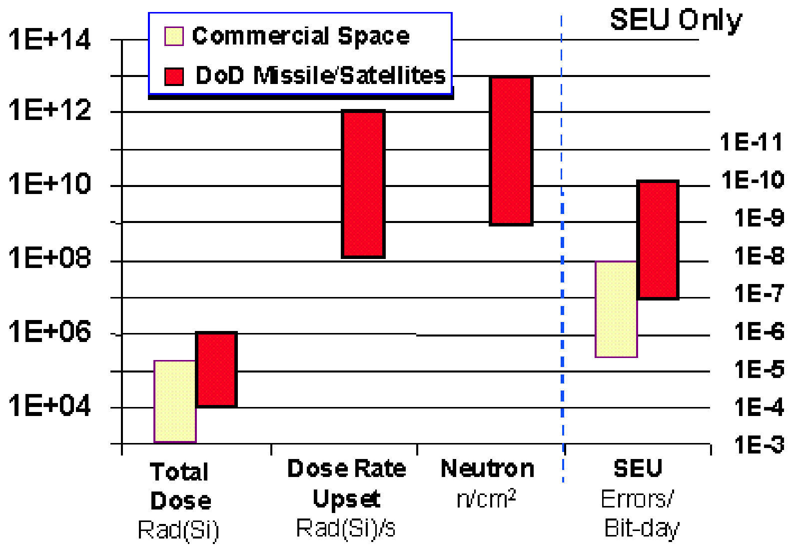
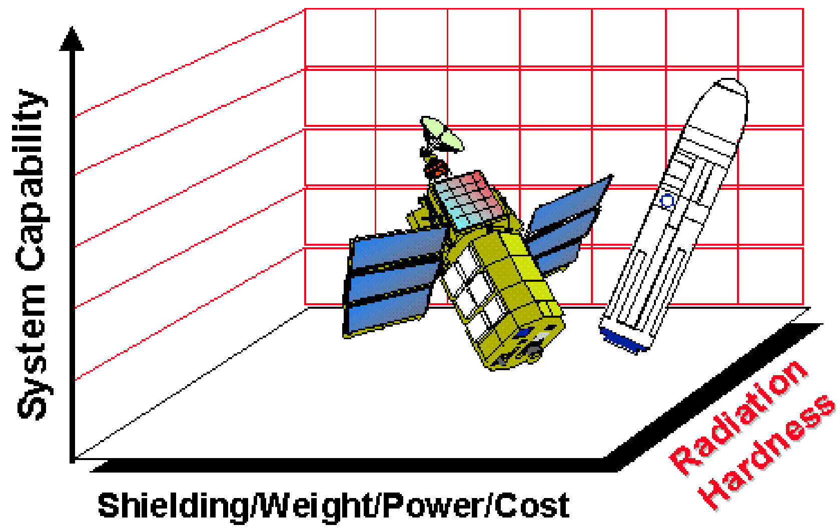
DoD Has Unique Radiation and Electrical Performance Goals

(Dose Rate Survival, Launch Detect, Missile Intercept, etc. are DoD Unique)

Radiation Goals



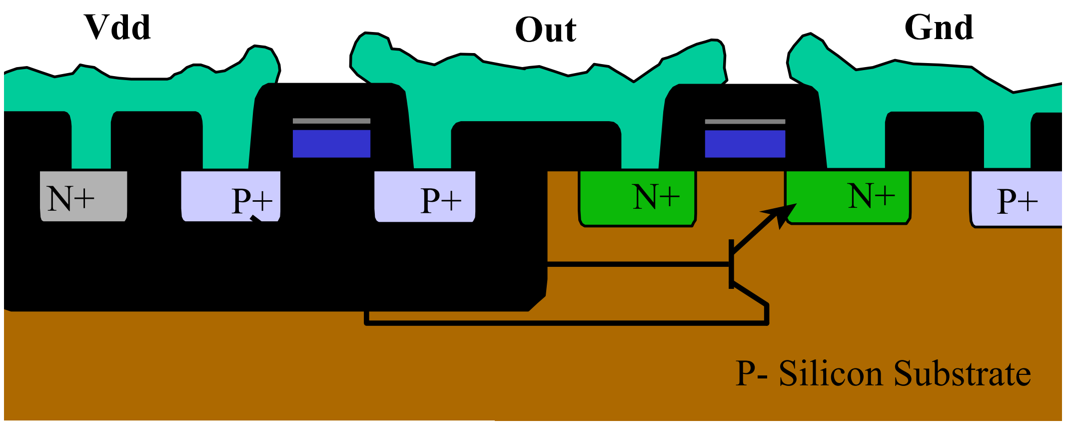
Design Tradespace



- Systems are built in a performance, cost, weight, and survivability tradespace
  - Cost savings accrue if hardness is designed in from the beginning
- Special materials, process and design rules are required for rad hard microelectronics
- Aerospace has been involved in all aspects of rad hard in support of space systems

SCALING

REDUCTION OF DESIGN FEATURE SIZES



IMPACT ON RADIATION HARDENING

- Improves total dose performance
- Degrades SEU tolerance
- Higher probability of latchup
- Decreases prompt dose performance

Emerging technologies create a change in effects to radiation

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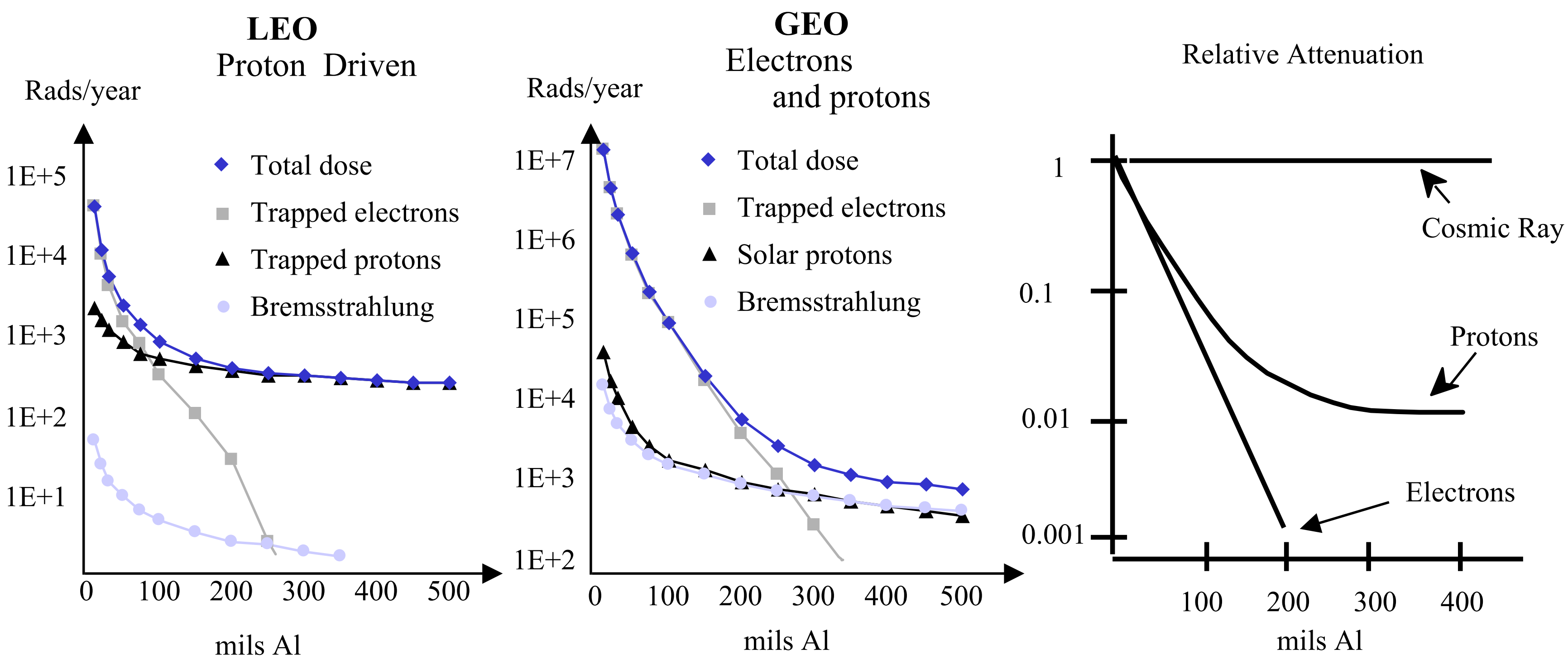
SHIELDING

- Shielding will not provide complete radiation immunity



- Shielding offers moderate to significant improvement for certain radiation effects

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Radiation Hardened Electronics Pre-1980's

- Satellites used minimal amount of electronics
  - "Bent pipe" operation
  - Most data processing performed on ground
- Electronic feature sizes were large
  - Technology tolerant to radiation
    - Use of bipolar technology
    - Digital electronics used technologies such as "Silicon on Sapphire (SOS)"
  - Electronics not affected by Single Event Effects
    - SEU not discovered until reduced feature sizes in electronics

Radiation Hardened Electronics 1980's and Beyond

- 1980's and into early 1990's DoD led the way
  - DoD Very High Speed Integrated Circuit (VHSIC) Program
    - Goal was to advance DoD electronics one generation ahead of commercial (for both non-hardened and hardened electronics technology)
    - DoD spent approximately $1 Billion over about 10 - 12 years to support all government electronic programs
    - Originally six contractors, downselected to three in 1987
      - IBM, Honeywell, and TRW
  - Other government programs funded many other contractors in development of radiation hardened electronics
    - Strategic Defense Initiative (SDI) helped contribute to the advancement of high speed electronics

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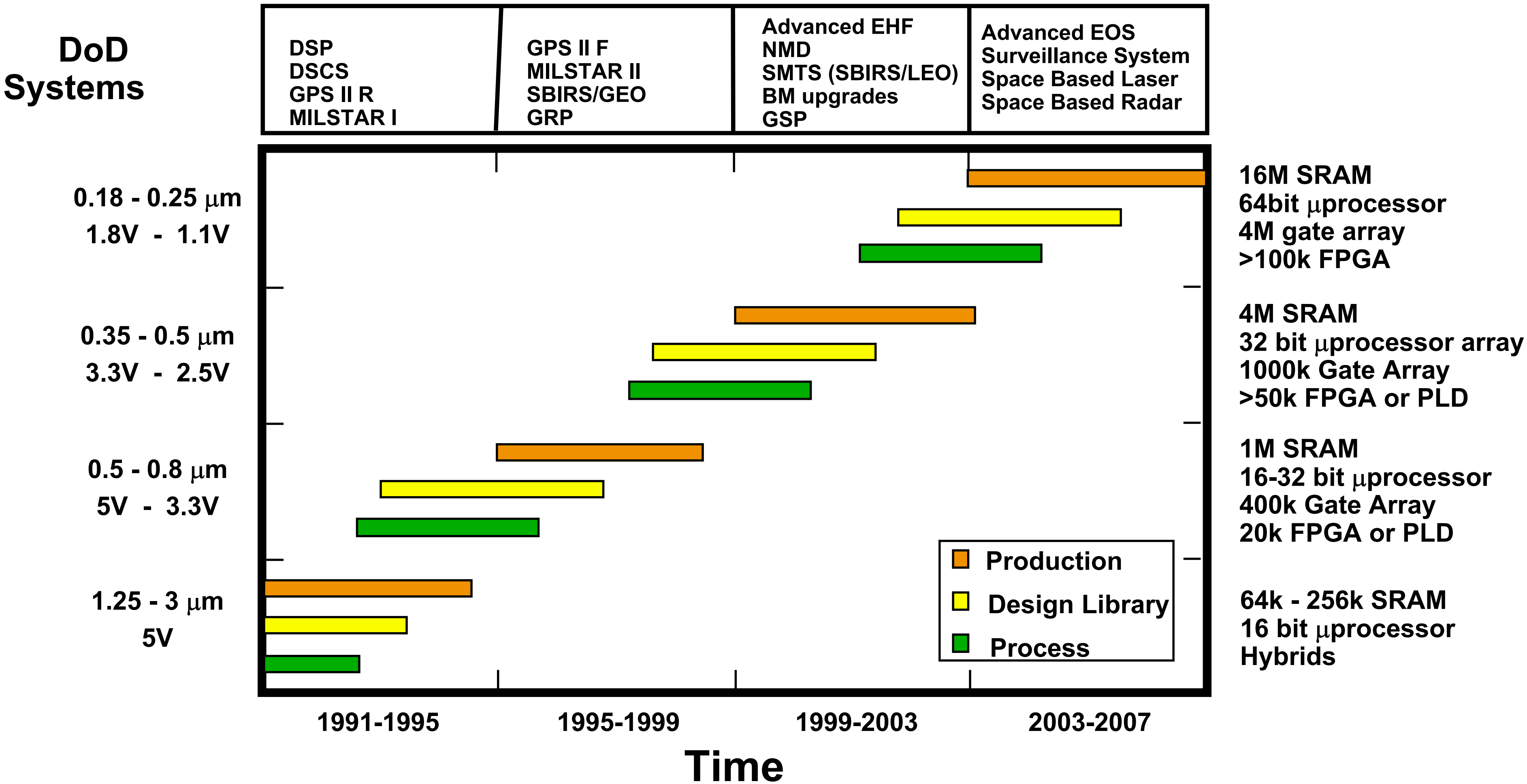
RAD HARD PRODUCT DEVELOPMENT
PROJECTED TECHNOLOGY TIMELINES



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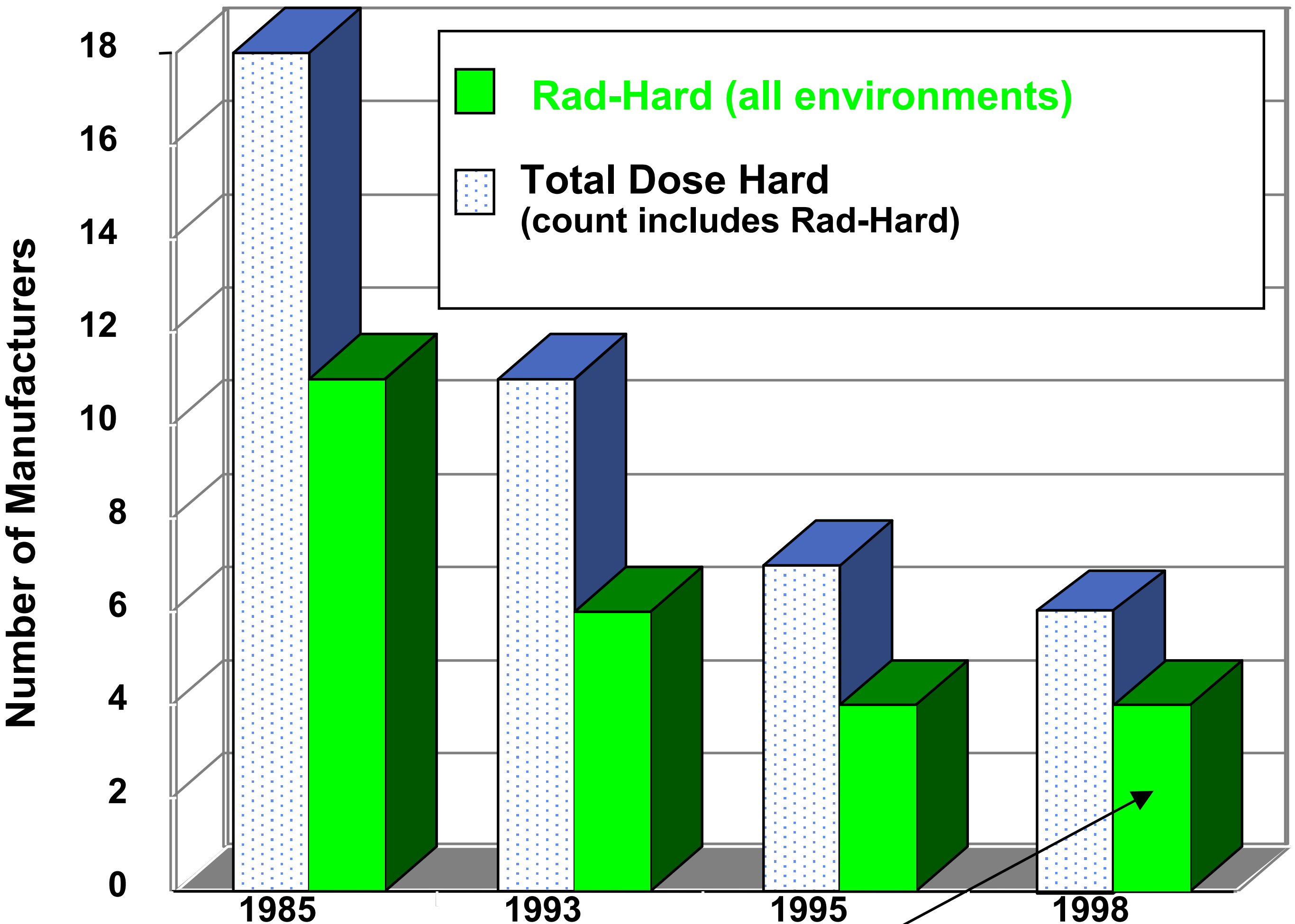
Radiation Hardened Electronics 1980's and Beyond (Con't)

- 1990's
  - Big reduction in Government funding
    - SDI programs reduced
      - Uncertain future
      - Biggest driver for radiation hardened electronics
  - Number of radiation hardened electronics manufacturers greatly reduced due to lack of funding and need
    - Over 30 manufacturers down to <6 by the late 1990's
  - Loss of expertise
    - Attrition, reduced emphasis in Universities

Production of Rad Hard Microelectronics Requires Special Manufacturers—but the Industry is in Jeopardy



2 Digital /2 Analog
LM (BAE) & Honeywell/ Harris & ADI

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Radiation Hardened Electronics 1980's and Beyond (Con't)

- In 1996 DoD formed a "Rad Hard IPT" to look at current and future radiation hardened electronic needs and recommend a strategy
  - Membership from across services and government organizations
  - Included Industry input
  - Key areas for IPT
    - DoD Requirements
    - Technology needs
    - Funding requirements
    - Technology Development Capabilities

Radiation Hardened Electronics 1980's and Beyond (Con't)

- December 1996 recommendations from "Rad Hard IPT"
  - Implement and fund Rad Hard IPT Strategy
    - Series of roadmaps and specific funding
  - Establish Radiation Hardened Electronics Oversight Council
  - Pursue graduate initiative

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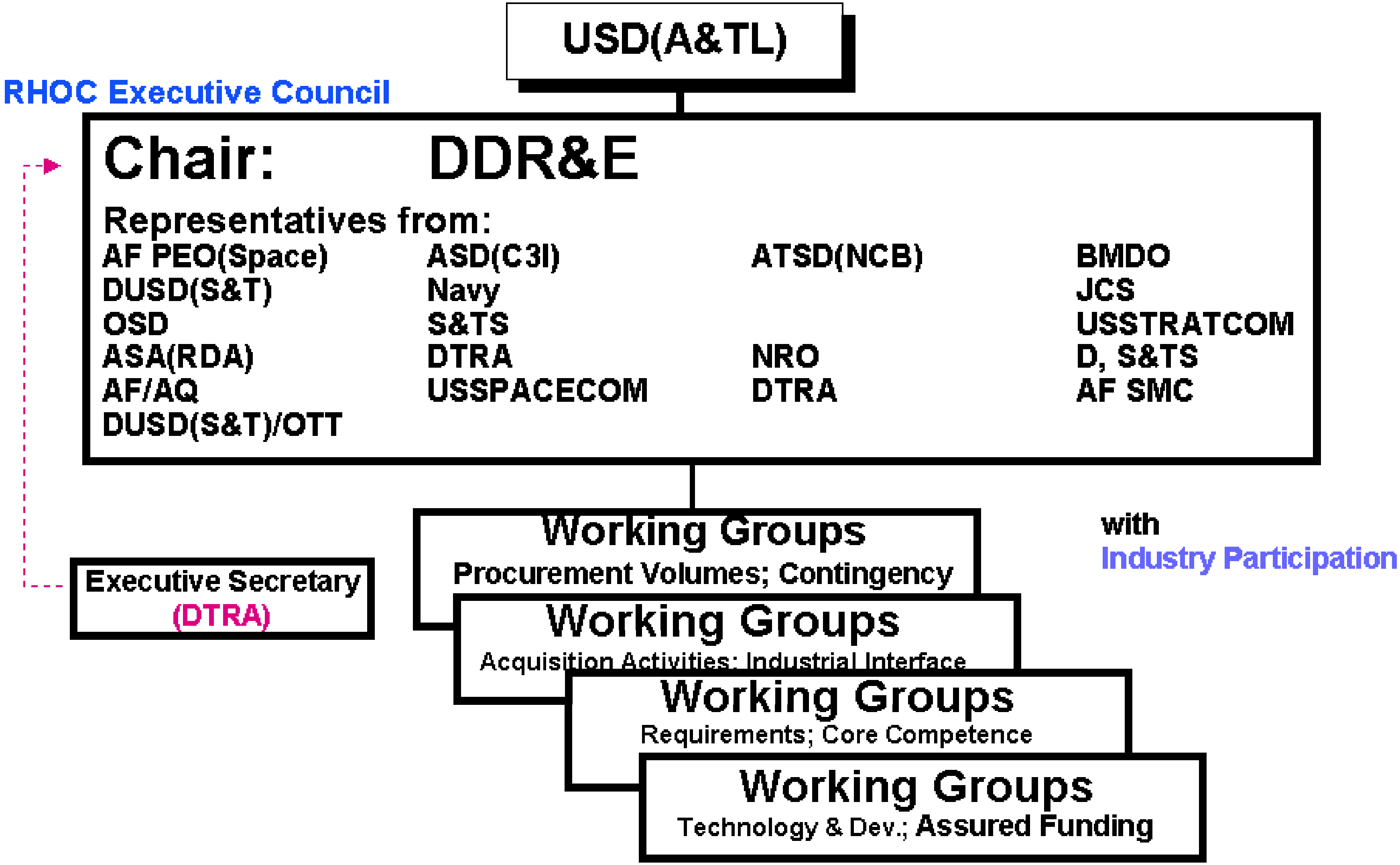
The Rad Hard Microelectronics "Solution" History

Jul 1994	STRATCOM alerts the National leadership and calls for study of rad hard electronics manufacturing infrastructure
Mar 1996	USD(A&T) charters Rad Hard Electronics IPT
Jun 1996	SEC DEF Perry responds to Congressional call for report: indicates USD(A&T) IPT will solve this problem
Dec 1996	IPT reports out; calls for "corporate" oversight and $60-70M "assured" funding for Rad Hard roadmap
May 1997	USD(A&T) Rad Hard Investment Strategy calls for implementation of all IPT recommendations---"corporate" leadership & "assured funding"
Dec 1997	Defense Reform Initiative: Rad Hard Electronics Oversight Council (RHOC) put on hold
Jan 1998	Dr. Gansler (USD (AT & L) instructs RHOC Working Groups to "continue working", concern with standing-up executive RHOC
Aug 1998	Dr. Gansler tasks Dr. Mark (DDR&E) to solve; RHOC Working Group reports to Dr. Mark
Jun 1999	DDR&E charters RHOC as "corporate" oversight body
Sep 1999	DDR&E chairs first RHOC meeting and accepts technology roadmap
10 Feb 2000	RHOC meeting to determine "assured funding" means for current roadmap
10 Mar 2000	Dr. Gansler (USD(AT&L)) signs Investment Strategy & directs full funding of RHOC rad hard roadmap

Radiation Hardened (Electronics) Oversight Council (RHOC)

- Charter
  - Objectives are to provide:
    - Oversight and coordination of DoD investment and procurement programs for rad hard electronics
    - Guidance on ensuring rad hard requirements are met
  - Functions:
    - Annually project expected procurement volumes
    - Monitor world-wide industrial capabilities
    - Coordinate science and technology activities in the development of rad hard electronics
    - Monitor DoD and other government and commercial needs and trends
    - Interface with industry
    - Monitor core competence

DoD Radiation Hardened Electronics Oversight Council (RHOC) Charter Organization/Membership



Radiation Hardened Electronics Oversight Council (RHOC)

Member	Representing
Dr. Hans Mark	(DDR&E) Director, Defense Research and Engineering, Chair
Dr. Delores Etter	(DUSD(S&T)) Deputy Under Secretary of Defense (Science and Technology)
Mr. Brent Collins	(AF PEO Space) Air Force Program Executive Officer for Space
Mr. Fred Celec	(ATSD)Assistant To the Secretary of Defense (NCB)
Dr. George Schneiter	(D, S&TS) Director, Strategic and Tactical Systems
Dr. Ted Hardebeck	Commander In Chief, USSTRATCOM (US Strategic Command)
BG Stephen J Ferrell	Commander In Chief, USSPACECOM (US Space Command)
BG Brian Arnold	(AF/AQ) Assistant Secretary of the Air Force (Acquisition)
Mr. John Andrews	Assistant Secretary of Defense (C3I)
Dr. Charles Davidson	Assistant Secretary of the Army (RDA)
Mr. John Schaefer	Assistant Secretary of the Navy (RDA)
Dr. William Frederick	(BMDO) Director, Ballistic Missile Defense Organization
BG Robert Summers	(DTRA) Director, Defense Threat Reduction Agency
Col Charles Bauland	(NRO) Director, National Reconnaissance Office
Mr. Marty Meth	Director, Industrial Capabilities and Assessments
Mr. Stan Jukubiak	(JCS) Joint Chiefs of Staff
Col Richard Skinner	C3ISR and Space Systems

RHOC Recent Activities

- 10 March 2000 - Dr. Gansler USD(AT&L) signs investment strategy and directs full RHOC roadmap funding
- National Defense Authorization Act for FY01 (Public Law 106-256)
  - Mandated that RHOC investment strategy be executed with full cooperation and participation
  - Secretary of Defense must submit an annual report to Congress - first report 1 April 2001
- Roadmap updates in progress - Recent meeting @ WPAFB with AFRL to update mixed-signal/analog technology
- Significant effort being expended by Space PEO to obtain support from other organizations
- Investigate "one generation" technology gap program

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Example of Detailed RHOC Roadmap ≥0.35 µm (funding removed)

Rad Hard Digital, ≥ 0.35 µm								
08/28/2000 8:28			Investment Plan ($M)					
Technology Capability Needs	**Maturity**		**FY00**	**FY01**	**FY02**	**FY03**	**FY04**	**FY05**
≥0.35 µm Technology								
SRAM tech dev & prototype								
Process development: 25 nsec, 0.35/0.5 µm;4M-bit SRAM **Proto-type** (LM , Honeywell)	P	62715BR/BH						
Product: 4M SRAM, **Productize, Qualify**	A	Productize/Qualify-UF						
4M SRAM Qualification and Yield Enh (Honeywell)		SSP						
4M SRAM Qualification and Yield Enh (Honeywell)	A	SBIRS-Low						
Million Gate ASIC								
1M Gate ASIC Prototype SOI-V (Honeywell)	P	63401F						
Design Libraries suitable for NGSP (Honeywell)	P	Congress Add (63401F)						
Product: 1M Gate Array SOI-V; **Productize, Qualify**	A	6.3-UF						
HX3000 completion (Honeywell)	A	SBIRS-Low						
Nonvolatile Memory								
Process development: Giant Magnetoreistive 1M NVR **Prototype** (Honeywell)	R, P	62715BR/BH						
Giant Magnetoreistive technology: Embedded NVR **Prototype** (Honeywell)	P	62715BR/BH						
Product: Embedded **NVR, Productize, Qualify**	A	Productize/Qualify-UF						
Process development: Chalcogenide NVRAM, 16M (LM)	R	Congress Add (63401F)						
16M non-vol memory, <40ns, 0.5 micron		63401F						
16M non-vol memory, <40ns, 0.5 micron		6.3-UF						
Product: 256k SONOS NVR 0.8 µm **(NG)**	A	63871C						
Product: 256K SONOS NVR		SBIRS-Low						
Product: Design of 1M SONOS NVR		SBIRS-Low						
Product: 1M SONOS NVR **EEPROM**		63871C						
		6.3-UF						
Product: NVR, Productize, Qualify (Single line for all NVR P&Q)	A	Productize/Qualify-UF						
Processors/Computer Architecture								
Next Generation Space Processor Power PC 603e; (Honeywell)	P	63401F						
PPC 603E Qualification and Yield Enh (Honeywell)	A	SBIRS-Low						
Product: Single Board Computer (Design, Validation, and Verification)	A	Productize/Qualify-UF						
Rad Hard Pentium (need: Internal DOE only: No stated DoD need)	P	63401F						
		62204F						
Pentium .35µm **(funds to Sandia, not commercial fabs)**		VS General						
Resolver - Analog to Digital Converter								
Resolver - Analog to Digital Converter (LM)		SBIRS-Low						
Sub total 62715BR/BH Funds								
UNFUNDED-DTRA								
Sub total AF S&T Funds								
UNFUNDED-AF S&T								
Subtotal BMDO Funds								
Unfunded BMDO								
Navy								
Subtotal Productize/Qualify								
UNFUNDED Productize/Qualify								

Technology Maturity Key
R = R&D Result **P** = Prototype/Demonstration **A** = Affordability Effort & Producibility/Qualification

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Examples of Detailed RHOC Roadmaps

EDA

Supporting Technology
Material & Basic Mechanisms / Hardness Assurance & Test Methods

ANALOG, Mixed Signal

Rad Hard Digital, 0.25-0.18 micron

Rad Hard Digital, ≥ 0.35 µm

08/28/2000 8:28 — Investment Plan ($M)

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4M SRAM Qualification and Yield Enh (Honeywell)		SSP						
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Product: 1M Gate Array SOI-V; Productize, Qualify	A	6.3-UF						
HX3000 completion (Honeywell)	A	SBIRS-Low						
Nonvolatile Memory								
Process development: Giant Magnetoreistive 1M NVR Prototype (Honeywell)	R, P	62715BR/BH						
Giant Magnetoreistive technology: Embedded NVR Prototype (Honeywell)	P	62715BR/BH						
Product: Embedded NVR, Productize, Qualify	A	Productize/Qualify-UF						
Process development: Chalcogenide NVRAM, 16M (LM)	R	Congress Add (63401F)						
16M non-vol memory, <40ns, 0.5 micron		63401F						
16M non-vol memory, <40ns, 0.5 micron		6.3-UF						
Product: 256k SONOS NVR 0.8 µm (NG)	A	63871C						
Product: 256K SONOS NVR		SBIRS-Low						
Product: Design of 1M SONOS NVR		SBIRS-Low						
Product: 1M SONOS NVR EEPROM		63871C						
		6.3-UF						
Product: NVR, Productize, Qualify (Single line for all NVR P&Q)	A	Productize/Qualify-UF						
Processors/Computer Architecture								
Next Generation Space Processor Power PC 603e; (Honeywell)	P	63401F						
PPC 603E Qualification and Yield Enh (Honeywell)	A	SBIRS-Low						
Product: Single Board Computer (Design, Validation, and Verification)	A	Productize/Qualify-UF						
Rad Hard Pentium (need: Internal DOE only: No stated DoD need)	P	63401F						
		62204F						
Pentium .35µm (funds to Sandia, not commercial fabs)		VS General						
Resolver - Analog to Digital Converter								
Resolver - Analog to Digital Converter (LM)		SBIRS-Low						
Sub total 62715BR/BH Funds								
UNFUNDED-DTRA								
Sub total AF S&T Funds								
UNFUNDED-AF S&T								
Subtotal BMDO Funds								
Unfunded BMDO								
Navy								
Subtotal Productize/Qualify								
UNFUNDED Productize/Qualify								

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• The need for Rad Hard microelectronics is a continuing DoD satellite/missile system and commercial satellite requirement
- commercial devices do not fill this need

• DoD is working to maintain radiation hardened technology to support current and future systems through the Radiation Hardened Oversight Council

• Need exists for continued advancement of radiation hardened technologies- reduce gap from five years to one generation

• Aerospace is a "key" player in the area of radiation hardened electronics at all levels

  - Environment
  - IR&D
  - Design
  - Analysis
  - Simulation

Acronyms

• EDA	Electronic Design Automation
• IPT	Integrated Product Team
• SECDEF	Secretary of Defense
• USD (A&T)	Undersecretary of Defense for Acquisition and Technology
• USD (AT&L)	Undersecretary of Defense for Acquisition, Technology and Logistics

Backup

Example of Detailed RHOC Roadmap 0.25-0.18 μm (funding removed)

Rad Hard Digital, 0.25-0.18 micron								
08/28/2000 8:28			Investment Plan ($M)					
Technology Capability Needs	Maturity		FY00	FY01	FY02	FY03	FY04	FY05
0.25 μm Technology RAD HARD								
Process Development: Rad Hard SOI process development 0.25 μm (Honeywell)	R	62715BR/BH						
Feeder Technology .25μm Fully Depleted SOI (MIT LL)	R	62715BR/BH						
0.25 μm **Prototype** Dev 4M Gate Array (LM , Honeywell, other?)	R,P	62715BR/BH						
Product: 4M Gate Array, Productize, Qualify	A	Productize/Qualify-UF						
16M SRAM Option (Honeywell)	A	SBIRS-Low P&Q						
PPC750 Radiation Hardened Desgin	R,P	6.3-UF						
Title III Product: Power PC 750 Productize, Qualify	A	94903D						
Title III RH PPC 750 & DSP 0.25 μm	A	94903D						
Title III RH PPC 750 & DSP 0.18 μm	A	94903D						
PPC 750 Microprocessor Development (LM)	A	SBIRS-Low P&Q						
Processor Technology Dev: Advanced Processor 0.25-0.18 μm (Honeywell)	P	63401F						
Chalcogenide RAM, 128M NV <40ns (LM)		63401F						
Chalcogenide RAM, 128M NV <40ns (LM)		6.3-UF						
Product: Chalcogenide RAM, 128M NV <40ns		Productize/Qualify-UF						
Chalcogenide Non-Vol FPGA		63401F						
Product: Chalcogenide 4M Gate FPGA (LM)		6.3-UF						
Product: Chalcogenide 1Gbit Mem <10ns (LM)		Productize/Qualify-UF						
≤ 0.25 μm Technology RAD Tolerant								
Non-invasive adaption of commercial process to rad tolerant								
Process: RH Process on Commercial Fab. Line (DUAP) (UTMC)	R	62715BR/BH						
Process: RH Process on Commercial Fab. Line (DUAP) ~~(National, MRC)~~	R,P	63401F						
Product: Rad Lite Power PC750; 200MIPS (LM)	R,P	Congress Add (63401F)						
RH LM-IBM co-processing integration	R,P	6.2-UF						
Prototype & Design Iterations	R,P	6.3-UF						
≤0.18 μm Technology RAD HARD								
Process Development: Rad Hard process development 0.18 μm (LM, Hnyl, other?)	R	62715BR/BH						
Feeder Technology .18μm FD SOI (MIT LL) SOI and CMOS, advanced materials	R	62715BR/BH						
0.18 μm Prototype Dev: 16M SRAM, 4M Gate Array (LM , Honeywell)	R,P	62715BR/BH						
Product: 16M SRAM, 0.18μm 4M Gate Array, Productize, Qualify	A	Productize/Qualify-UF						
Scalable 1Gflop Multi-Processor DSP, design, architecture	P	63401F						
Prototype: Reconfigurable computer	P	63401F						
Product: Reconfigurable computer Productize, Qualify	A	Productize/Qualify-UF						
R-H by Design Research of 0.08 μm - 0.13 μm L_{eff}	R	62601F						
Sub total 62715BR/BH Funds								
UNFUNDED-DTRA								
Sub total AF S&T Funds								
UNFUNDED-AF S&T								
Title III								
Subtotal Productize/Qualify								
UNFUNDED Productize/Qualify								

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Example of Detailed RHOC Roadmap
Analog/Mixed Signal (funding removed)

ANALOG, Mixed Signal

08/28/2000 8:28 — Investment Plan ($M)

Technology Capability Needs	Maturity		FY00	FY01	FY02	FY03	FY04	FY05
Analog & Mixed Signal Technology								
Process/Prototype Dev: 0.6 µm Mix Sig Tech CMOS, Low Pwr, 12-14bit, <200mW, 65 MSPS ADC (Intersil)	R, P	62715BR/BH						
Product: 0.6 µm Mix Sig Tech, Low Power, 12-14 bit, <200mW, 65 MSPS ADC **Productize, Qualify**	A	Productize/Qualify-UF						
Process/Prototype Dev: 0.25 µm Mix Sig Tech CMOS, Very Low Pwr, 12-16bit, <100mW, >100 MSPS ADC	R, P	62715BR/BH						
Product: 0.25 µm MixSig Tech, Very Low Pwr, 12-16bit, <100mW, >100 MSPS ADC **Productize, Qualify**	A	Productize/Qualify-UF						
Product: **Analog Digital Converters** (non-S&T that leverages S&T)								
12-16 bit Linear CMOS **(low power) ADC (ADI & Honeywell)**	A	63871C						
ADI/TSMC process transfer to Honeywell	A	6.3-UF						
12-bit ADC (Complete design transfer and fund 2nd lot) (HNY)	A	SBIRS-Low						
	A	Productize/Qualify-UF						
12-16 bit Complimentary Bipolar **(high performance) ADC (Analog Devices Inc)**	A	63871C						
(ADI XFCB)	A	6.3-UF						
	A	Productize/Qualify-UF						
Chalcogenide based Microelectronics NV 8bit Analog Memory, **0.25µm (LM)**		63401F						
Chalcogenide based Microelectronics NV 8bit Analog Memory, **0.25µm (LM)**		6.3-UF						
NV 8bit Analog Memory		Productize/Qualify-UF						
High Performance ADC Photcompensation, TID RH, SEU, Latchup protection		6.3-UF						
High Performance ADC Photcompensation, TID RH, SEU, Latchup protection	A	6.3-UF						
High Performance ADC Photcompensation, TID RH, SEU, Latchup protection	A	Productize/Qualify-UF						
R-H Cryo-Readouts for Improved E-O Sensors								
Low-noise, Single Pixel Readout		62601F						
Process/Prototype Dev: **RH 0.5 µm** Low noise amplifier & singal conditioner (Cryo ROIC)	R, P	62715BR/BH						
Title III Rad Hard Cryo Readout Circuit P&Q 0.5 µm Low Noise Amp	A	Title III 94903D						
Process/Prototype Dev: **RH 0.35 µm** Low noise amplifier & singal conditioner (Cryo ROIC)	R, P	62715BR/BH						
Product: RH 0.5 and 0.35 µm Low noise amplifier & singal conditioner (Cryo ROIC)		6. 2-UF						
		Productize/Qualify-UF						
Rad Hard Materials - Analog								
Title III Thick Box SOI	A	Title III 94903D						
Title III Thin Box SOI	A	Title III 94903D						
Sub total 62715BR/BH Funds								
UNFUNDED-DTRA								
Sub total AF S&T Funds								
UNFUNDED-AF S&T								
S&T BMDO-UF								
Subtotal 63871C Funds								
Unfunded BMDO								
Title III								
Tile III-UF								
Subtotal Productize/Qualify								
UNFUNDED Productize/Qualify								

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Example of Detailed RHOC Roadmap
Supporting Technology (funding removed)

Supporting Technology Material & Basic Mechanisms / Hardness Assurance & Test Methods								
08/28/2000 8:28			Investment Plan ($M)					
Technology Capability Needs	**Maturity**		**FY00**	**FY01**	**FY02**	**FY03**	**FY04**	**FY05**
6.1 Basic Research								
iii-V Tech **(NRL)**	R	61153N						
Oxide charging model; 6.1 basic research **(AFRL)**	R	61102F						
MURI - Defects models; Oxide models **(Vanderbilt)**	R	61103D						
6.2 Radiation Response of Materials/Materail Dev.								
Defects & Rad Response Investigation and Modeling (BM) **(NRL)**	R	62715BR/BH						
SOI Material and Technology (R-H BOX SOI, Thin-BOX SOI) **(NRL)**	R	62715BR/BH						
Low-Power, 0.25μm SOI and CMOS, SiGe 2 nm oxide **(AFRL)**	R	62601F						
RH FD & PD SOI 0.25-0.13 micron validation **(AFRL)**		62601F						
Photonics - Optical								
Photonics-Materials/Devices (VCSEL tech, polymide tech, compound semi tech) **(NRL)**	R	62715BR/BH						
Hardness Assurance & Test Methods								
RHA and Testing - Development of Enh Low DR Test Method, RHA Guidelines **(NSWC)**	R, P	62715BR/BH						
Single Event Effects Research & mitigation of SEE in CMOS, SOI, 0.25 μm tech **(NRL)**	R, P	62715BR/BH						
Sub total DTRA Funds								
UNFUNDED-DTRA								
Sub total AF S&T Funds								
UNFUNDED-AF								
Sub total Navy Funds								

Technology Maturity Key

R = R&D Result **P** = Prototype/Demonstration **A** = Affordability Effort & Producibility/Qualification

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Example of Detailed RHOC Roadmap
EDA (funding removed)

EDA								
08/28/2000 8:28			Investment Plan ($M)					
Technology Capability Needs	Maturity		FY00	FY01	FY02	FY03	FY04	FY05
Electronic Design Automation System								
EDA for Sub & Deep submicron Dig Tech; DSP & microprocessor dev;submicron analog; Design Tools, C40, combined digital & analog on a single chip	R, P	62715BR/BH						
Product: RH C30, RH C40, single chip combined digital & analog **Productize/Qualify**	A	Productize/Qualify-UF						
Advanced RH Circuit Design Automation								
Analog circuit design tools; demo chip 555 Timer & OP467	A	63871C						
		63871C-UF						
Modeling & Simulation (RH TCAD)								
RHTCAD Development & Process Validation	A	Navy System						
RHTCAD Technology Evolution	A	6.4-UF						
Sub total DTRA Funds								
UNFUNDED-DTRA								
Sub total BMDO Funds								
UNFUNDED-BMDO								
Sub total NAVY System Funds								
UNFUNDED-NAVY								
Subtotal Productize/Qualify								
UNFUNDED Productize/Qualify								

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