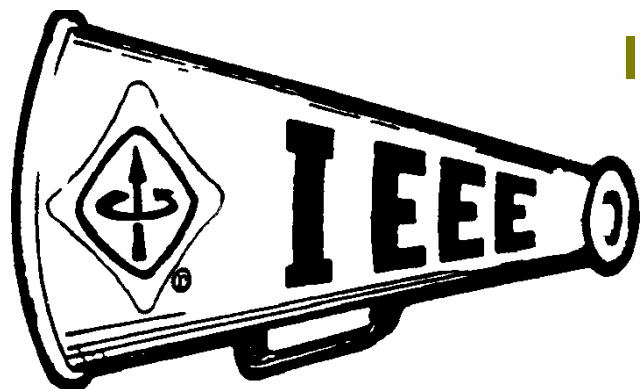


The Valley Megaphone



Newsletter of the
**IEEE – Institute of Electrical and
Electronic Engineers, Inc.
Phoenix Section**
July 2003, Volume XVII, Number 7

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Executive Committee contd..

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The Valley Megaphone is the newsletter of the Phoenix Section of the Institute of Electrical and Electronics Engineers. It is published monthly, September through June. The publication reaches about 4000 members. Submit articles, advertisements, and announcements to Dongming He at the above email address. Deadline for announcements and advertisements is the third Friday of the month prior to publication.

Advertising Rates: Full page: \$200, 3/4page: \$125, 1/2 page: \$75, 1/3 page:\$50,1/4 page:\$25. Change of address/email? Call toll free 1-800-678-IEEE. Please allow 6-8 weeks. Section Web Page is : <http://www.ieee.org/phoenix>



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Chapters & Branches

Contd.. from page 1

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SC2003 Conference on High Performance Computing and Networking to Be Held In Phoenix

From Nov. 15th to 21st, 2003, thousands of high-performance computing and networking experts will flock to the Phoenix Civic Plaza Convention Center to attend SC2003, the annual high performance networking and computing conference. The conference combines two days of tutorials, four days of technical papers and discussions and three days of exhibits featuring systems and applications by the world's leading vendors and research organizations.

SC2003 brings together scientists, engineers, educators, visualization artists, programmers, and business leaders to share ideas and glimpse the future of high performance networking and computing, data analysis and management, visualization, and computational modeling. Held each year in a different U.S. city, this year's conference will be held in Phoenix.

For more information about the conference, go to <http://www.sc-conference.org/sc2003/>. SC2003 is sponsored by the Institute of Electrical and Electronics Engineers Computer Society and the Association for Computing Machinery's Special Interest Group on Computer Architecture.

Job Opportunities

There are a few positions posted at www.thegreenstonegroup.com. Each of these current positions described at <http://www.thegreenstonegroup.com/opportunities.html> has to do with the design, enhancement and lifecycle maintenance of personal computer systems and servers, so experience will be needed in the computer hardware industry. It is important that anyone interested carefully review the individual requirements of any positions they may be interested in.



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High-field Effects and Fast Pulse Responses in Bio-Systems Workshop

October 19, 2003
Hyatt Regency Albuquerque
Albuquerque, New Mexico

In connection with the CEIDP 2003, a workshop on “High-field Effects and Fast Pulse Responses in Bio-Systems” will be held on Sunday, October 19, 2003, in the Hyatt Regency Albuquerque, Albuquerque, New Mexico. This Workshop builds on the success of the 2002 Workshop “Dielectric Properties and Electrical Breakdown of Biological Membranes”, which was organized by Karl Schoenbach, Old Dominion University.

Targeted Audience are those with interests in:

Biodielectrics	Biophysics
Biotechnology	Pulse technology
Liquid dielectrics	Industrial applications
Biotech Applications	Medical applications

Preliminary Technical Program (Sunday, October 19, 2003)

- Cellular Structure and Compartmentalization
- Electrical Parameters of the Cell Membrane and Compartment
- Macromolecular dielectrics
- Bio-dielectric responses to high fields
- Dielectrophoretic effects
- Effects of short pulses
- Biotechnological applications
- Panel and Participant Discussion

Technical information will be made available to registered participants in a Workshop Booklet.

Organization

The Workshop will take place on Sunday, October 19, 2003, in connection with but just before the start of the CEIDP 2003, in Albuquerque NM.

For further details contact

Vice-Chair: Raji Sundararajan, Arizona State University East.

Tel: 480-727-1507, Fax: 480-727-1723 e-mail: raji@asu.edu

Workshop Fee:

A workshop fee of \$ 75 will be charged to participants, and will provide entitlement to the Workshop Booklet, snacks at coffee breaks, etc.

Information on the CEIDP Conference (website: <http://ewh.ieee.org/soc/dei/ceidp/>)

The Conference on Electrical Insulation and Dielectric Phenomena (CEIDP) is sponsored by the IEEE Dielectrics and Electrical Insulation Society (DEIS) to provide an international forum for the discussion of work in progress on



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research on dielectric phenomena and measurements. The conference provides an opportunity for specialists from around the world to meet and exchange their experience.

The 2003 IEEE/CEIDP Conference Location and Date:

Albuquerque, New Mexico, USA, October 19 - 22, 2003.

Hotel Accommodations:

All sessions and activities of the 2003 CEIDP will be held at the

Hyatt Regency Albuquerque

330 Tijeras NW

Albuquerque, NM 87102

USA

TEL: 800-233-1234 or 505-842-1234

FAX: 505-766-6729

Be sure to mention that you are attending the 2003 IEEE/CEIDP when making your reservation to receive the Conference room rate.

The Conference room rate is US \$139 plus tax per night for single or double occupancy.

To ensure this rate, your hotel reservation and deposit must be received by September 25, 2003.

IEEE Senior Member and Fellow Grades

All IEEE Phoenix Section Members interested in getting nominated to Senior Member or Fellow Grade, please contact Vasu Atluri by telephone at (480) 554-0360 or by email at vpatluri@ieee.org. Please refer to www.ieee.org for more information related to senior member and fellow grades.

IEEE Phoenix Section Graduate of the Last Decade (GOLD) Affinity Group

Volunteers are needed to serve as officers for IEEE Phoenix Section Graduate Of the Last Decade (GOLD) Affinity Group. Volunteers should be active IEEE members from IEEE Phoenix Section who have obtained their first professional degree, preferably a Bachelor of Science in Engineering, within last decade. If interested, please contact Vasu Atluri by telephone at (480) 554-0360 or by email at vpatluri@ieee.org. Please refer to www.ieee.org for more information related to GOLD Affinity Group.



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IEEE-Phoenix Section PACE Announcement

A PROFESSIONAL CHALLENGE: CHANGING JOBS

Saturday, July 19, 2003

8:30 AM

Salt River Project Information Systems Facility
1600 North Priest (Washington and Priest)

The Valley job market is evolving. There are many companies downsizing, discontinuing or relocating product lines, re-engineering their organization or being purchased by other companies. In addition, there are new opportunities created by emerging technologies, business births, economic development and other factors.

The challenge for the displaced engineer or the individual searching for a new opportunity is how to effectively identify/qualify job leads and hiring organizations, develop an effective resume/job application package, and have a successful interview.

The workshop will go through each phase of your job transition including: preparation, search, contact, interview, selection, and growth.

Major workshop topics include:

- Personal SWOT analysis
- Resume development
- Networking
- Market analysis
- Search (industry and market)
- Interviewing (competency based and technical)
- Follow-up

In this four-hour workshop, you will:

- Identify and analyze your attributes, interests, skills and accomplishments and the impact you can make on an organization
- Develop a competency based resume and companion introduction letter
- Determine methods for making effective contacts and distributing your materials
- Identify of the different resources and personal networks that can be used in your job search
- Discuss elements of effective interviewing, including competency-based interviews, technical interviews and interview scoring
- Identify personal improvement opportunities and options
- Develop a marketing and tracking plan for all applications, interviews and feedback.

Registration

The registration fee for the program is \$10.00, payable to the IEEE-Phoenix Section. Registration and course related questions should be made directly to Michael Andrews, m.andrews@ieee.org. Registration is limited. Each participant will utilize a computer and Microsoft Word. You may bring a personal computer (optional).

Participants should bring an existing resume and current work history (soft copy and hard copy).



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COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY SOCIETY

Recent Advances in Wafer Level Packaging

Prof. C.P. Wong
Georgia Tech, Atlanta, GA

ABSTRACT

A paradigm shift from conventional discrete packaging to Wafer Level Packaging (WLP) is brewing in the IC packaging world, driven by rapid advances in IC fabrication and the growing market for high performance low cost electronic products. Wafer level chip scale packaging drives down the packaging cost per chip for wafer size increase or die size reduction. It also promises to improve the flip chip attach reliability without additional underfilling steps in the assembly process. Further cost reduction could be realized by doing wafer level test and burn-in on these WLP processed wafers.

This talk will focus on the following four key areas of the wafer level packaging process:

- a) Thin film redistribution and bumping
 - Structural enhancement to improve board level reliability and to enable SMT compatible assembly
- b) Encapsulated Wafer Level Packaging
 - Sealing wafer between two glass plates that is ideal for optical display
- c) Compliant interconnects
 - CTE mismatch stress relief between die and substrate, in large die applications, through the use of compliant interconnects such as “Microspring Contact on Silicon Technology” that provide for compliancy in both in-plane and out-of-plane directions.
- d) Wafer Level Underfill
 - Application of underfill to a bumped wafer, to eliminate individual underfill dispensing in flip chip assembly

Recent advances in material development and process approaches, in the above areas, will be discussed.

BIOGRAPHY

Dr. Wong received his B.S. degree in chemistry from Purdue University and his Ph.D. degree in inorganic/organic chemistry from the Pennsylvania State University. After a two-year post doctoral fellowship study with Nobel Laureate Prof. Henry Taube at Stanford University, he joined AT&T Bell Labs in 1977 as a member of the technical staff and worked on polymeric materials for electronics and photonic applications. With continued achievement and growth, he was bestowed with the prestigious award of AT&T Bell Laboratories Fellow, in 1992, for his fundamental contributions to low-cost high performance plastic packaging of semiconductors.

Since 1996, Dr. Wong is a Professor at the School of Materials Science and Engineering and a Research Director at the NSF funded Packaging Research Center at the Georgia Institute of Technology. He was named a Regents’ Professor in July 2000. Dr. Wong holds over 40 US patents, numerous international patents and has published over 450 technical papers. He serves on the editorial boards of the IEEE Transactions on CPMT, the Chip Scale Review and several other journals. He has authored and co-authored several text books and handbooks. Dr. Wong is a



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fellow of the IEEE and AIC and has served as the technical vice-president (1990 & 1991) and the president (1992 & 1993) of the IEEE CPMT Society. He was elected as a member of the National Academy of Engineering in 2000.

Date: Friday, August 15th, 2003.

Location: Motorola, 2100 E. Elliot Rd., Tempe, AZ (Dan Noble Conference Room).
Entrance to the facility through main (south) lobby by the flagpoles. You will be escorted to the Conference Room.

Time: 5:30-6:00 p.m. - Social/Refreshments; 6:00-7:00 p.m. - Presentation; 7:00 p.m. Dinner

IEEE members & non-members are welcome. Refreshments, pizza & soda provided by CPMT Society Phoenix Chapter.

For more information, please call any of the following officers:

Mali Mahalingam, Motorola (480) 413-5368

Rao Bonda, Motorola (480) 413-6121

Eric C. Palmer, Intel (480) 554-8710

Sam Karikalan, Primarion (602) 659-4634

Ravi Sharma, Microchip (480) 792-7920

Vasu Atluri, Intel (480) 554-0360