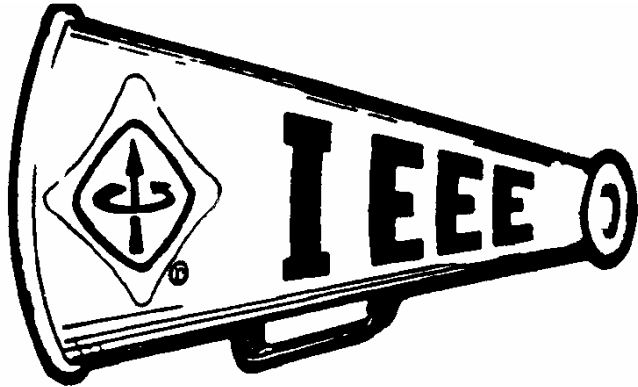


The Valley Megaphone



Newsletter of the
**Institute of Electrical and
Electronics Engineers, Inc.**
Phoenix Section
July 2005, Volume XIX, Number 7

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This Issue of The Valley Megaphone Features:

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IEEE Phoenix Section Executive Committee meeting minutes can be found at: <http://www.ieee.org/phoenix>

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The Valley Megaphone is the newsletter of the Phoenix Section of the Institute of Electrical and Electronics Engineers. It is published monthly, usually September through June. The publication reaches about 4000 members. Submit articles, advertisements, and announcements to Eric Palmer at the above email address. Deadline for announcements and advertisements is the third Friday of the month prior to publication.

Advertising Rates: Full page: \$200, 3/4page: \$125, 1/2 page: \$75, 1/3 page: \$50, 1/4 page: \$25. Change of address/email? Call toll free 1-800-678-IEEE. Please allow 6-8 weeks. Section Web Page is: <http://www.ieee.org/phoenix>



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IEEE ANNOUNCEMENTS

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Peak Oil: the Reality and the Aftermath Geoff Sutton, ETA Engineering

Date: Thursday, July 14, 2005

Time: Networking begins at 6:30 p.m.

Dinner begins at 7:00 p.m.

Place: Denny's Restaurant

3315 N. Scottsdale Rd.

Scottsdale, Arizona 85251

Abstract: This presentation brings an awareness of trends in the fossil fuels industry. The industry is gradually reaching a point where global demand for oil outpaces the supply. At current rates of consumption and drilling, there is no question that an inflection point will take place that will change the way we harness energy for our everyday needs. The main questions are: when will it take place and what can we do now to minimize any repercussions?

Speaker: Geoff Sutton is a sales representative with ETA Engineering. He offers renewable energy solutions and assists customers with their project development. He recently appeared on Fox 10 News to offer his perspective on the fossil fuels industries and renewable energy. He has worked in sundry firms all involved in the fossil fuels industry including banks, construction, automobile firms, and an advertising agency.

Directions: In Scottsdale, go west from Highway 101 and Indian School Road. Turn left on Scottsdale Road to head south. It is at the southeast corner on Scottsdale Road at Osborn Road.

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IEEE ANNOUNCEMENTS



Institute of Electrical and Electronics Engineers, Inc. Phoenix Section

Components, Packaging and Manufacturing Technology Society Chapter
&

Waves and Devices Chapter

PRESENT AN ALL-DAY WORKSHOP ON

Devices, Interconnects, and Packaging for Next Generation Computing and Communication Applications

Date: Thursday, November 10th, 2005

Time: 7:00 A.M. – 5:00 P.M.

Location: Arizona State University, Tempe, Arizona – ASU Memorial Union (Arizona Room)

Abstract

The one-day workshop will focus on device, interconnect and packaging challenges for next generation computing and communication applications. Participants will hear from leading contributors from industry, academia and the national labs. Long-range technology roadmaps will be reviewed and state-of-the-art processor, memory, and mixed-signal technologies will be addressed. Chip, package, and board-level interconnect issues will be discussed. Key materials, process, and performance challenges for physically realizing the required devices, interconnects and packaging will be presented. Market trends in computing and communications are within the scope of the workshop as well. A panel discussion on the future of computing and communications will bring closure to the day's workshop. Vendors representing the entire supply chain of chip, package, and board will display their products and services.

Topics

- ? **System & Architecture:** Future computing approaches (local vs. net-centric, personal & server computer); convergence of computing and communication; advances in processor technology such as multi-core, high-bandwidth buses and advanced drivers/receivers; memory/processor integration; SoC partitioning, modeling, and testing challenges/issues.
- ? **Materials & Processing:** ITRS roadmap for CMOS technology; Moore's law/prognosis in the context of the next few technology nodes; BEOL processing (low-k/Cu, ultra low-k/Cu); advances in memory technologies.
- ? **Simulation & Modeling:** Simulation for advanced devices; EM simulation in RF circuit/module/package design; signal noise analysis for SoC.
- ? **Advanced Packaging:** New packaging technologies, especially flip-chip, lead-free, 3D interconnect, multi-chip, and RF modules.
- ? **Special Topics:** Signal integrity; power delivery and distribution; cooling/thermal management.
- ? **Panel discussion on the future of computing and communications.**



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