LICS @ UCR
Laboratory for Integrated Circuits and Systems

- RF/Mixed-Signal/Analog IC & SoC
- On-Chip ESD Protection for ICs
- IC CAD & Modeling
- Semiconductor Devices
RECENT RESEARCH PROJECTS

Projects:
* Low-parasitic hi-robust ESD protection for RF/AMS ICs
* Super compact ESD protection
* 3D ESD protection simulation-design methodology
* 3D hi-l electro-thermal ESD device modeling
* ESDcat – whole-chip ESD design synthesis & verification CAD
* ESD protection for nano technology
* Multi-mode CMOS RF transceiver ICs
* Gbps full-band carrier-free impulse 1-UWB SoC
* On-Si antenna for UWB
* 24GHz RFID with on-chip antenna
* Transistor-size M-cored inductors for CMOS RF SoC
* RF-ESD co-design methodology
* New PA circuit model
* Modeling & CAD for electro-magnetic devices
* Precision bandgap reference IC in CMOS/BiCMOS
* Resolution/sampling/power-optimized ADC in SiGe BiCMOS
* Low-power multi-Gsps ADC in CMOS

Sponsors:
* National Science Foundation
* SRC, AKM, RF Integrated Corp., National Semiconductor, ESD Association, Mektronix, Synopsys, Agilent, Skyworks, SMIC, GSMC, etc.

Lots of joint designs with companies.
We use industrial design flows.
We deliver working Si, not just reports.
Outlines

• Basics on ESD Protection
• Mixed-Mode ESD Simulation-Design Method
• RF ESD Protection Circuit Design
• ESD+RF IC Co-Design
• Summary
A Multi-Billion-$ Problem!

- ESD = Electrostatic Discharge
- Phenomena: huge I/V-pulses
  $\Rightarrow$ IC damages!

- A multi-billion-$ problem
- ESD failures $\rightarrow$ 30%-50% IC failures
- A killing factor to time-to-market

☞ on-chip ESD protection required!

Informal ESD Failure Statistics

- Fab: 26%
- Assembly: 14%
- Good 4% on 3%
- Unknown: 15%
- ESD/EOS: 37%

ESD Testing Standards

• HBM - human body model.
• MM - machine model.
• CDM - charged device model.
• IEC - International Electrotechnical Commission
• TLP - transmission line pulse model
• etc....
HBM Test Model

MIL-STD-883E, Method 3015.7

- **MIL-STD-883E**
  - \( L_{\text{ESD}}=0 \)H
  - \( L_{\text{ESD}}=15 \)uH
  - \( L_{\text{ESD}}=7.5 \)uH, \( C_s=1 \)pF,
    \( R_L=500 \)Ohm, \( C_L=30 \)pF

### Circuit Table

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_0 )</td>
<td>( 10^6 - 10^7 ) ( \Omega )</td>
</tr>
<tr>
<td>( R_{\text{ESD}} )</td>
<td>1500 ( \Omega )</td>
</tr>
<tr>
<td>( C_{\text{ESD}} )</td>
<td>100pF ( \pm 1% )</td>
</tr>
</tbody>
</table>

### Equation

\[
i_{\text{ESD}}(t) = \frac{V_{\text{ESD}}}{2L_{\text{ESD}}\sqrt{\frac{\alpha^2 - \alpha_0^2}{C_{\text{ESD}}}}} \left( e^{\alpha t} - e^{\alpha_0 t} \right)
\]

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ESD Protection Basics

Various ESD protection solutions:

• Advanced package solutions.
• Buffers using new anti-ESD materials.
• Surge protection devices on board
• etc.

☞ On-Chip ESD protection circuitry for all I/Os of IC chips.
ESD Failure & Protection

• Two types of ESD damages:
  • Thermal damage: heating in Si/metal $\leftarrow$ high currents
  • Dielectric rupture $\leftarrow$ high electric field $\leftarrow$ high voltage

• Two ESD protection principles:
  • To discharge hi-current safely,
  • To clamp pad voltage to a sufficiently low level.
ESD Protection Mechanisms

- Simple turn-on I-V,
- Snapback I-V.
- Protect EVERY I/O pad on chip!

Basic ESD Protection

• Diodes
• Bipolar transistors
• MOSFET
• SCR
• Other novel/exotic structures
ESD Protection: Simple or Complex?! 

Emerging Challenges in ESD Design

- Design prediction by simulation
- Design optimization by simulation
- 3D ESD protection device modeling
- Whole-chip ESD design theory and methodology
- CAD algorithm & tools for ESD synthesis and verification
- ESD protection circuitry for RF/AMS ICs
- RF-ESD co-design method
- ESD protection for nano technologies
Mixed-Mode ESD Simulation-Design

• 2D/3D Mixed-Mode ESD Simulation-Design Methodology:
  ✓ Electro-thermal-process-device-circuit-layout coupling
  ✓ Static-transient ESD simulation

⇒ ESD design optimization, no trial-and-error!
  no over/under-design!
⇒ Forward ESD design, not backward analysis!
⇒ Compact ESD protection designs
⇒ Minimize ESD-induced parasitic effects
⇒ Explore novel ESD structures

ESD Design Method: New ~ Old

**Traditional**
- Experience
- Isolated SIM (device or circuit)
- ESD design
- Silicons
- Debug

**New Approach**
- ESD specs
- Mixed-mode SIM (device + circuit)
- ESD design
- Si w/ Confidence
- Measurement

Full ESD simulation

**Goal: 1st Si Success!**
Mixed-Mode ESD Design Principle

- Chip-level ESD circuit design
- No-assumptions
- Freeze-up your rich experiences for a while

![ESD Circuit Diagram]

- $V_{HBM}$
- $C_C$
- $L_s$
- $R_d$
- $C_s$
- $C_t$

ESD source circuit (e.g., HBM model)

ESD sub-circuit to be simulated

Core IC Chip

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Example-1: NMOS ESD Designs

- ggNMOS $\Rightarrow$ gcNMOS

HBM Model

- $R = 1.5K$
- $L = 10uH$
- $C = 100pF$
- $C_1 = 0.1pF$
- $R_1 = 10K$

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Example-1: ggNMOS ~ gcNMOS ESD
Example-1: ggNMOS ~ gcNMOS ESD

To reduce triggering $V_{tt}$ by design.
## Example-1: ggNMOS ~ gcNMOS ESD

<table>
<thead>
<tr>
<th></th>
<th>GGNNMOS</th>
<th>GCNMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>SIM.</td>
<td>TEST</td>
</tr>
<tr>
<td>$V_{t1}(V)$</td>
<td>14.68</td>
<td>12.56</td>
</tr>
<tr>
<td>$t_1(ns)$</td>
<td>0.2</td>
<td>-</td>
</tr>
<tr>
<td>$V_{h}(V)$</td>
<td>6.92</td>
<td>6.48</td>
</tr>
<tr>
<td>$V_G(V)$</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>$t_G (ns)$</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

Triggering $V_{t1}$ reduced successfully,

Good design prediction and 1st Si success.
RF ESD Protection Design

- What’s **Unique** for RF ESD protection?!
  - RF IC is sensitive to ESD-induced parasitic effects
  - Need accurate RF ESD characterization
  - Low-parasitic compact RF ESD protection design
  - Whole-chip ESD protection circuit design concept

- **New & Critical:** ESD-Circuit Interactions
  - ESD-to-Circuit Influences
  - Circuit-to-ESD Influences

- **RF+ESD co-design**

Circuit-to-ESD Influences

- ESD protection may be affected by the core circuits:
  - Weak discharge links in core IC → Early ESD Failure.
  - ESD unit triggers upon ESD pulses & stays OFF otherwise,
  - dV/dt, dl/dt effects contribute to ESD triggering,
  - Fast RF and M-S signals may trigger ESD units ACCIDENTLY

Unique Challenge 1:

ESD Mis-Triggering by RF signals.
ESD Parasitics: $C_{ESD}$

- Circuit performance may be affected by ESD circuitry:
  - ESD-induced parasitic $C_{ESD}$ (up to $\sim$pF) & $R_{ESD}$,
  - $C_{ESD} R_{ESD}$ delay $\Rightarrow$ signal integrity, clock corruption, ...
  - $C_{ESD}$ $\Rightarrow$ loading effect, Z-matching, power efficiency, BW, ...
  - $\Delta C_{ESD}$, $\Delta R_{ESD}$ $\sim$ frequency, biasing, temperature, ...

فض: Unique Challenge 2:
- Accurate $C_{ESD}$ estimation,
- Including $C_{ESD}$ in RF IC design,
- Reduce $\Delta C_{ESD}$ over $\Delta f_{RF}$
ESD Parasitics: Noises

• Substrate noise coupling effect due to $C_{ESD}$:
  – Incident noises at I/O coupled into substrate,
  – Substrate noises $\Rightarrow$ I/O $\Rightarrow$ signal path

• ESD self-generated noises:
  – Thermal noises,
  – Flicker noises,
  – Shot noises, etc.

☞ Unique Challenge 3:
ESD noises into RF ICs.
Mixed-Signal ESD Protection

- No global ESD solutions!
- No one $V_{t1}$ fits the whole chip!
- Multi-$V_{DD}/V_{SS} \Rightarrow$ locally-optimized $V_{t1}$ for different I/Os,
- Need a safety margin for $V_{t1}$:
  - $V_{t1}$ of 5V fits $V_{DD} = 3.3$V blocks,
  - $V_{t1}$ of 23V good for $V_{DD} = 15$V blocks.

➢ Challenge 4: multi-$V_{t1}$ ESD design in RF/AMS ICs
  ⇒ whole-chip ESD design optimization,
  ⇒ on-chip local ESD design optimization
Circuit-to-ESD Influences

- Observation in TLP testing of ESD structures:
  - ggNMOS, dSCR ESD structures, etc.
  - TLP pulse $t_r \approx 0.2 \sim 20$ns,
  - Strong $V_{t1} \sim t_r$ correlation,
  - $t_r \Rightarrow V_{t1} \Rightarrow$

![Diagram of ESD structures and TLP testing](image)
Example-3: ESD-Protected RF IC Design

ESD affects RF IC substantially:

- 5GHz LNA for dual-band WLAN transceiver
  - CE-CB cascode topology
  - High/low gain switching
  - Unique double shutdown function
- 0.18μm SiGe BiCMOS
- 2KV ESD protection

Example-3: LNA Noise ~ ESD

<table>
<thead>
<tr>
<th>LNA circuits</th>
<th>$S_{21}$(dB)</th>
<th>$S_{11}$(dB)</th>
<th>NF(dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>w/o ESD</td>
<td>18.11</td>
<td>-8.3</td>
<td>2.99</td>
</tr>
<tr>
<td>with ESD</td>
<td>15.08</td>
<td>-7.2</td>
<td>3.19</td>
</tr>
<tr>
<td>Degradation</td>
<td>16.73%</td>
<td>17.25%</td>
<td>6.8%</td>
</tr>
</tbody>
</table>

$F_{Total} = F_{ESD} + \frac{F_{LNA} - 1}{G_{ESD}}$

$NF_{ESD} \geq 0.1$ dB

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Reference-1: 2.4GHz LNA+ESD

ESD modeled by $C_p = C_{ESD} + C_{BP}$ ?

External $L_g$ & $C_b$ to tune 50Ω matching?!

Still show big LNA degradation!!

<table>
<thead>
<tr>
<th>LNA</th>
<th>$f_0$ (GHz)</th>
<th>NF (dB)</th>
<th>$S_{21}$ (dB)</th>
<th>$S_{11}$ (dB)</th>
<th>$S_{22}$ (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2kV Diode ESD</td>
<td>2.46</td>
<td>2.36</td>
<td>14</td>
<td>-18.5</td>
<td>-15.5</td>
</tr>
<tr>
<td>No ESD</td>
<td>2.4</td>
<td>2.77</td>
<td>12.1</td>
<td>-19</td>
<td>-20.7</td>
</tr>
</tbody>
</table>

Reference-2: 5.5GHz LNA+ESD

5.5GHz LNA
2kV ESD
90nm CMOS
$L_{ESD} = 3\text{nH}$
$L_g = 4.3\text{nH}$
$L_s = 0.4\text{nH}$
$R_{ESD} = ?$

These ideal models do NOT work!
No co-design for RF optimization!

Reference Design 2: 5.5GHz LNA+ESD

“...without altering anything to original core LNA design....”?! 
“No significant degradation of core LNA RF performance...”?!

<table>
<thead>
<tr>
<th>90nm</th>
<th>$f_0$ (GHz)</th>
<th>NF (dB)</th>
<th>$S_{21}$ (dB)</th>
<th>$S_{11}$ (dB)</th>
<th>$S_{22}$ (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>No ESD</td>
<td>5.5</td>
<td>2.7</td>
<td>12.3</td>
<td>-10.3</td>
<td>-19</td>
</tr>
<tr>
<td>L-ESD</td>
<td>5.5?!</td>
<td>2.95</td>
<td>13.3</td>
<td>-14.4</td>
<td>-19?!</td>
</tr>
</tbody>
</table>

RF ESD Design Characterization

- Comprehensive & accurate RF ESD characterization:
  - S-parameter measurement,
  - Noise measurement,
  - Q-factor? \( Q = \frac{1}{2\pi f C_{ESD} R_{ESD}} \)
  - Critically affect I/O z-matching of RF ICs!
  - Never trust foundry ESD models yet!

Example-4: RF ESD Characterization

- Most commonly ESD protection structures
  - ggMOS
  - SCR
  - dSCR
  - Diode string: Dx1, Dx2, Dx3, Dx4, Dx5, … Dxn
- Designed and fabricated in 0.35μm BiCMOS
- 2kV/5kV ESD protection
- Design optimization by mixed-mode ESD simulation
- Simulation matches measurement very well
Example-4: 2kV $C_{ESD}$ by SIM & Test

![Graph showing $C_{ESD}$ vs. frequency for different components: SCR, ggNMOS, Dx1, Dx2, dSCR, and a comparison with measurement data.](image)
Example-4: 2kV $C_{ESD}$ by Test

![Diagram showing the ESD capacitance $C_{ESD}$ for different devices as a function of frequency $f$ (GHz). The graph displays the capacitance values at various frequencies for SCR, Dx1, Dx2, Dx3, Dx4, Dx5, and dSCR devices.]
Example-4: 2kV $C_{ESD} \sim$ Size

2kV Layout Size Comparison

- Dx1
- Dx2
- Dx3
- Dx4
- Dx5
- ggNMOS
- SCR
- dSCR

ESD Structures

$C_{ESD}$ (pF)

$D_{x1}$ $D_{x2}$ $D_{x3}$ $D_{x4}$ $D_{x5}$ ggNMOS SCR dSCR

Layout Size (um2)

0 500 1000 1500 2000 2500

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FoM for Overall ESD Design Evaluation

- Each parameter has different/conflicting meaning,
- Optimization by overall ESD design performance,
- Need a new FoM parameter: F-factor

\[ F = \frac{kV}{Size(\mu m^2) \times C_{ESD}(pF) \times NF(dB)} \]

2kV F-Factor Comparison (Measured)
Example-4: Give me the Numbers

- Extracted testing data at 2.4GHz,
- Optimized ESD design by simulation for min-size, min-parasitics,
- Some ESD designs just not good for RF ICs,
- Trial-and-error designs and “rich” experiences do not work here!

☞ You still have to integrate ESD into RF IC designs!!

<table>
<thead>
<tr>
<th>ESD</th>
<th>Dx1</th>
<th>Dx2</th>
<th>Dx3</th>
<th>Dx4</th>
<th>Dx5</th>
<th>ggNMOS</th>
<th>SCR</th>
<th>dSCR</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{ESD}$ (fF)</td>
<td>48.7</td>
<td>26.3</td>
<td>16.3</td>
<td>18.7</td>
<td>21.0</td>
<td>448.3</td>
<td>66.6</td>
<td>42.4</td>
</tr>
<tr>
<td>Size ($\mu$m²)</td>
<td>506</td>
<td>956</td>
<td>1405</td>
<td>1855</td>
<td>2305</td>
<td>1433</td>
<td>396</td>
<td>257</td>
</tr>
<tr>
<td>F (V/μm² pF)</td>
<td>79.4</td>
<td>88.1</td>
<td>88.1</td>
<td>60.6</td>
<td>44.1</td>
<td>3.1</td>
<td>75.0</td>
<td>180.4</td>
</tr>
</tbody>
</table>
RF ESD PROTECTION SOLUTIONS

- No all-fit RF ESD protection design!
- Any ESD protection ⇒ RF ESD
  given ESD-Circuit interactions ↓↓↓

> Goal for RF ESD ⇒ ANY NOVEL structures:
  - Ultra-fast ESD switching,
  - Novel triggering mechanisms,
  - Hi-ESDV/Si ratio,
  - Small size,
  - Low-parasitics,
  - Multiple-mode ESD protection, …
Novel ESD Protection Design Helps
Example-5: A Dual-Direction ESD
Example-6: All-Mode SCR ESD Protection

Example-7: Low-Parasitic Poly-Si SCR ESD Excellent Prediction

- 0.35μm SiGe BiCMOS.
- 3.2kV HBM ESD protection level using a small 750μm² poly-Si SCR
- A high F-factor of 42
- The lowest reported $C_{ESD}$ of ~92.3fF.
- Adjustable $V_{t1}$.

Xie, et al, "A New Low-Parasitic Polysilicon SCR ESD Protection Structure for RF ICs",
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Example-7: Design Splits

<table>
<thead>
<tr>
<th>Structures</th>
<th>SRC_1</th>
<th>SCR_2</th>
<th>SCR_3</th>
<th>SCR_4</th>
<th>Diode</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Dimensions</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>W (μm)</td>
<td>75</td>
<td>75</td>
<td>30</td>
<td>75</td>
<td>150</td>
</tr>
<tr>
<td>N⁺ Length (μm)</td>
<td>2.3</td>
<td>2.3</td>
<td>2.3</td>
<td>2.3</td>
<td>3.0</td>
</tr>
<tr>
<td>P⁺ Length (μm)</td>
<td>1.6</td>
<td>1.6</td>
<td>1.6</td>
<td>1.6</td>
<td>3.0</td>
</tr>
<tr>
<td>S (μm)</td>
<td>0.8</td>
<td>2.4</td>
<td>0.8</td>
<td>0.8</td>
<td>0.8</td>
</tr>
<tr>
<td><strong>Measurements</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vₜ₁ (V)</td>
<td>11.0</td>
<td>15.0</td>
<td>11.0</td>
<td>9.0</td>
<td>-</td>
</tr>
<tr>
<td>Vₜ₂ (V)</td>
<td>5.5</td>
<td>9.6</td>
<td>5.4</td>
<td>5.0</td>
<td>-</td>
</tr>
<tr>
<td>Vₜ₂ (V)</td>
<td>15.5</td>
<td>15.3</td>
<td>13.8</td>
<td>20.00</td>
<td>13.5</td>
</tr>
<tr>
<td>Iₜ₂ (A)</td>
<td>2.1</td>
<td>1.4</td>
<td>1.5</td>
<td>2.8</td>
<td>1.1</td>
</tr>
</tbody>
</table>
Full-Chip ESD Protection Scheme-1

- Full-chip ESD protection principles:
- Set up a low-R discharging path between ANY two pads,
- Estimate Ron in the longest path – worst case,
- Solution 1:
- A pad + clamp scheme

Full-Chip ESD Protection Scheme-2

- Using a common ESD discharging path,

New ESD+RFIC Co-Design Method

- ESD-induced parasitics is a BIG deal to RF IC design. It corrupts the critical RF I/O matching and causes RF IC performance degradation,
- Foundry-provided ESD structures are generally not optimized for minimized parasitics and sizes,
- Don’t trust the so-called ESD SPICE models and parameters provided by foundries yet,
- Using the foundry ESD model in RF simulation shows NO effect; but testing shows substantial specs shift from post-simulation.
- New ESD-RFIC co-design method is critical to ESD protected RFIC designs.

- Sorry, due to IEEE copy right rules, slides for the new ESD-RFIC Co-Design Method and related examples cannot be disclosed here until after it is presented at IEEE RFIC in June 2008. please go to the RFIC08 Proceedings for details.

Summary

• ESD failure is a killing factor to ICs,
• On-chip ESD protection required for ICs,
• RF/AMS ESD design is very challenging,
• ESD affects RF IC performance significantly:
  ✓ RF ESD design optimization for minimum parasitics,
  ✓ RF ESD design characterization is critical,
  ✓ RF+ESD co-design is important & feasible!
• CMD ESD design is extremely challenging
• ESD design prediction by mixed-mode simulation
REFERENCES


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