Analog-to-Digital Converters for Software Definable Radios

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Analog-to-Digital Converters for Software-Definable Radios

Intro
- Radio architecture considerations
- ADC limitations

Case Study #1: Discrete-Time $\Sigma\Delta$ with Multi-bit Quantizer
- Architecture
- Circuit Design
- Measurements
- Alternate approaches

Case Study #2: Pipelined Redundant-Signed-Digit (RSD) ADC
- Architecture
- Double-sampling
- Issues
- Measurements

ADCs in other parts of the radio

Conclusions
The Ideal Software-Definable Radio Receiver:

ADC at the Antenna
DSP performs all selectivity and BB processing
Maximum Flexibility
Initial thoughts on power dissipation:

\[ 2 \times F_s = 2 \times P \]

Adding one bit of resolution = 4 * P

**FILTERING IS KEY**

One more bit of resolution only adds 6dB to the ability of the receiver to reject interferers. Filtering is much cheaper!!

Trend towards wider bandwidth modulations with stringent close in blocker specs places incredible demands on ADC design. Usually filtering is easier!!
Now, assume the filtering is sufficient to allow us to ignore aliasing issues.

\[ N = \frac{kT}{C} \quad \text{Thermal noise of switch} \]

\[ FsR_G = \frac{1}{C} \quad \text{Max power transfer condition} \]

\[ N = kT F_S R_G \]

Similar to purely resistive case \[ \text{SNR} = \frac{P_{\text{SIG}}}{kT F_S} \]

Conclusion: Need amplifier before the sampler!
Still assuming we have sufficient filtering, but now a fixed gain in the pre-amp, how much ADC dynamic range do we need?

Requirements vary, but 80 to 100dB of receiver dynamic range is not uncommon nor unreasonable to expect.

This means the ADC must be at least 13 bits. What does that cost?
As stated previously:

\[ P_{\text{ADC}} \propto F_s \]

\[ P_{\text{ADC}} \propto 4^N \]

If an ADC is optimized for low power:
• Each doubling of Fs costs at least 2X power.
• Each additional bit of resolution costs at least 4X power.

An additional bit of ADC resolution buys only 6dB of dynamic range. It is usually more cost effective to provide 6dB of AGC.

This will probably remain the case regardless of improvements in transistor technology, CCD samplers, or MEMS development.
So, now the RF sampling radio looks something like this.

Two more issues:
Switch Linearity
Sampling Jitter
The switch is modeled as a non-linear resistance in series with an ideal switch. The voltage sampled onto the cap deviates from the ideal in proportion to the signal current. The signal current is directly proportional to the signal frequency and the cap size.

\[ \therefore \text{You would like to sample low frequency signals onto small caps.} \]
Sampling Jitter

Phase noise in the sampling instant = increased noise floor.

\[ \text{SNR} \propto \frac{1}{\omega_{\text{sig}}^2 \sigma_j^2} \]

\[ \therefore \text{Again, you want to sample low frequency signals.} \]
A sampler can be thought of as a very non-linear mixer. Almost any imaginable improvement in sampler technology should be accompanied by a similar improvement in mixer technology. For high frequency signals, mixers are generally better behaved and more efficient to implement.

Look Familiar?
Initial Conclusions:

• It is possible to make a very poor performing receiver with a simple sampling circuit at the antenna.

• The idea that an ADC can be put at the antenna and somehow rid a high performance radio of the LNA, BPF, AGC, and MIXER is a pipe dream. At the least, it’s not the most efficient approach.

• The direct conversion approach is a good one for exploiting today’s ADC technology and provides a good platform for migrating to future ADC architectures.

• Two new technologies that may improve ADC performance and thus relax requirements on the above mentioned blocks are:


  Continuous time and/or multi-bit $\Sigma\Delta$

• Tunable filters at the front end are key to multi-band receiver and will probably arrive first.
Direct Conversion/Baseband Sampling

- Line-up includes pre-select filter, at least one mixer with the final mixer being quadrature and placing final IF at or near DC, LPF, AGC, and ADC followed by additional digital selectivity and demodulator.
- Moderate flexibility.
- Wide range of ADC requirements 4-15Bits 100KHz-10GHz.

ADC Type - Pipeline, Flash, Folding, and Sigma-delta.
Fundamental limits of ADC resolution and speed.

Below 100kHz sampling rate, thermal noise limits ADC resolution for a given signal power. At higher sampling rates sampling jitter limits resolution regardless of signal power.
Advances in ADC performance enable more flexible radio architectures.

- Below 1GHz sampling rates, state of the art ADC’s available today are at or near the performance limit corresponding to 0.5pS sampling jitter.
- Improvement has been slow - about 1.5 bits at any given sampling rate over the last 8 years. [Walden, IEEE Comm. Magazine Feb. 1999]
What type of ADC is best for DCRCV?

Well, it depends...

Different resolutions and bandwidths call for different ADC architectures.

![Diagram showing ENOB vs. Sampling Rate for different ADC architectures: Flash, Sigma-Delta, Pipeline, Folding, SAR. The diagram includes ENOB values of 24, 20, 18, 16, and 12, and sampling rates from 100K to 26.2G. The x-axis represents Sampling Rate, and the y-axis represents ENOB.]
Focus on $\Sigma\Delta$ and Pipeline ADCs.

- Each architecture is starting to invade the territory of the other.
- Pipeline converters have acceptance for wide bandwidth (>10 or 20MHz) applications as long as latency is not an issue.
- Digital calibration techniques are making pipelines feasible for resolutions > 12 bits but the required digital circuitry consumes Si (best at <90nm process nodes).
- Matching issues tip the scale in favor $\Sigma\Delta$ over pipeline for resolutions > 10-12 bits and bandwidths up to a few MHz and process improvements are pushing up the sampling speeds.
- $\Sigma\Delta$ Bandwidth is inherently programmable at the expense of SNR.
Case Study #1:

Switched-Capacitor Multi-Bit Sigma-Delta ADC

Application
System design
Dynamic Element Matching Technique
Circuit design
Test results

Motivation:

Single ADC to satisfy all cellular requirements:

- Handheld power dissipation (10’s of mW)
- 0.18u CMOS part (Dual Gate Oxide process with MIM Cap)
- Variable and agile resolution

<table>
<thead>
<tr>
<th>Standard</th>
<th>Frequency (kHz)</th>
<th>Resolution</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMPS</td>
<td>15</td>
<td>15 bits</td>
</tr>
<tr>
<td>GSM</td>
<td>180</td>
<td>13 bits</td>
</tr>
<tr>
<td>CDMA</td>
<td>615</td>
<td>12 bits</td>
</tr>
<tr>
<td>W-CDMA</td>
<td>1900</td>
<td>11 bits</td>
</tr>
</tbody>
</table>
Agility requirement points toward low order loop
High-resolution quantizer needed for W-CDMA
Make flash power $\approx$ integrator power $\Rightarrow$ 6-bit flash ADC
Mismatch noise from DAC = $N_D$

Quantization Noise = $N_Q$

Mismatch noise from DAC is unshaped.
System Design - $\Sigma\Delta$ Architecture

Feedback DAC element mismatch limits overall linearity of multi-bit sigma-delta ADC.

Multi-Bit Delta-Sigma Modulator
Noise-Shaped Dynamic Element Matching

EX: DAC states for code sequence 3, 2, 4
Circuit Design:

\[
Y = X z^{-2} + N_Q(1-z^{-1})^2
\]
Bottom-plate sampling
No correlated double-sampling
Judicious use of high voltage devices.

35 Å NMOS
70 Å (DGO) NMOS (stage 1 only)
70 Å (DGO) TGATE
Offset chopping reduces high-frequency spurs by up to 20 dB (measured)
Chopping necessitates low impedance resistor string.
2.5 mm

- DACs
- DEM
- Flash ADC
- ADC_I
- ADC_Q
- Integrators
Input shorted – 20 MHz clock

Signal power (dB)

Frequency (Hz)
Small degradation from 1/f noise.
46 MHz clock; FS-3dB, 2.1MHz signal
23 MHz clock; FS–3dB, 17.4kHz signal
Shotgun Learning

6/18/08

Test Results

SINAD and SFDR

- AMPS: 95 dB
- CDMA: 70 dB
- GSM: 81 dB
- CDMA: 77 dB
- W-CDMA: 70 dB

SINAD & SFDR for a 17.4 kHz input

SFDR: 95 dB max
AMPS: 95 dB
GSM: 81 dB
CDMA: 77 dB
W-CDMA: 70 dB
(46 MHz clock)
# Test Results - Summary

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.18u CMOS, MIM CAP, 35/70 A DGO</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>2.7 V</td>
</tr>
<tr>
<td>Active Area</td>
<td>1.4 mm²</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>30 mW (20A/10D) at 23MHz Fsamp</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>50 mW (30A/20D) at 46MHz Fsamp</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bandwidth</th>
<th>W-CDMA</th>
<th>CDMA</th>
<th>GSM</th>
<th>AMPS</th>
</tr>
</thead>
<tbody>
<tr>
<td>SINAD</td>
<td>70 dB</td>
<td>77dB</td>
<td>81 dB</td>
<td>92 dB</td>
</tr>
<tr>
<td>ENOB</td>
<td>11.3</td>
<td>12.5</td>
<td>13.2</td>
<td>15</td>
</tr>
<tr>
<td>SFDR</td>
<td></td>
<td></td>
<td>95 dB MAX</td>
<td></td>
</tr>
</tbody>
</table>
Alternate Approaches:

T. Stockstad, D. Garrity, US patent #6,087,969

If sufficient dynamic range cannot be achieved by adjusting the oversampling ratio alone, additional filtering can be added either within or after the first ΣΔ modulator.
Continuous-Time Sigma Delta ADCs:


- discrete-time feedback DAC reduces clock jitter sensitivity
- a great deal of research both in academia and industry is currently focused in this area

74dB/83dB/92dB in a 3.84MHz/1.228MHz/200kHz bandwidth with power dissipation of 4.5mW/4.1mW and 3.8mW respectively!!!
Continuous-Time $\Sigma\Delta$ RxADC

### Specifications:
- **Input Clip Point:**
  1.8 Vpeak, differential.
- **SNDR:**
  65 dB over 4 MHz for DVB,
  80 dB over 2 MHz for WCDMA,
  90 dB over 200 kHz for GSM-EDGE.
- **Clock:**
  360 MHz for DVB,
  312 MHz for WCDMA,
  52 MHz for GSM-EDGE.

### Continuous-Time Input:
- **Low Power:** 10mW (4 mA) (dominated by WCDMA).
- **Inherent Anti-Aliasing:** 5th-Order.

### Clock Jitter Sensitivity:
- **Reduced by discrete-time feedback.**
- **Reduced by OSR.**
Continuous-Time SD RxADC

Specs: BW = 10MHz
fs = 184Mhz
SNR = 70dB
Case Study #2:

Pipelined RSD (1.5 bit-per-stage) ADC

Application
System design
Circuit design
Test results
ADC for Wireless LAN radio receiver (and other broadband radio receivers):

✓ two ADCs required (I and Q)
✓ low power dissipation (no separate track and hold)
✓ 0.13\(\mu\)m digital CMOS with isolated p-well option (for isolation)
✓ high performance with low cost
✓ specific requirements:
  
  no more than 0.6mm\(^2\) per ADC
  sample rate > 20MHz
  10 bit resolution
  SINAD > 56dB
  power < 25mW per ADC
  SFDR > 65dB
10 bit 20Ms/s Pipelined RSD ADC
RSD Stage Block Diagram and Transfer Function

Block Diagram

Robertson Diagram
RSD ADC: Offset Effects

Comparator Offset

Loop Offset
RSD stage single-ended block Diagram:

Note that since RSD comparator accuracy requirements are significantly reduced, a separate track and hold is usually not required for resolutions up to 10 bits and input signal frequencies up to ~ 50MHz or so.
Pipelined RSD ADC layout:
Expected Results (simulated):

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.13(\mu)m CMOS, Fringe CAP, 70 A DGO</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>3.3 V</td>
</tr>
<tr>
<td>Active Area</td>
<td>0.53 mm(^2)</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>24 mW at 20MHz Fsamp</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>input bandwidth</th>
<th>10MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>SINAD</td>
<td>57dB</td>
</tr>
<tr>
<td>ENOB</td>
<td>9.2</td>
</tr>
<tr>
<td>SFDR</td>
<td>65 dB</td>
</tr>
</tbody>
</table>
What if you need to go faster but you can’t spend anymore power or area:

double-sampled pipeline ADC - theory of operation

Simplified single-ended block diagram of a double-sampled RSD gain stage:

Single ended version of improved gain stage with associated timing diagram.

* Note that the input voltage is still sampled at the original system clock rate, while the internal circuitry is operating only half as fast. This allows a corresponding factor of 2 reduction in the supply current required for the gain stage opamp.
operation of single ended version of improved gain stage:

odd input during p1o

gain stage during p1e

gain stage during p2e with signal hi high

gain stage during p2o with signal lo high
conventional non-overlapping clock generator for SC circuits

For a clock period of 50ns:
- clkin
- p1 high for 20ns
- p1d
- p2 high for 17.5ns
- p2d
frequency response (fft) of 10-bit ADC output (hanning window)
non-overlapping clock generator for time-interleaved SC circuits

D. Garrity, D. Bersch, US patent 5,886,562
frequency response (fft) of 10-bit ADC output (hanning window)
Experimental Results:

10 bit, 40Ms/s double-sampled pipelined ADC
measured output spectrum for a 10 bit 40Ms/s ADC

SNR = 60.5 dB
SNDR = 59.7 dB

dBFS

normalized frequency

BW=8,500,000
## Measured Results:

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.5(\mu)m BiCMOS, Double-Poly Capacitor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>3.0 V</td>
</tr>
<tr>
<td>Active Area</td>
<td>2.5 mm(^2) (20% more than original ADC)</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>100mW at 40MHz Fsamp (20% more)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>input bandwidth</th>
<th>20MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>SINAD</td>
<td>57dB</td>
</tr>
<tr>
<td>ENOB</td>
<td>9.34(at 2MHz), 8.5 (at 20MHz)</td>
</tr>
<tr>
<td>SFDR</td>
<td>60 dB</td>
</tr>
</tbody>
</table>
Alternate approach: Single ADC that processes I and Q Channels
(garrity et al. US patent #7,064,700)

Simplified block diagram of prototype I/Q sampling ADC. The resolution and required clock phases for each stage are listed in parentheses.

Simplified timing diagram for I/Q sampling ADC
Measured Results:

plot of ADC layout (1.727mm\(^2\) total area and per-ADC area of 0.864mm\(^2\)):
Measured Results:

I-Channel ADC Response to a 2.4MHz sine wave:

SNR = 58.2dB
SNDR = 55.6dB
Measured Results:

Q-Channel ADC Response to a 2.4MHz sine wave:

SNR = 57.2dB

SNDR = 55.2dB
Measured Results:

I and Q channel ADC SNR Response vs Input Frequency:

![Graph showing measured I and Q ADC SNR versus input frequency](image-url)
<table>
<thead>
<tr>
<th></th>
<th>I-channel ADC</th>
<th>Q-channel ADC</th>
</tr>
</thead>
<tbody>
<tr>
<td>resolution</td>
<td>10 bits</td>
<td>10 bits</td>
</tr>
<tr>
<td>sample rate</td>
<td>40MHz</td>
<td>40MHz</td>
</tr>
<tr>
<td>Input voltage range</td>
<td>1 Vpp differential</td>
<td>1 Vpp differential</td>
</tr>
<tr>
<td>peak SNR/SNDR</td>
<td>58.5/56.5 dB</td>
<td>58.5/56.5 dB</td>
</tr>
<tr>
<td>DNL</td>
<td>-0.48/0.58 lsb</td>
<td>+/- 0.5 lsb</td>
</tr>
<tr>
<td>INL</td>
<td>+/- 1 lsb</td>
<td>+/- 1 lsb</td>
</tr>
<tr>
<td>power consumption</td>
<td>25mW</td>
<td>25mW</td>
</tr>
<tr>
<td>technology</td>
<td>90nm CMOS</td>
<td>90nm CMOS</td>
</tr>
<tr>
<td>area</td>
<td>0.864mm²</td>
<td>0.864mm²</td>
</tr>
</tbody>
</table>
Other parts of the radio: Power Control System

Levels output power into varying load

Polar architecture shown for reference

Digital implementation

- Minimizes analog area
- Simplifies multi-mode support
  - Example
    - GSM + EDGE + WCDMA

>10 bits resolution
> 1Ms/s
~ 1mW power
< 0.1mm² in 0.18μm CMOS
single-stage cyclic ADC architecture

recent example:
• 10 bit, 1Ms/s, TSMC 0.18mm
• 1.38mW from 3V, 0.085mm$^2$
• measured performance on upcoming slides
D. Garrity, P. Rakers, US patent 6,535,157
measured output spectrum for a 10 bit 1 Ms/s Cyclic ADC

8192 POINT FFT
FSAMPLE = 1.1 MSPS
FIN = 101.9 kHz
SNR = 60.7 dB
SNDR = 60.5 dB
THD = -69.8 dB
SFDR = 74.8 dB
measured 10 bit 1Ms/s Cyclic ADC differential nonlinearity

\[ \text{dnl}^+ = 0.11 \text{ LSB} \]
\[ \text{dnl}^- = -0.22 \text{ LSB} \]
## Measured Results:

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.18(\mu)m (TSMC)CMOS, MiM CAP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>2.7 V</td>
</tr>
<tr>
<td>Active Area</td>
<td>0.085 mm(^2)</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>1.3 mW at 1MHz Fsamp</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>input bandwidth</th>
<th>500kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>SINAD</td>
<td>60dB</td>
</tr>
<tr>
<td>ENOB</td>
<td>9.76</td>
</tr>
<tr>
<td>INL/DNL</td>
<td>+/- 0.39 lsb, +/- 0.22 lsb</td>
</tr>
</tbody>
</table>
Conclusions:

• For bandwidths up to 10MHz or 20MHz and dynamic ranges of greater than 70dB, $\Sigma \Delta$ based ADCs are the most promising.

• Continuous-time $\Sigma \Delta$ ADCs are especially promising for the higher end of the $\Sigma \Delta$ bandwidth range.

• For bandwidths greater than several 10’s of MHz and resolutions up to 12 bits or so, pipelined ADCs are a good choice for low power and low cost.

• Improvements in dynamic range/power/bandwidth come about mainly from ADC architectural breakthroughs and secondarily from IC process advances.


Suggested Reading & Bibliography


