



SAN FRANCISCO BAY AREA
NANOTECHNOLOGY COUNCIL

Tuesday – December 15, 2009 Seminar

Title: Embedded Molecular Nano-Capacitor

Speaker: Dr. Ritu Shrivastava, VP Manufacturing Technology, ZettaCore Inc.

An IEEE 125th Anniversary Celebration Event
Co-sponsored by these IEEE Santa Clara Valley Chapters



Date: Tuesday December 15, 2009

Time: Registration, networking & light lunch 11:30am. Presentation & Q/A 12:00 to 1pm

Location: National Semiconductor Bldg E-1 CMA Room. 2900 Semiconductor Drive, Santa Clara, CA

Map: See two pages below

Cost: IEEE Members and Students \$5. Non-IEEE Members \$10

Please RSVP at our web site: www.ieee.org/nano

Talk Abstract:

This talk will discuss the use of charge storage molecules at the nanoscale with molecular attachments to metals, to form a capacitor which is unlike any conventional capacitor. This nanoscale device uses a different physical mechanism which involves utilizing charge storage in self assembled monolayers (or polymers). The capacitor can be integrated using silicon IC wafer technology to achieve an ultrathin capacitor, but there are other potential implementations also possible for non-semiconductor based applications, such as embedded capacitor formation for PCB multi-layer IC substrates. The uniqueness of this approach is to achieve capacitance/area values in a thin profile which are unachievable using conventional dielectrics in the frequency range of application. This is a new type of device which exhibits a unique frequency dependent capacitance. Advantages and uniqueness of the device will be discussed for potential user community.

Speaker Biography:

Ritu Shrivastava is currently Vice President of Manufacturing Technology at ZettaCore Inc., where he is responsible for guiding the company's molecular technology integration and manufacturing strategy, as well as building relationships with semiconductor manufacturers and foundries. He came to ZettaCore from Alliance Semiconductor Corp., where he was responsible for technology development, initial ramp-up, and volume manufacturing of SRAM, DRAM and Flash memories, as well as mixed signal and logic products. Prior to Alliance, Dr. Shrivastava worked at Cypress Semiconductor for more than 10 years. He began his industry career at Mostek Corporation/United Technologies, after serving on the faculty at Louisiana State University. He earned a BSEE and an MSEE from the Indian Institute of Science, and a Ph.D. in Electrical Engineering from Louisiana State University. He is a Fellow of IEEE, and an inventor in 23 issued US patents related to various semiconductor technologies. Shrivastava also served as CMOS technology editor for IEEE Transactions on Electron Devices.

Directions To National Semiconductor Campus

□ Address: Building E Auditorium, 2900 Semiconductor Dr., Santa Clara, CA 95051

□ If heading South on Lawrence Expressway from Highway 101:

✖1a: Turn RIGHT (west) onto **Kifer Road**.

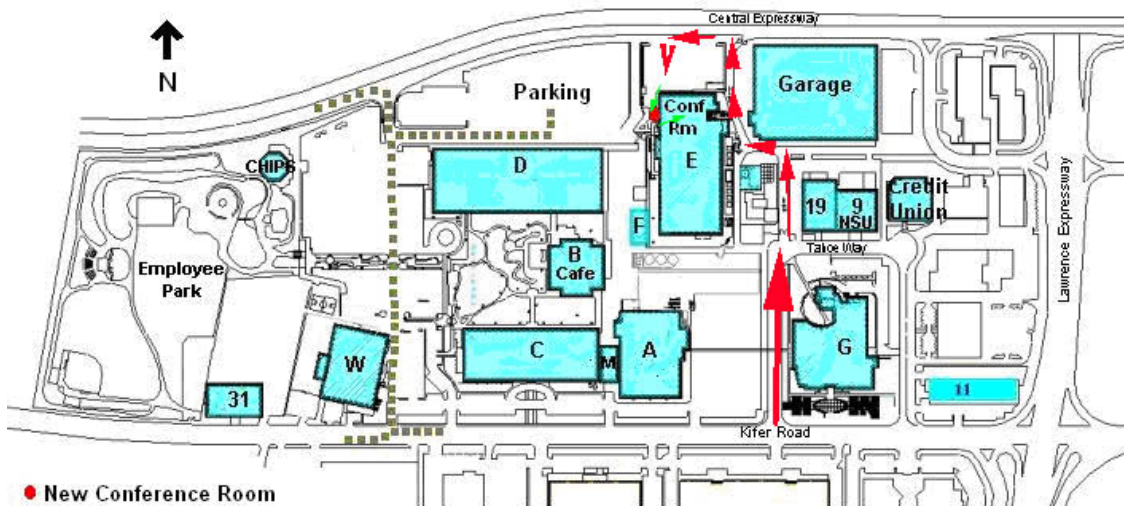
□ If heading North on Lawrence Expressway from El Camino Real:

✖1b: Turn LEFT (west) onto **Kifer Road**.

□ Then:

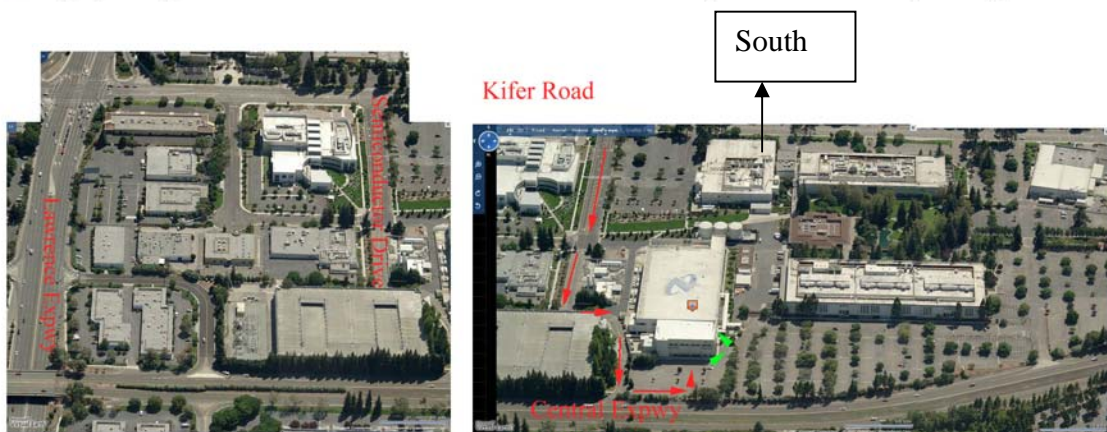
✖2: Turn RIGHT (north) at First Stop Light onto 2900 Semiconductor Drive

✖3: See National Semiconductor Campus Map below (follow red arrows to park; follow green arrows to walk to auditorium entrance).

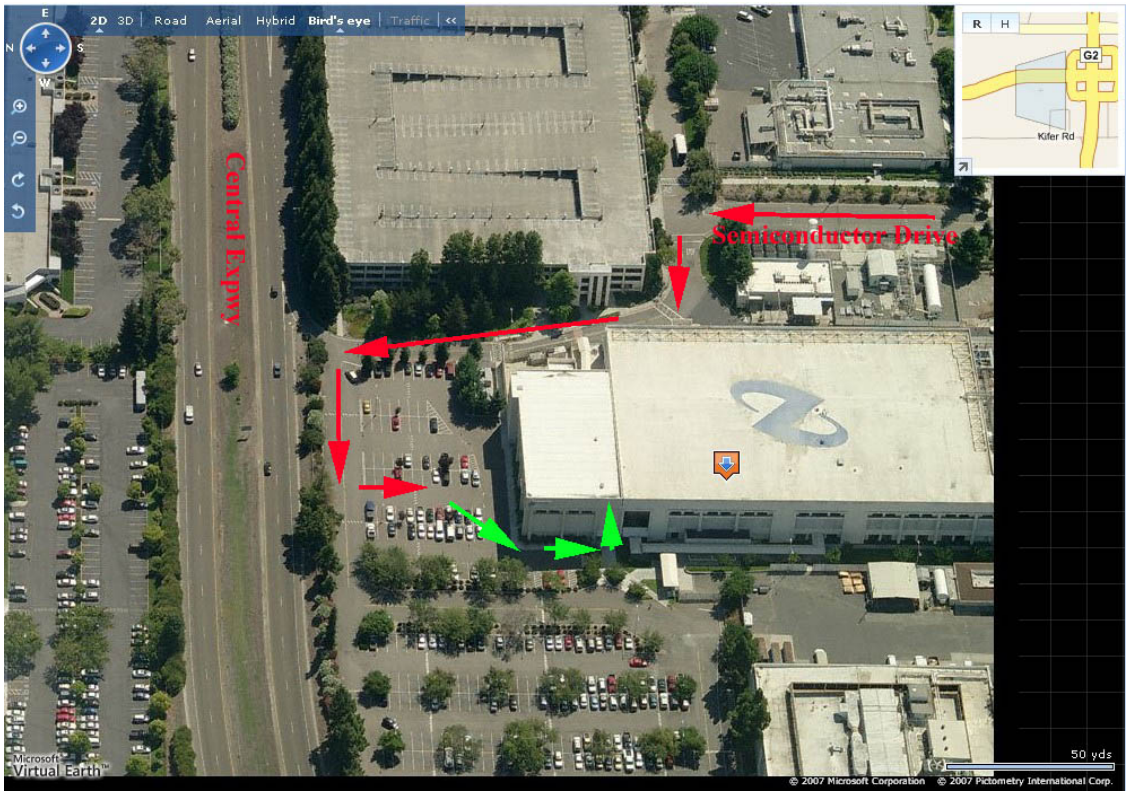


● New Conference Room
(Enter through Bldg E Lobby)

■ Bldg E parking is accessible from both directions of Kifer and driving east on Central Expressway.



Aerial photos looking southward.



Aerial photos looking eastward.