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Job Title : Sr Staff Engineer (PLL)

Field of Interest : Engineering

Full Time/Part Time : Full-Time

Division : Technology - ASIP

Department : ASIP - Anita

City : Fremont

State : California

Description : You will be responsible for developing advanced CMOS PLL's with industry leading performance and features in multi-giga bit per second SerDes and other applications such as fractional synthesis and SSC. You will lead projects that deliver these circuit IP's to the highest standards in the physical IP industry.

You will also provide technical leadership in a team project setting, as well as in customer interface where you can present the competency and benefits of our solutions.

#### Requirements

- BSEE or higher in integrated circuit design. MSEE/PhD preferred.
- > 7 years of CMOS IC design experience in high performance PLL's
- Direct experience and track record in developing advanced CMOS PLL's in giga bit per second data transmission and other application such as fractional synthesis that meet stringent jitter, power, area and SSC requirements
- Must be able to independently specify, model, architect, design, verify and characterize the PLL's to meet required frequency range, jitter, noise conditions as well as power/area budget.
- Familiarity with mainstream PLL circuit design EDA, such as Matlab, Cadence ADE and advanced CMOS processes.
- Familiarity with PHY protocols such as PCIE, SATA, XAUI, DP/HDMI, USB and MIPI is a plus.
- Good communication skill, interpersonal skill and team leadership.

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