# *3G Spells Deconstruction for the Wireless Industry*

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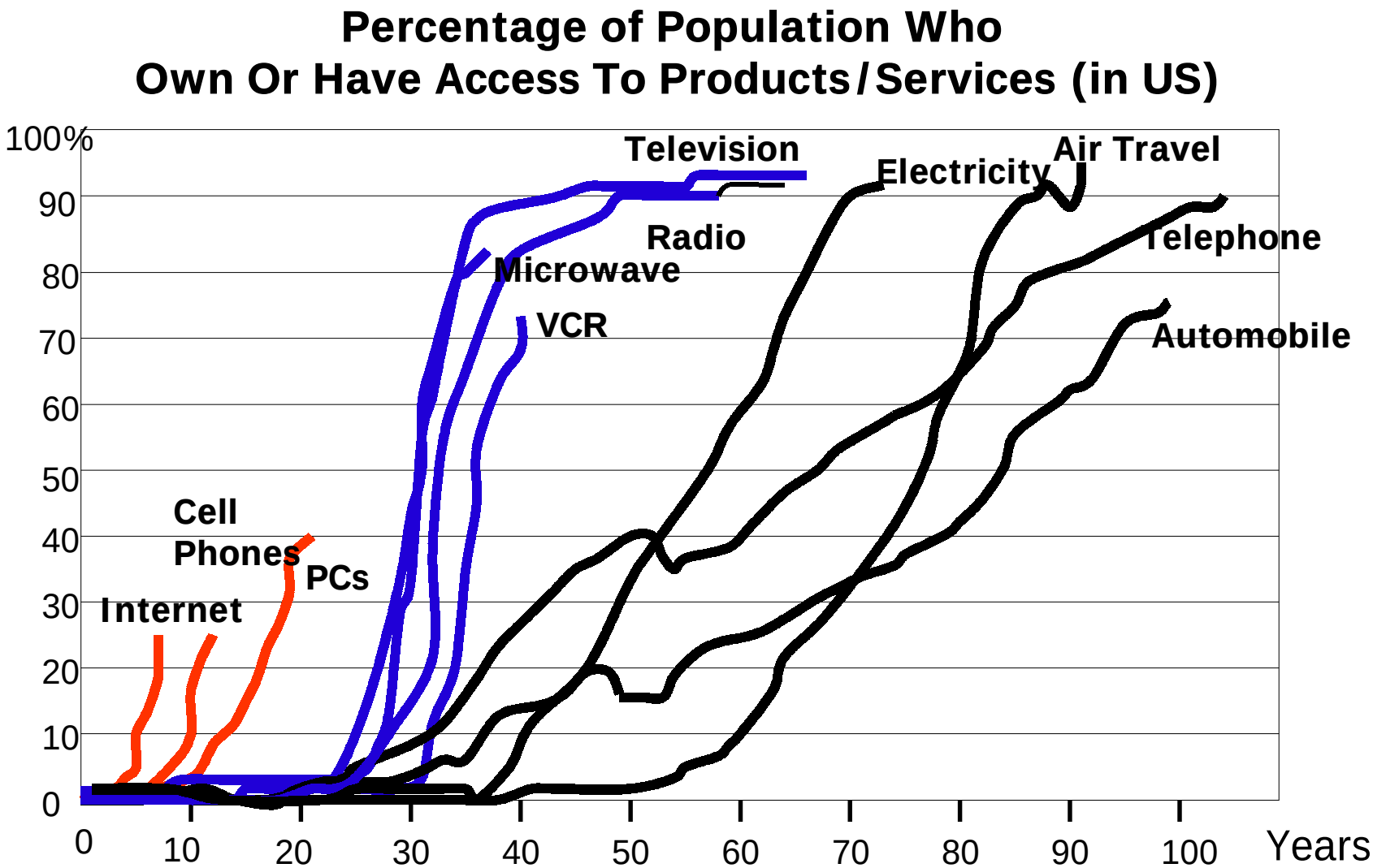
# Outline

- **Introduction**
- **The Vertical Industry Chain**
  - Service Providers
  - Equipment Manufacturers
  - Semiconductor Houses
- **Deconstruction**
- **Enabling Technologies for 3G (oops…>2G)**
- **SW Radio- Myths and Realities**
- **Rules of Competition**

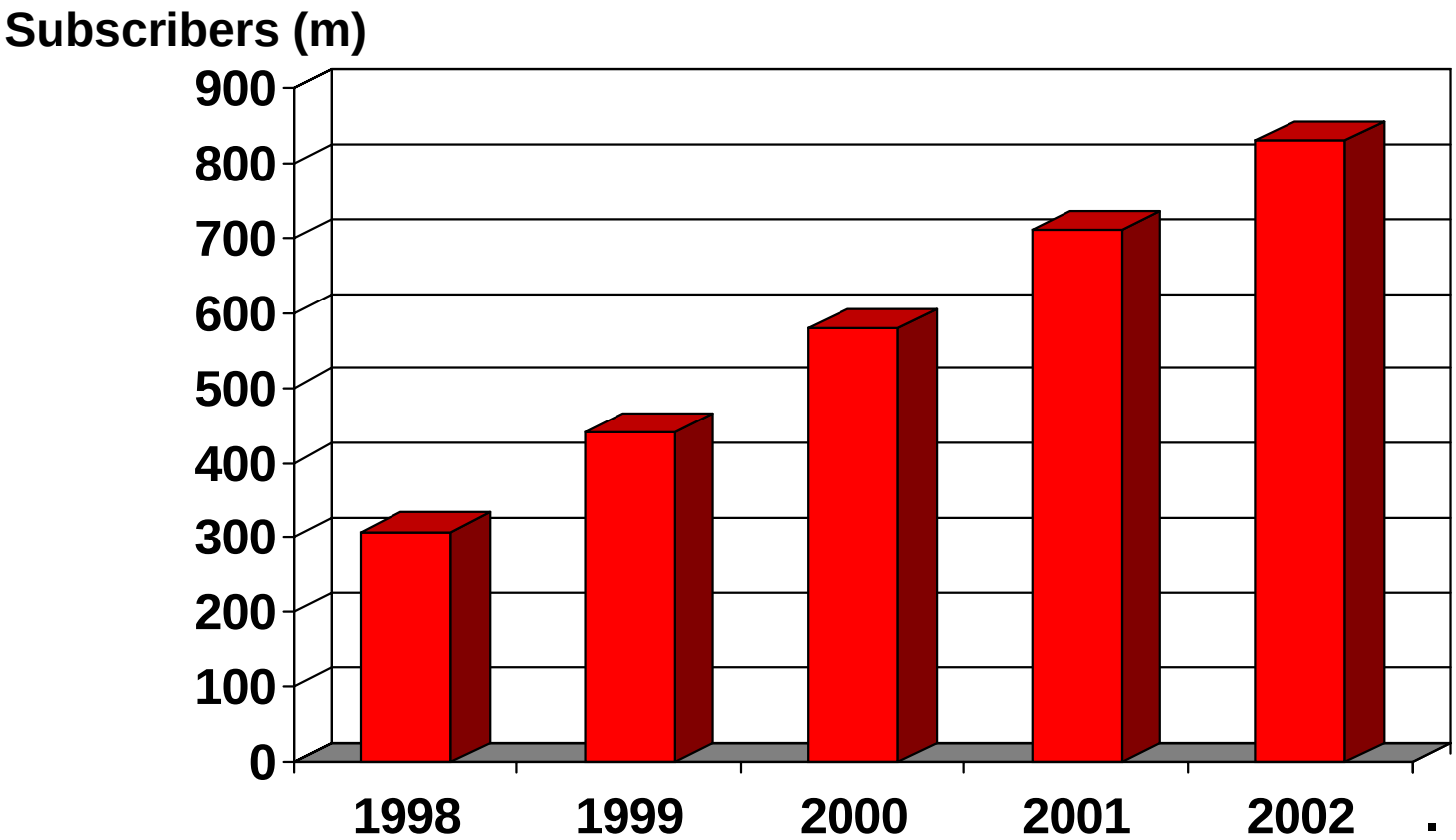
# The Evolution of Consumer Acceptance




Source: C. Farill, 1998

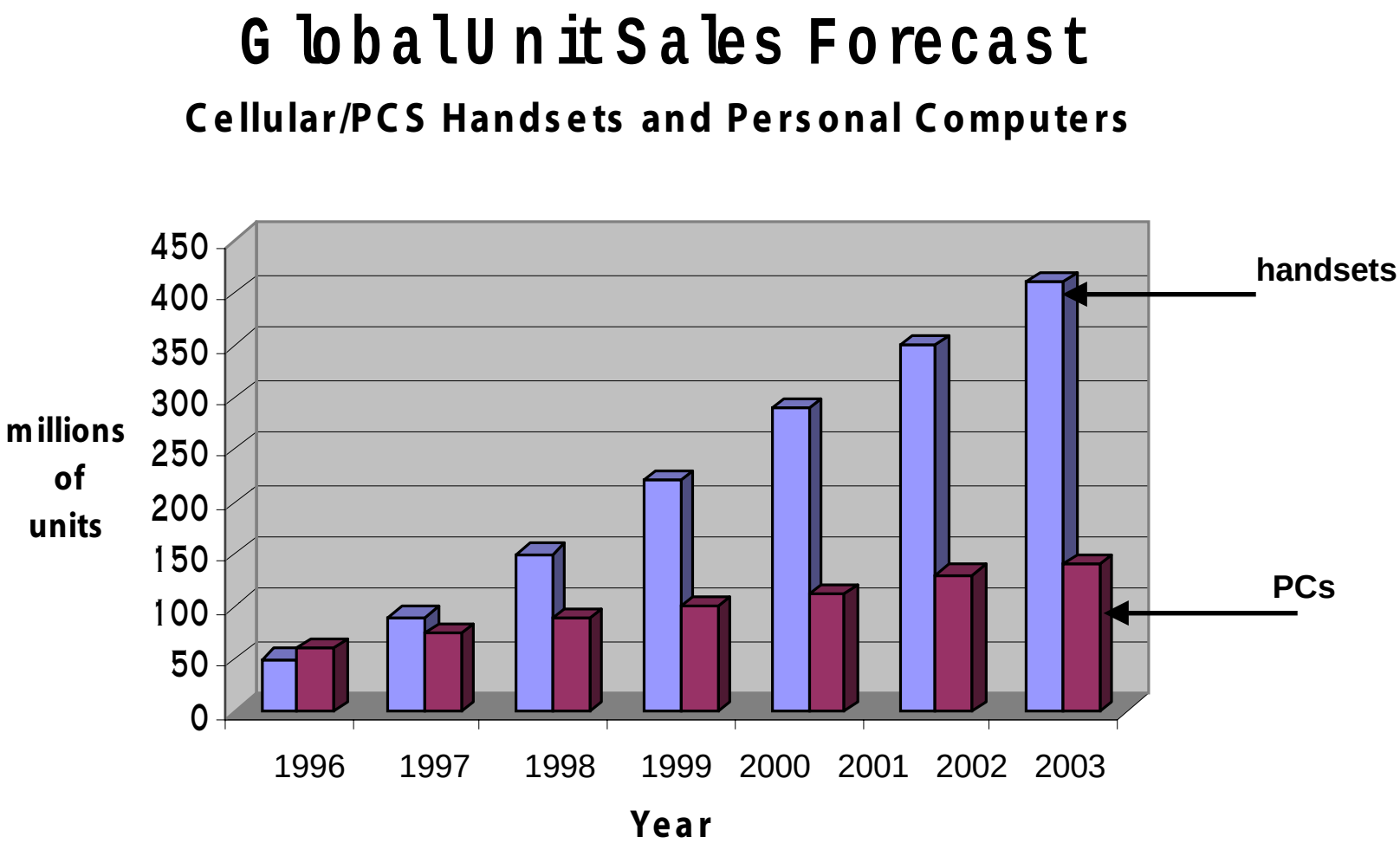
# *Wireless Market Growth*

**Worldwide cellular & PCS subscribers are projected to grow to over 800 million* by 2002.**




*Strategis, Herschel Shosteck, Dataquest, Nokia, Ericsson

# Moving To A Data-Pipe-Centric World

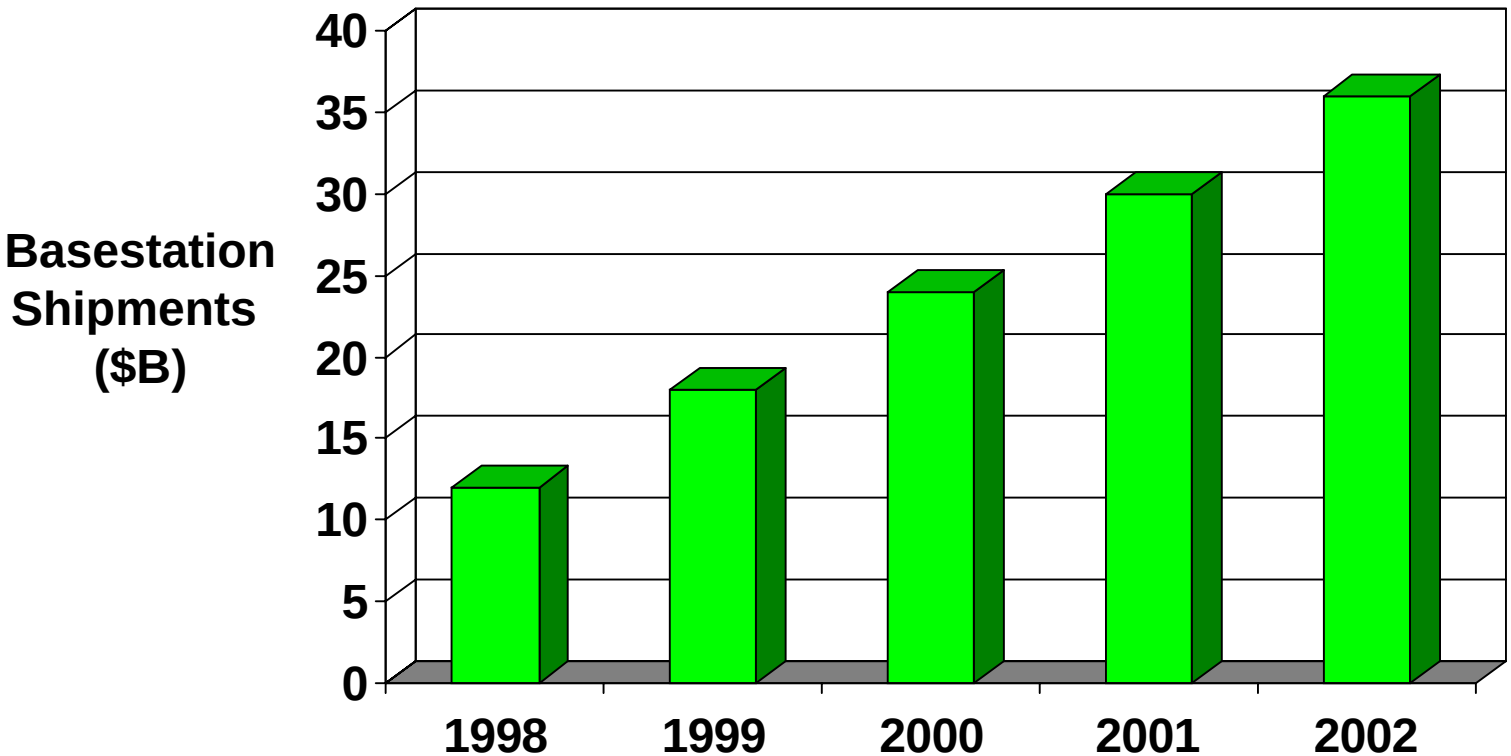



**Handset market is projected to be worth $60 Billion by 2002!**

Source: BT Alex Brown, Morgan Stanley, ITU, Ericsson, Nokia, Strategis
Notes: 1999-2003 are estimates

# *Base Station Shipments*

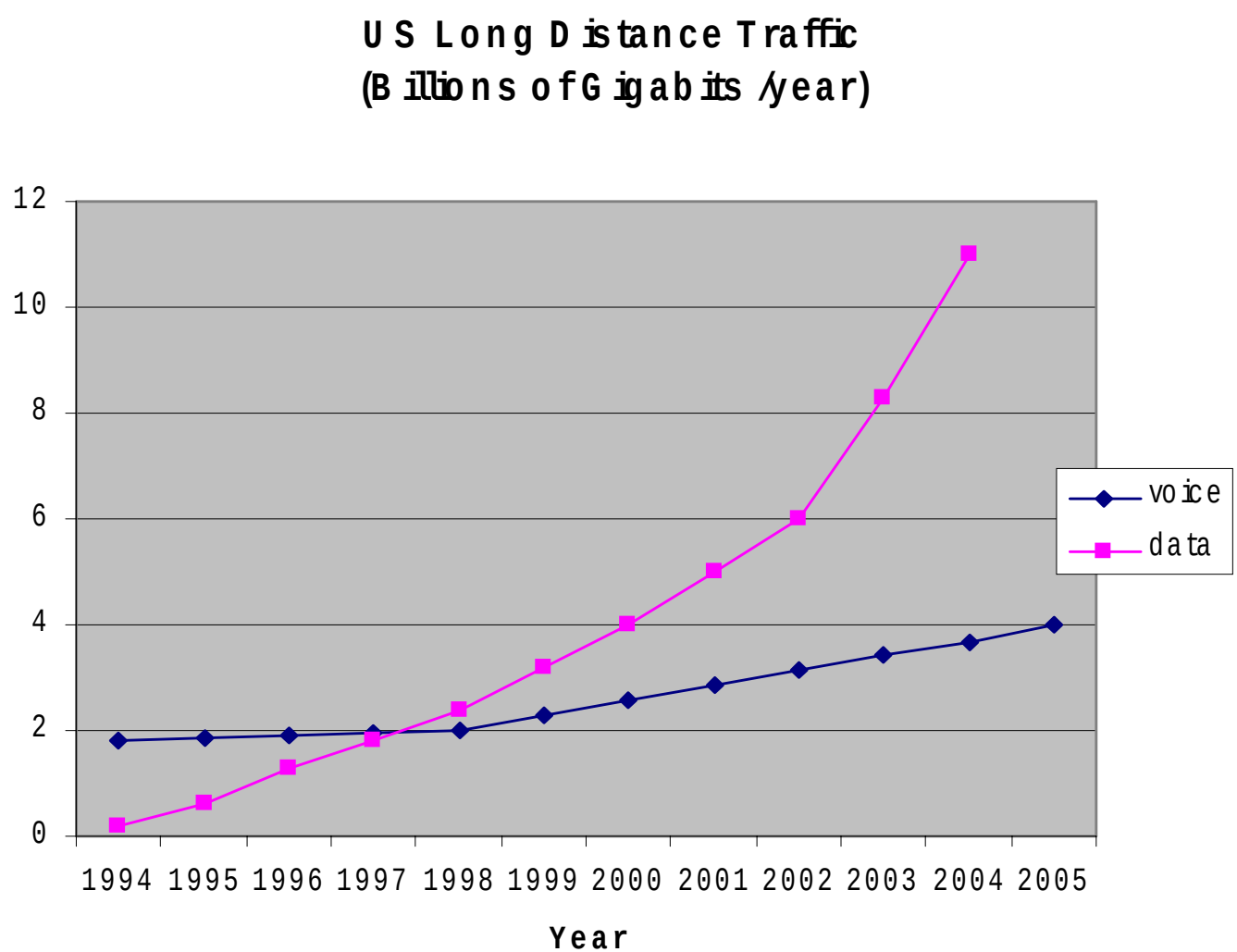
**Network growth will drive sales of base stations and will approach $36B by 2002.**




**Enterprise base stations will drive this market strongly**

*ABI, Dataquest, Nokia, Ericsson

# The Turning Point




Source: BT Alex Brown, Nortel, Lucent, Telcordia

# The Industry Chain


Service Consumer

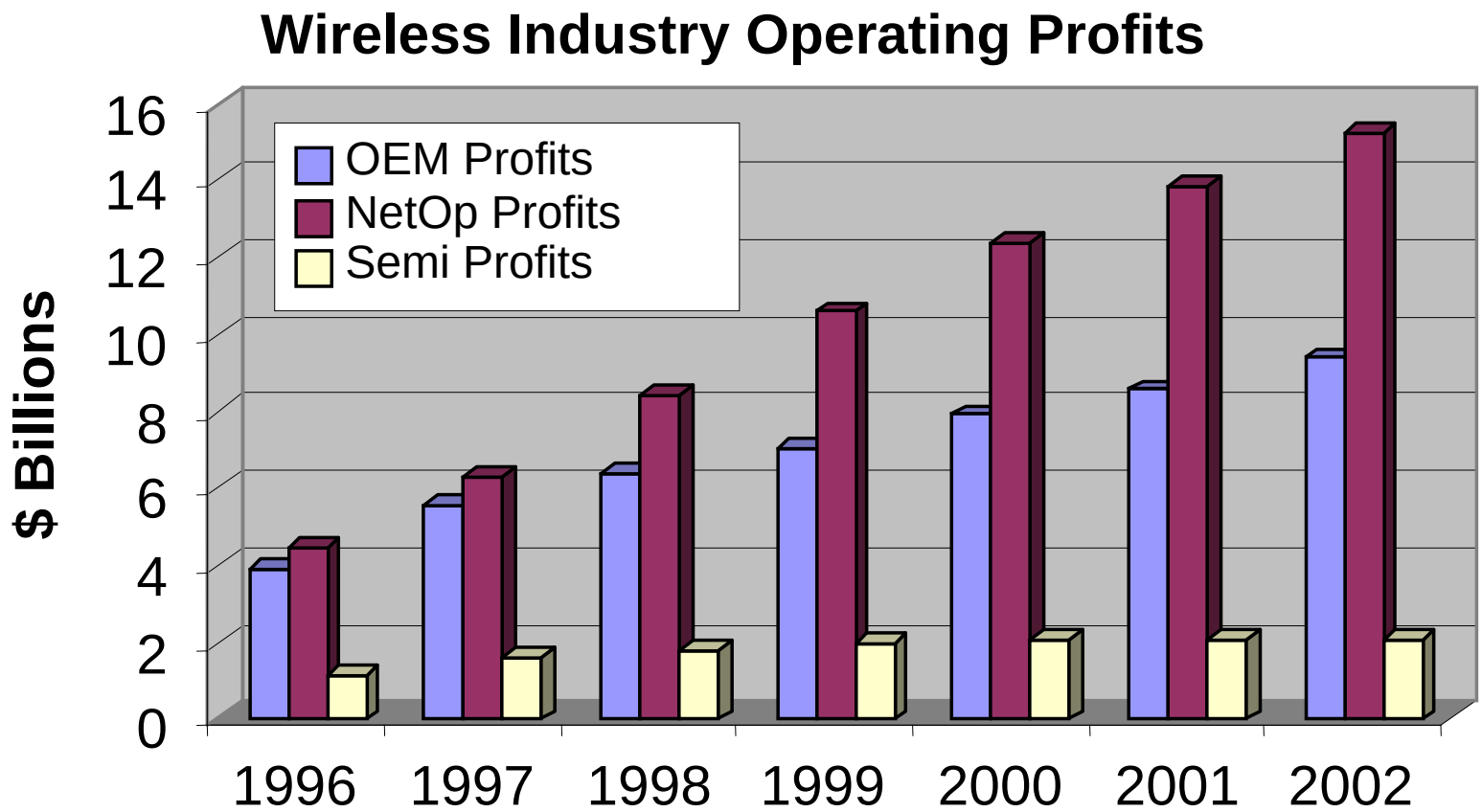
Network Operator

Equipment Manufacturer

Semiconductor House

Enabling Technology Providers

# Profits In This Chain

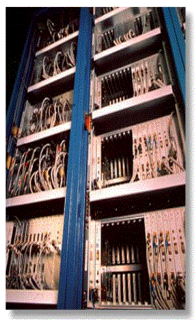



Sources: EMC Database, Salomon Smith-Barney Research, BT Alex.Brown Research, Strategis, Herschel Shosteck Associates, Wireless Industry 10K Reports

# Network Operators

- **It's all about owning the market for global telecom minutes**
  - Wireless will grow to an estimated 25-30% of global telecom minutes [Strategis, 1997]
  - 25% of wireless traffic will be data by 2002
- **Major players have a worldwide plan (function of bal. sheet)**
  - Today, 95+% of network operators= service provider
  - Network Operators
    - Consolidation brings multistandard properties worldwide
    - Infrastructure investment protection
    - Future-proofing handsets
  - Service Operators
    - Evolve to providing value-added services over plant
    - Evolution to a software business model
- **Their suppliers are beginning to compete with them**

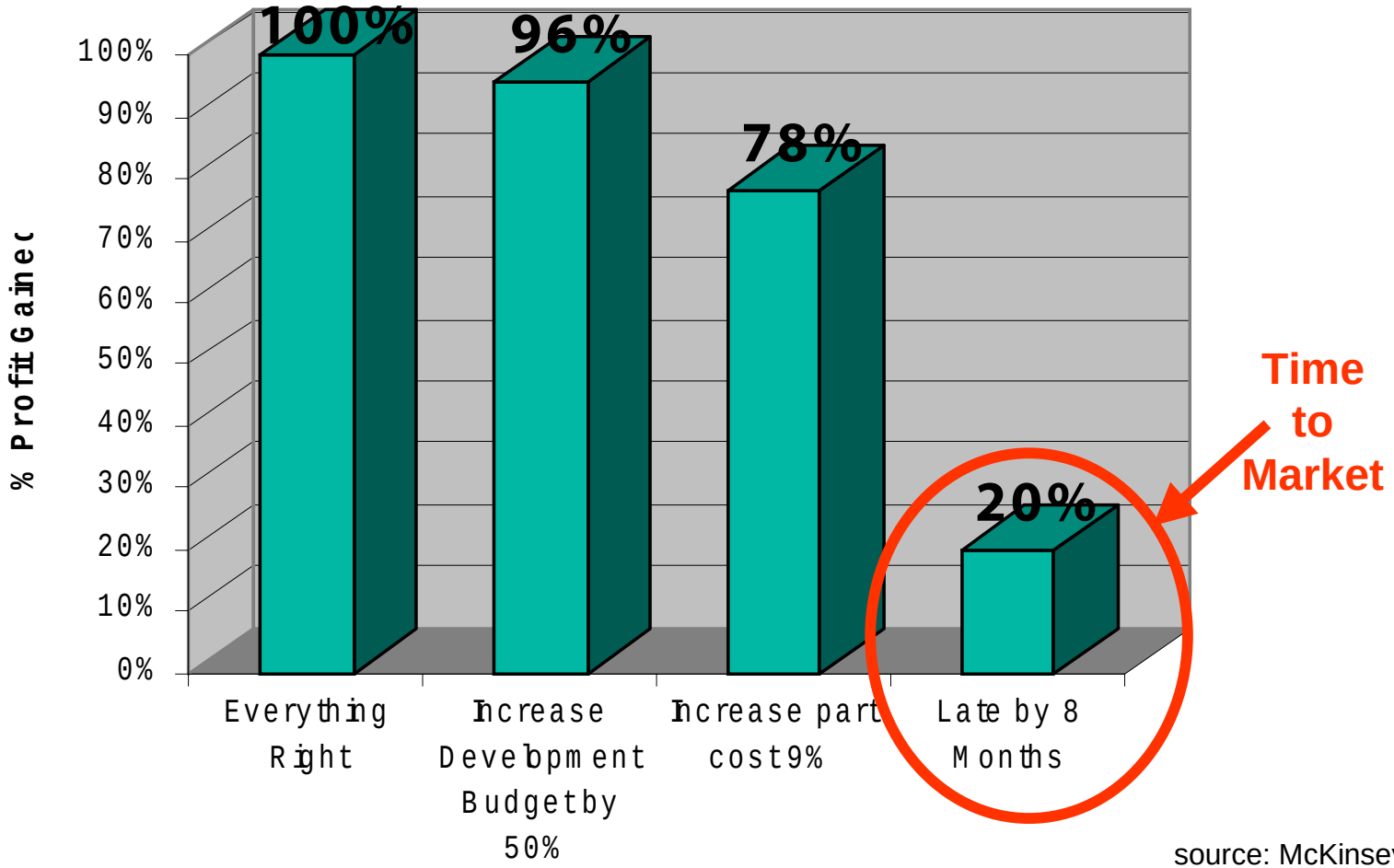
# Equipment Manufacturers




- Equipment manufacturers are facing an explosion in standards
- New standards are driving new product architectures
- New product architectures driving new silicon solutions
- Control of the product <-> control of the product architecture <-> silicon architects in system houses
- Equip manufacturers are financing more and more of their sales-> moving to operating the network

# Equipment Manufacturer Challenges

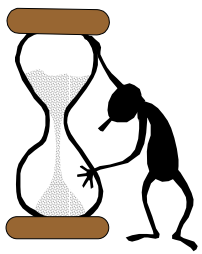
## Winning Means Capturing Profits By Being To Market First!




source: McKinsey & Co.

# Semiconductor Houses…Are Stretched!

- **Every new standard is getting more and more complex**
  - AMPS->GSM 10x
  - GSM->IS-95CDMA 10x
  - IS-95CDMA->UTRA 10x

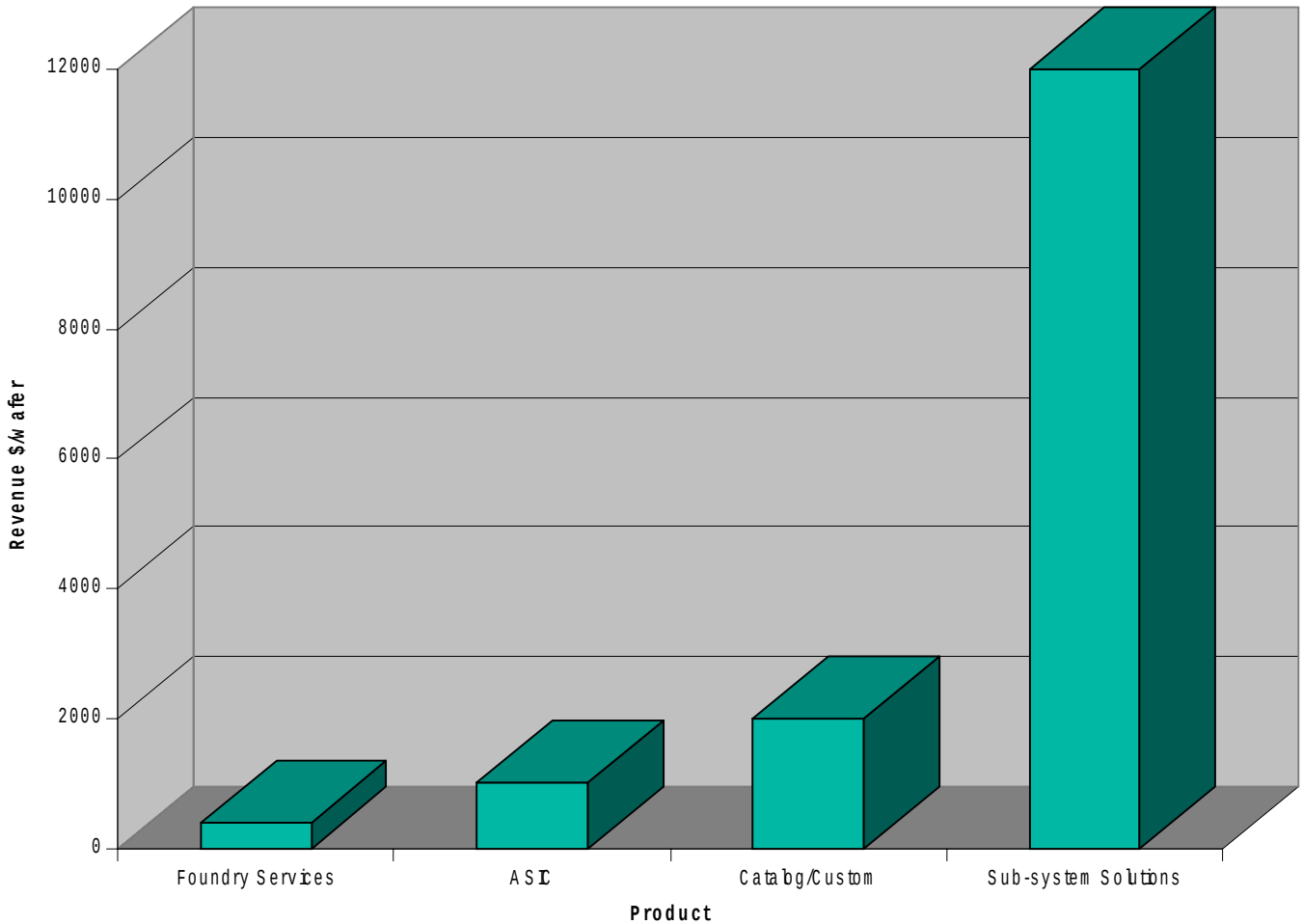


- **The time it takes to design the new standard-specific silicon platform is growing**

- **The wireless system becomes a “commoditized chip” faster**

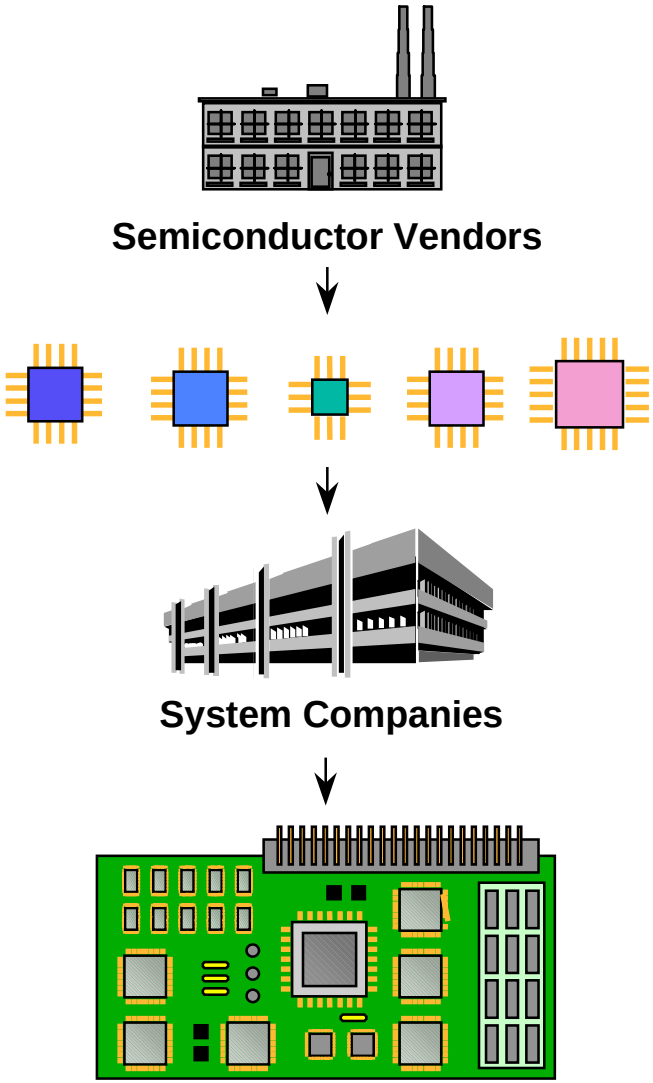
# So What Types of Chips Bring High Margins?

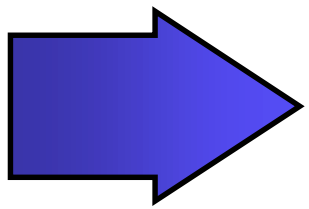
## The Value-Added Chain In System ICs

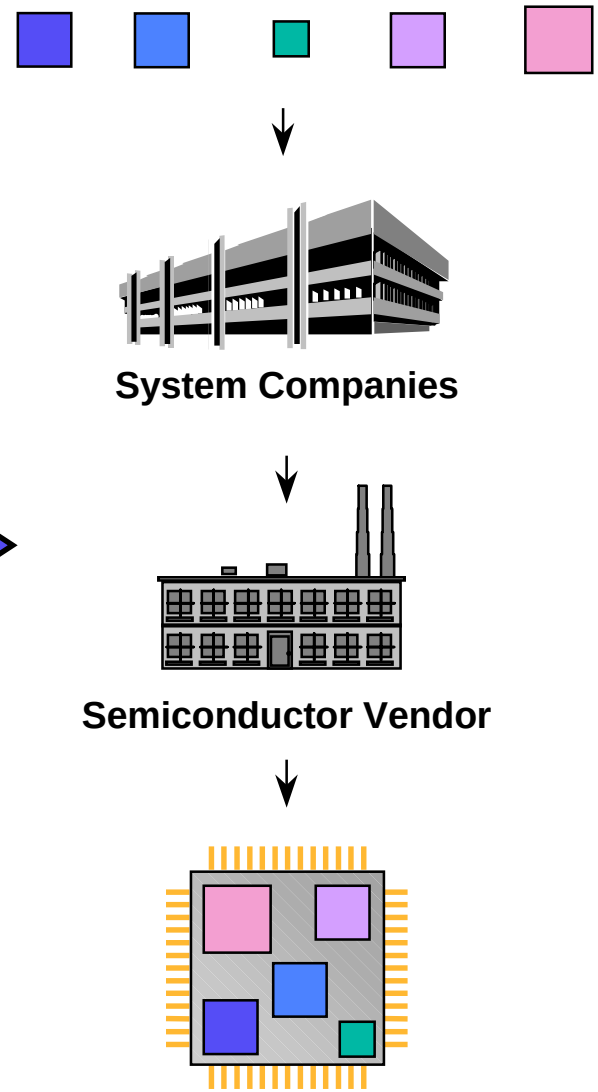



Source: Dataquest, 1998

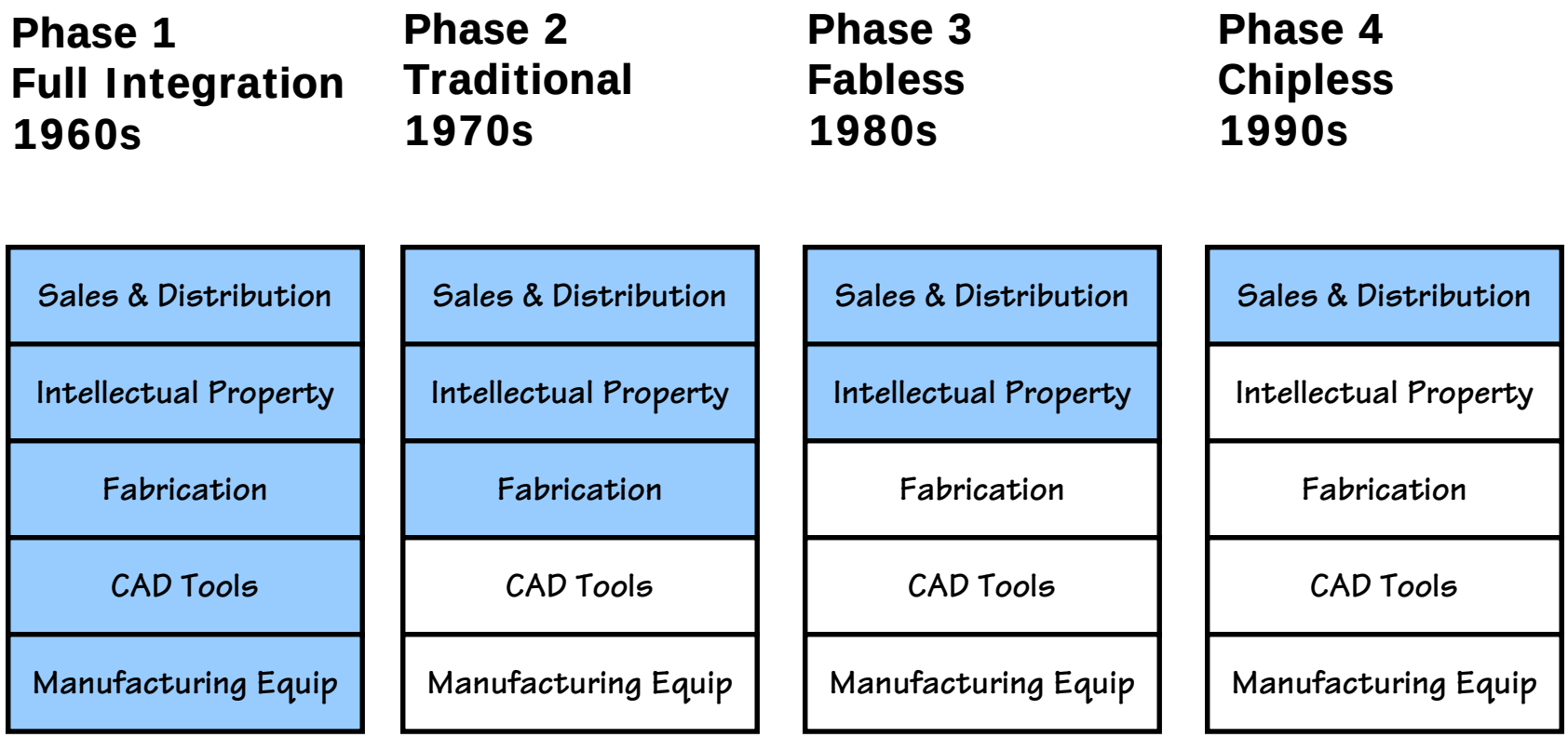
# System-On-A-Chip Design Is Bringing Change





# The Deconstruction of The Semiconductor Industry



# Semiconductor IP Industry

- **A new stage in the evolution of semiconductor industry**
  - semiconductor house
  - fabless semiconductor house
  - fabless, chipless semiconductor house= SIP
- **SIP business model similar to that of software company**
- **Digital SIP companies are establishing the business models**
- **Analog SIP companies are starting up**

# Ingredients for SIP Success

## ❑ Serving A Unique Need In The Market

- Need to systematically deal with critical functionality in product
- System vendors define the need
- Provide key technology differentiator

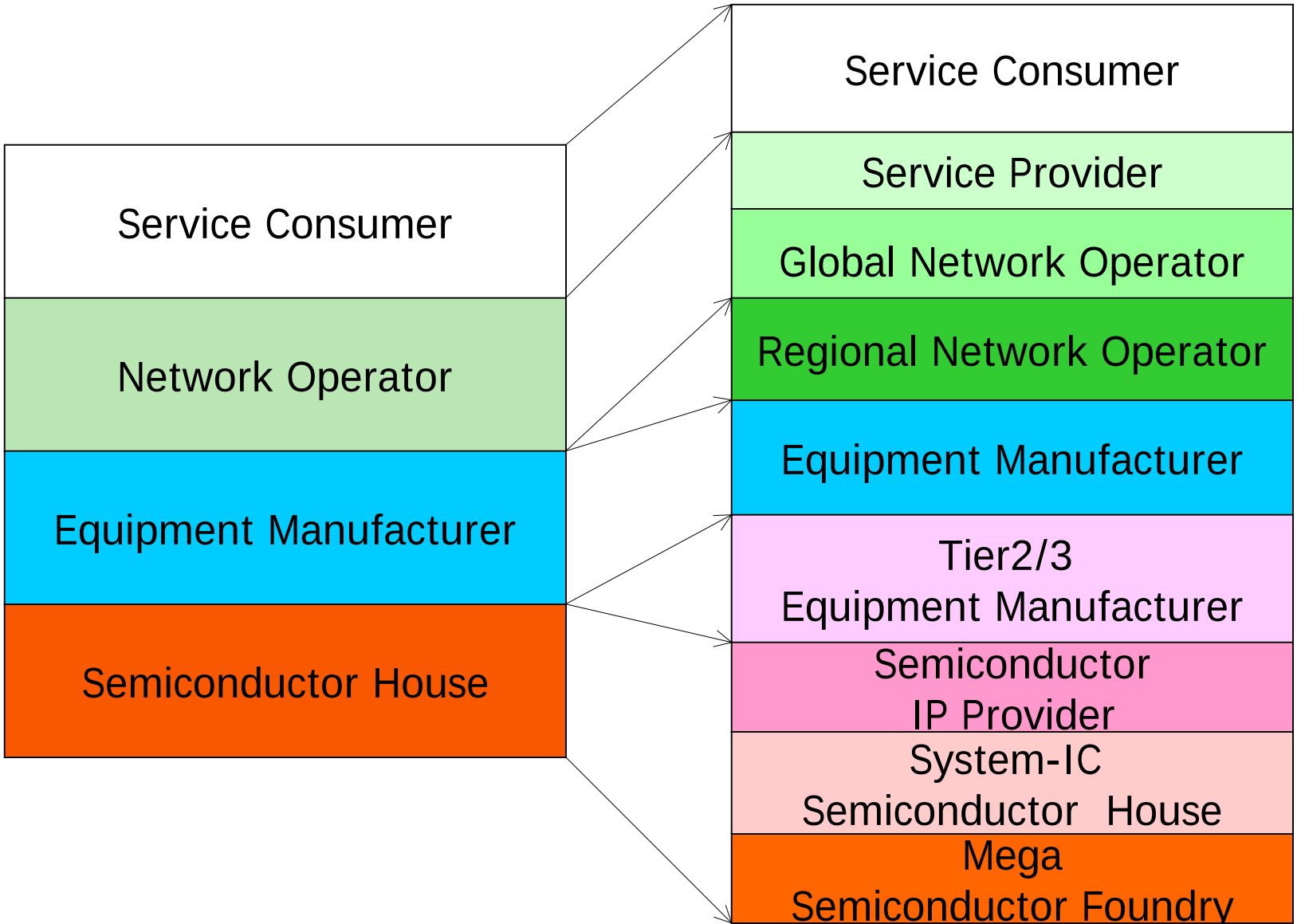
## ❑ Attacking a Large Market

## ❑ Building Significant Barriers to Entry

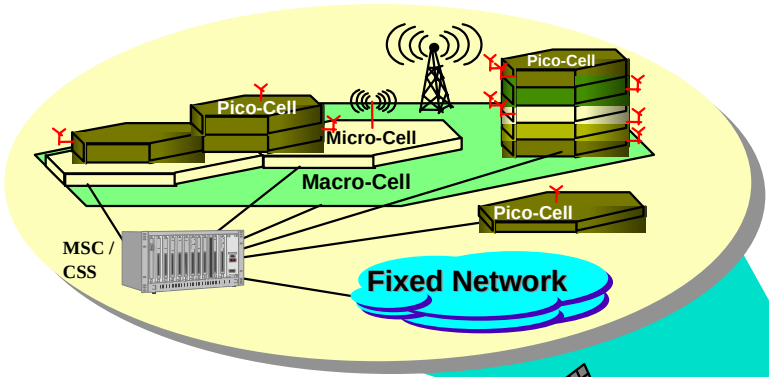
- Unique technology and design methodology
- Offer a substantially better solution at competitive prices
- Substantial and growing patent portfolio

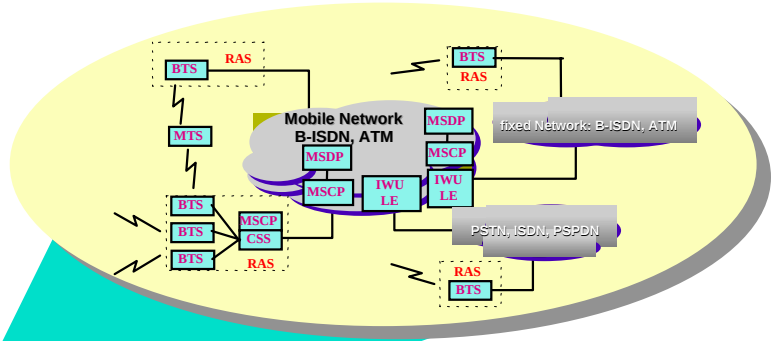
## ❑ Establishing Appropriate Business Models

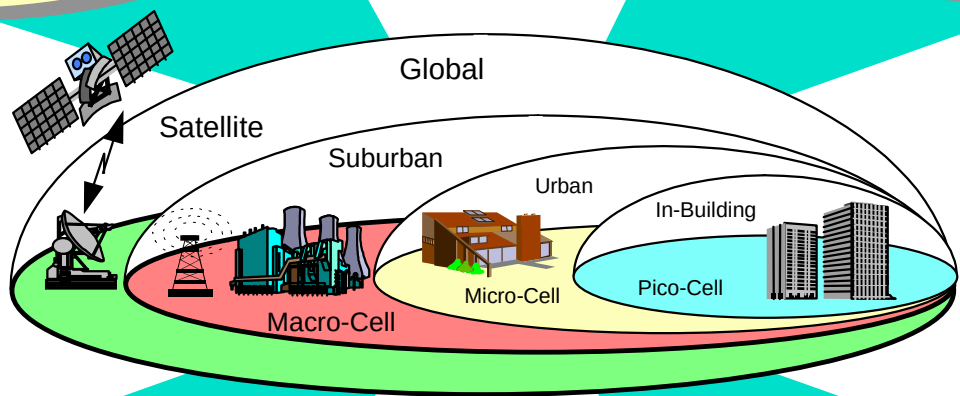
# Post-Deconstruction

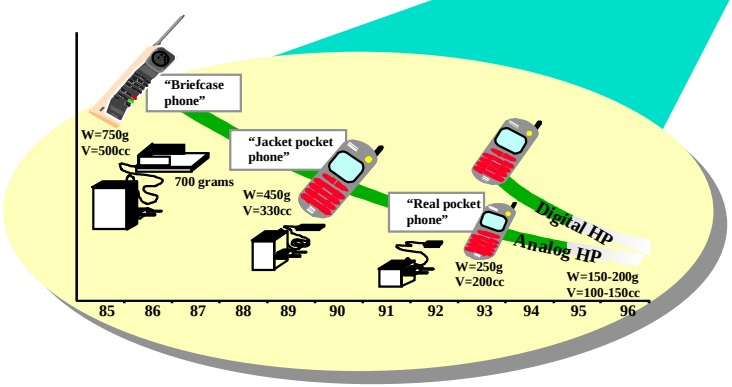


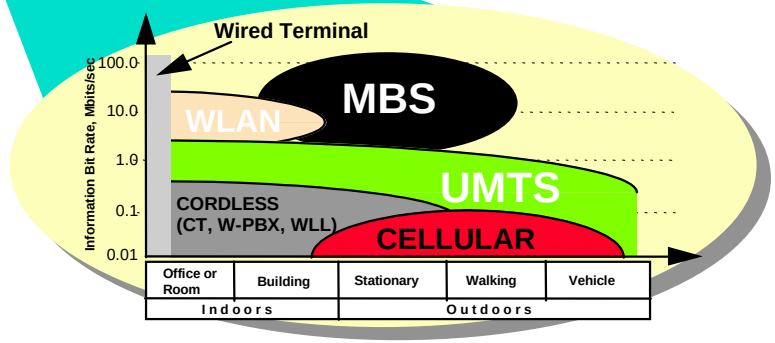
# UMTS



# Cellular Standards

## 2G

- GSM
- DCS1800
- PCS1900
- IS-95
- IS-54B
- IS-136
- PDC

## 2.5G

- GPRS
- HCSD
- IS-95 MDR
- IS-95 HDR
- IS-136 HS

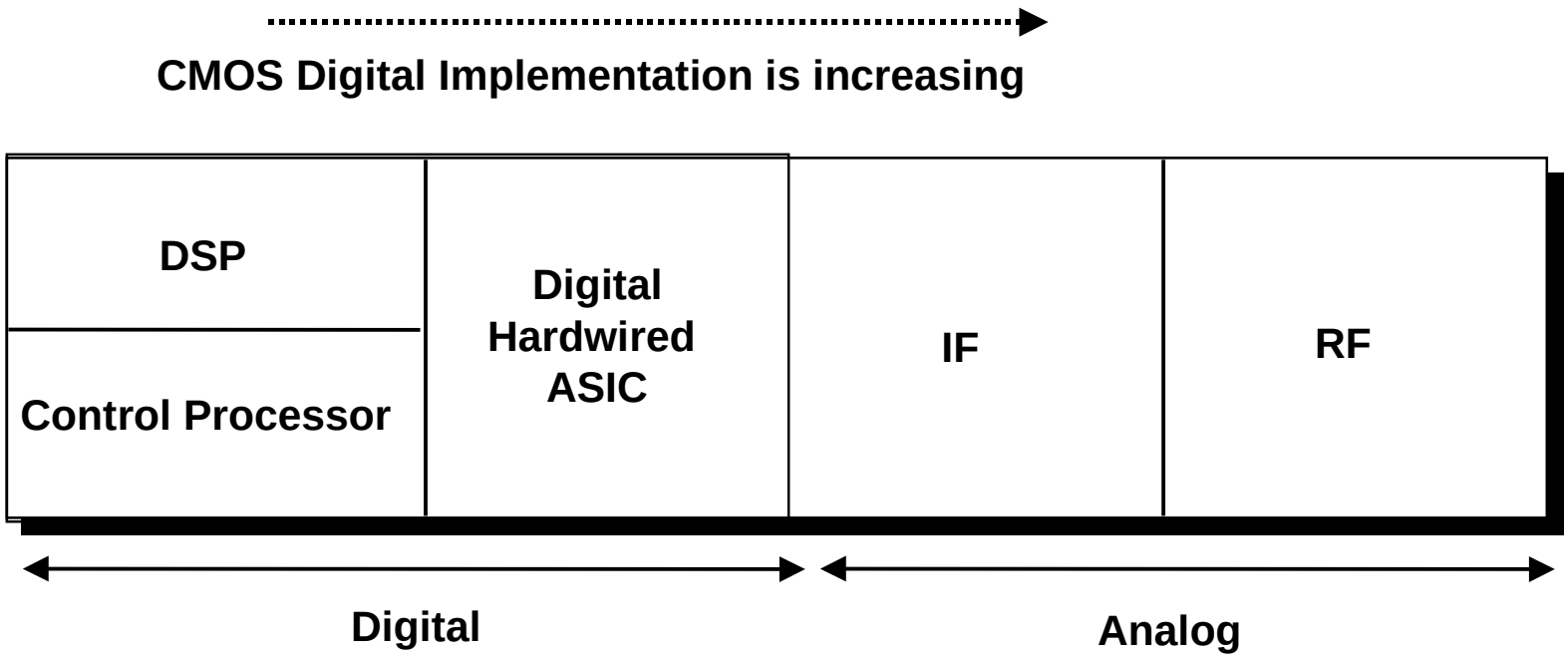
## 3G

- ETSI UTRA
- ARIB W-CDMA
- TIA  cdma2000
- W-TDMA (UWC)

**CIRCUIT**
**VOICE**
**NARROWBAND**

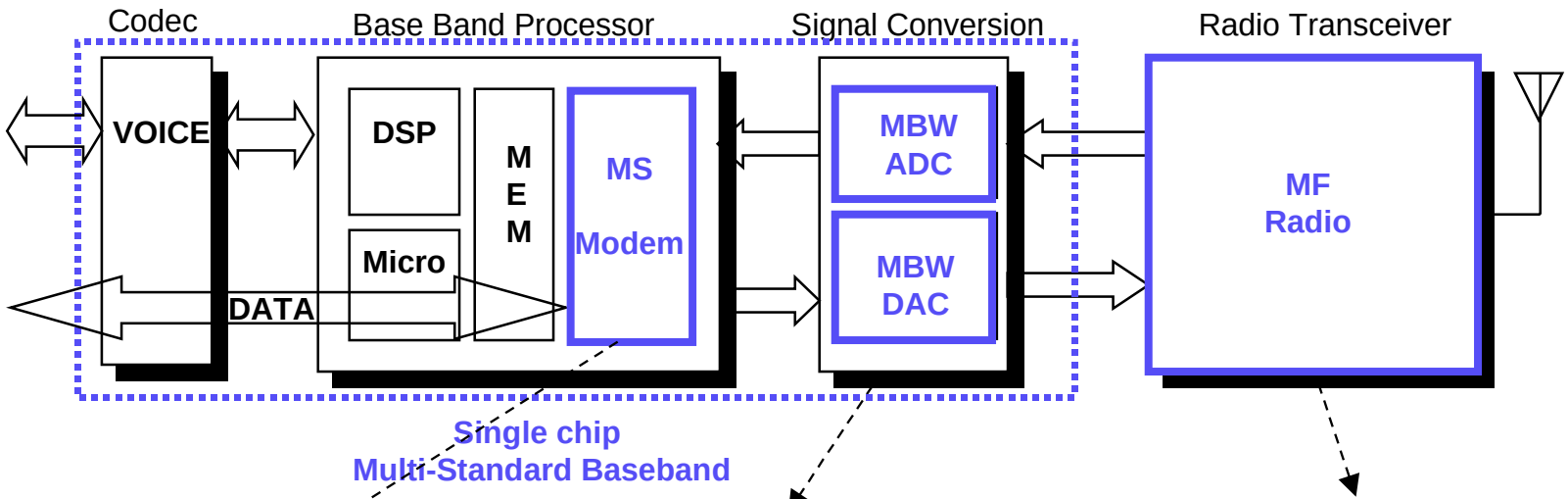
**PACKET**
**DATA**
**WIDEBAND**

# Wireless Hardware Platforms



# Multi-Standard Silicon Architectures

**Current product architectures in common use support single standards -multiple standards, need 3 key issues to be addressed.**




## 1. Multi-Standard Digital Modem

All-digital transceiver capability for multiple standards and scaleable data rates.

## 2. Multiple-Bandwidth Signal Conversion

An ADC/DAC element that is variable in BW and resolution allowing support of multiple standards.

## 3. Multiple Frequency Radio Transceiver

Radio Frequency (RF) section capable of operating over the 800/900/1800/1900/2000 bands.

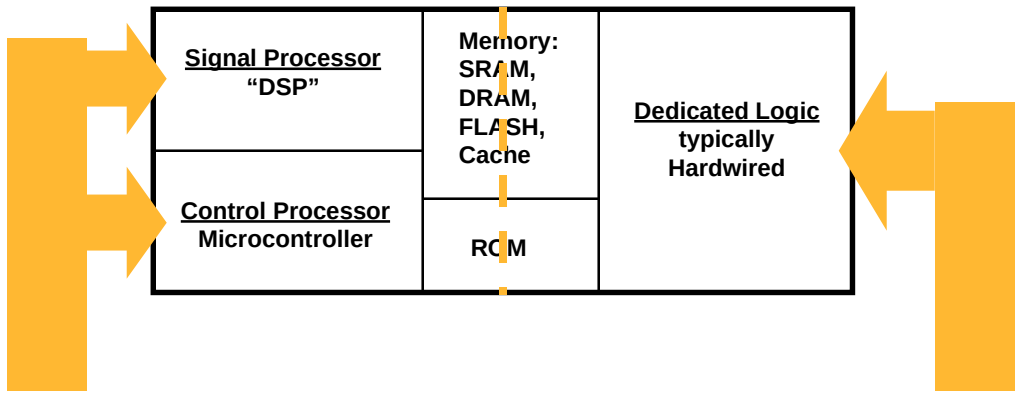
Multiple Bandwidth and multiple carrier issues are being supported BUT, multi-standard receivers and modems are not!

# System Partitioning Tradeoffs

System tradeoffs in partitioning are based on the following criteria:

**Software Instruction Processing**
Maximize Flexibility
Minimize Development Time
Minimize Risk
Maximize Design Reuse

**Hardwired Logic Processing**
Maximize Speed
Minimize Power Consumption
Minimize Cost
Minimize Size




Programmable, low-speed signal processing and control functions

**Signal**
Speech Coding
Encryption

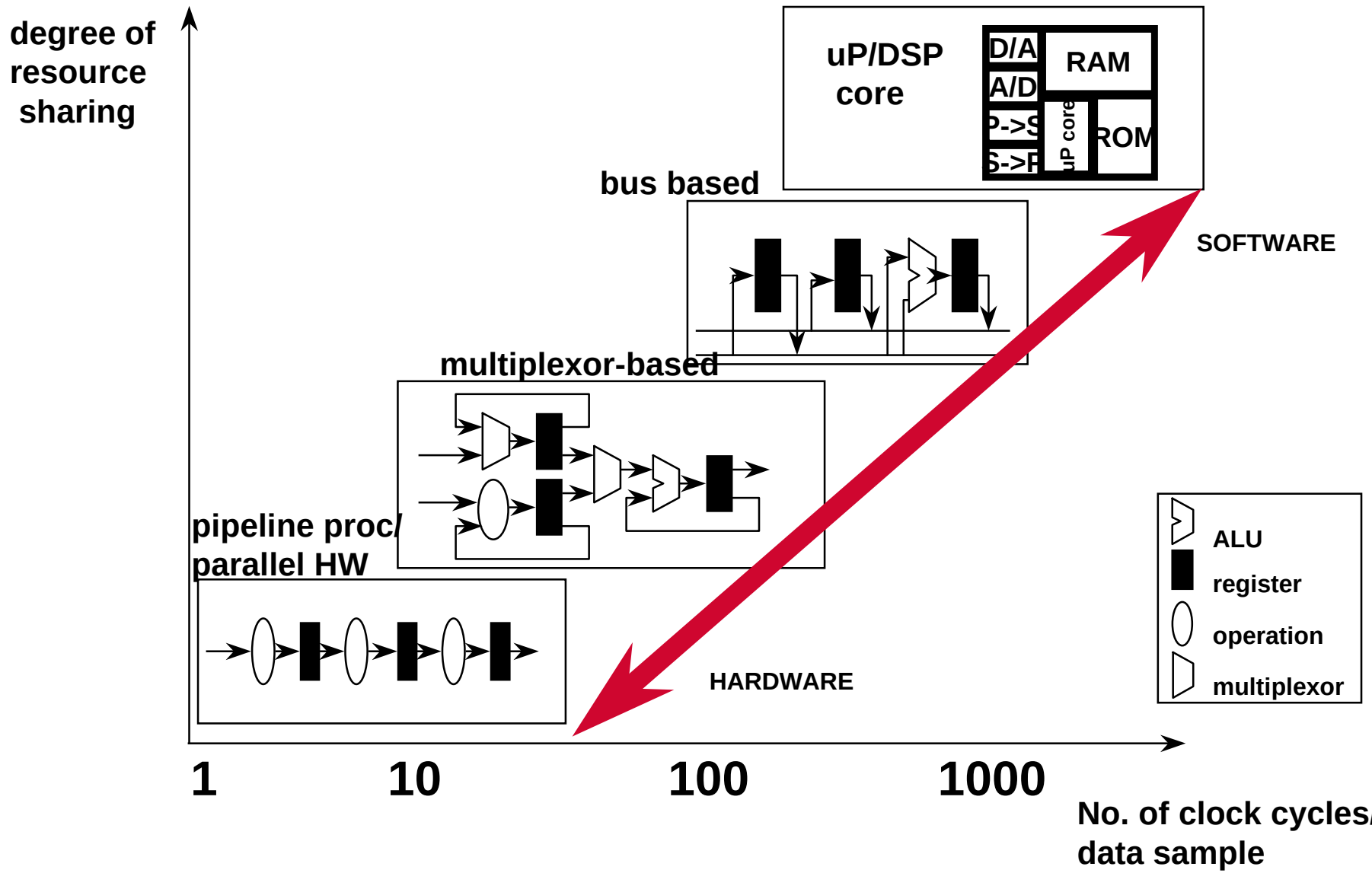
**Control**
Protocol Stack
User Interface...

Power efficient, high-speed signal processing and fixed algorithms

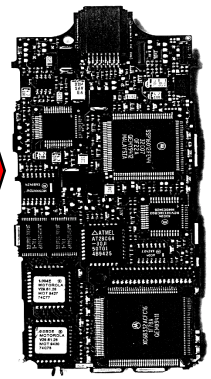
**Signal**
High-speed Modulation
Viterbi Decoding
Channel Estimation
Matched Filtering
Synchronization
Deinterleave
Equalization
Encryption

**FLEXIBLE** ⟷ **HARDWIRED**

# Exploring The Target Architecture Space



# A View of Terminal Architecture Today



memory

Algorithmic Coprocessors

Algorithmic Coprocessors

DMA

uP core

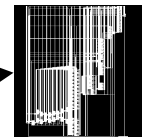
DSP core

ADC/ DAC

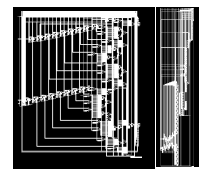
peripherals

RF/IF Subsystem

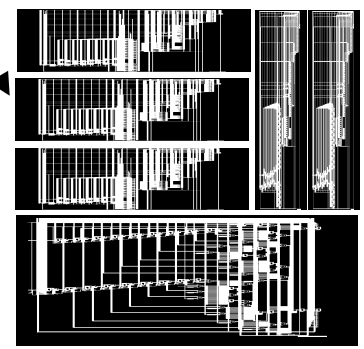
PDC



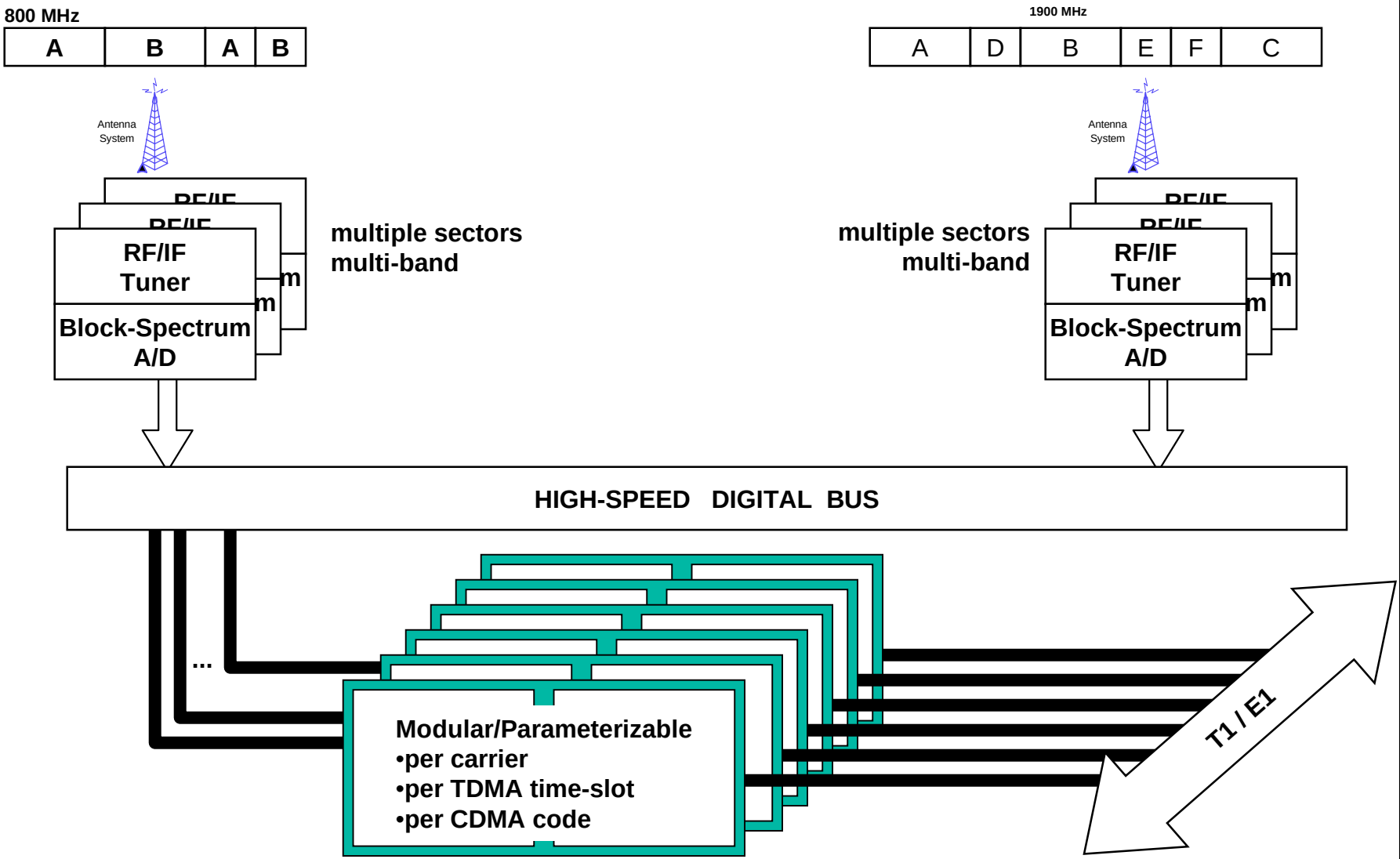
GSM



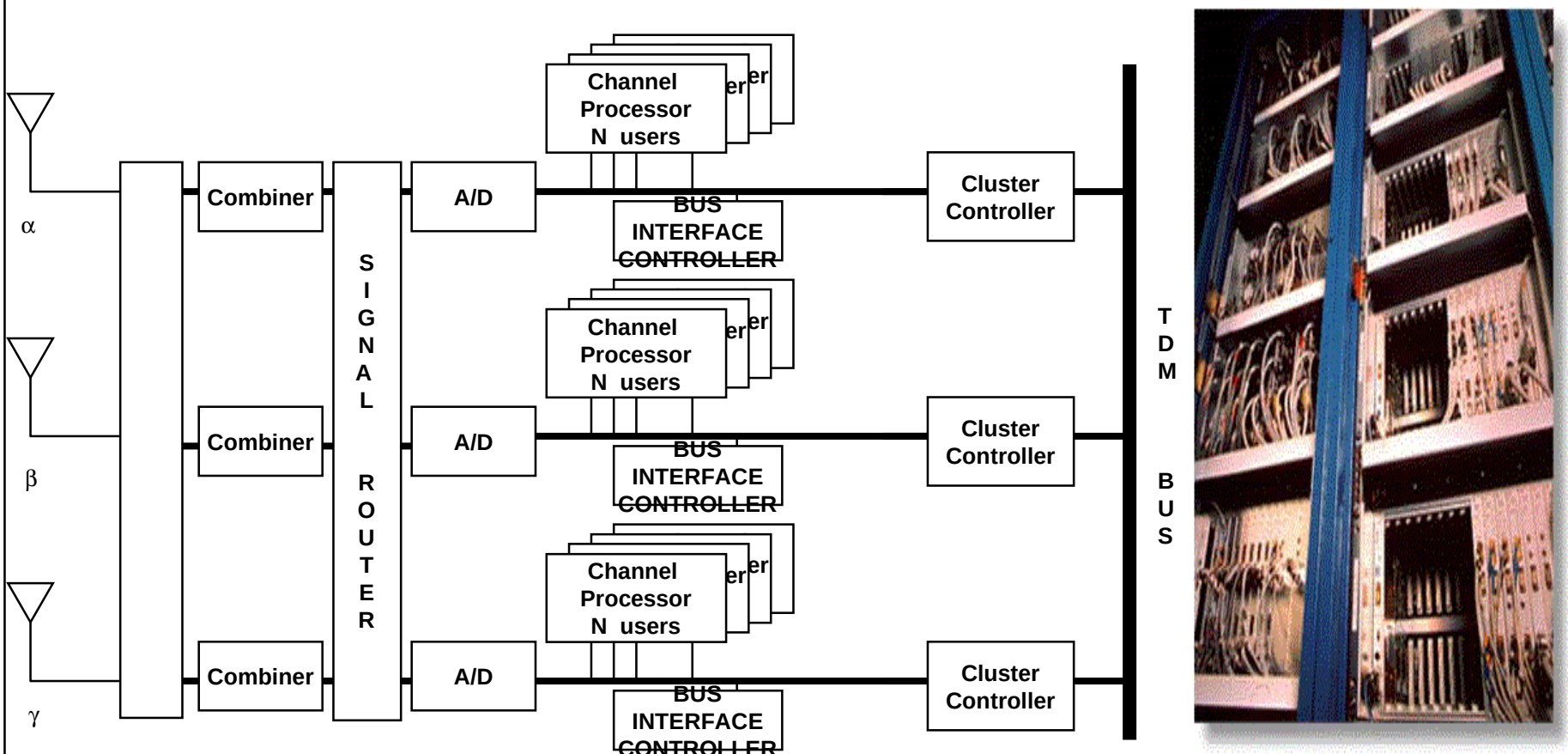
IS-95



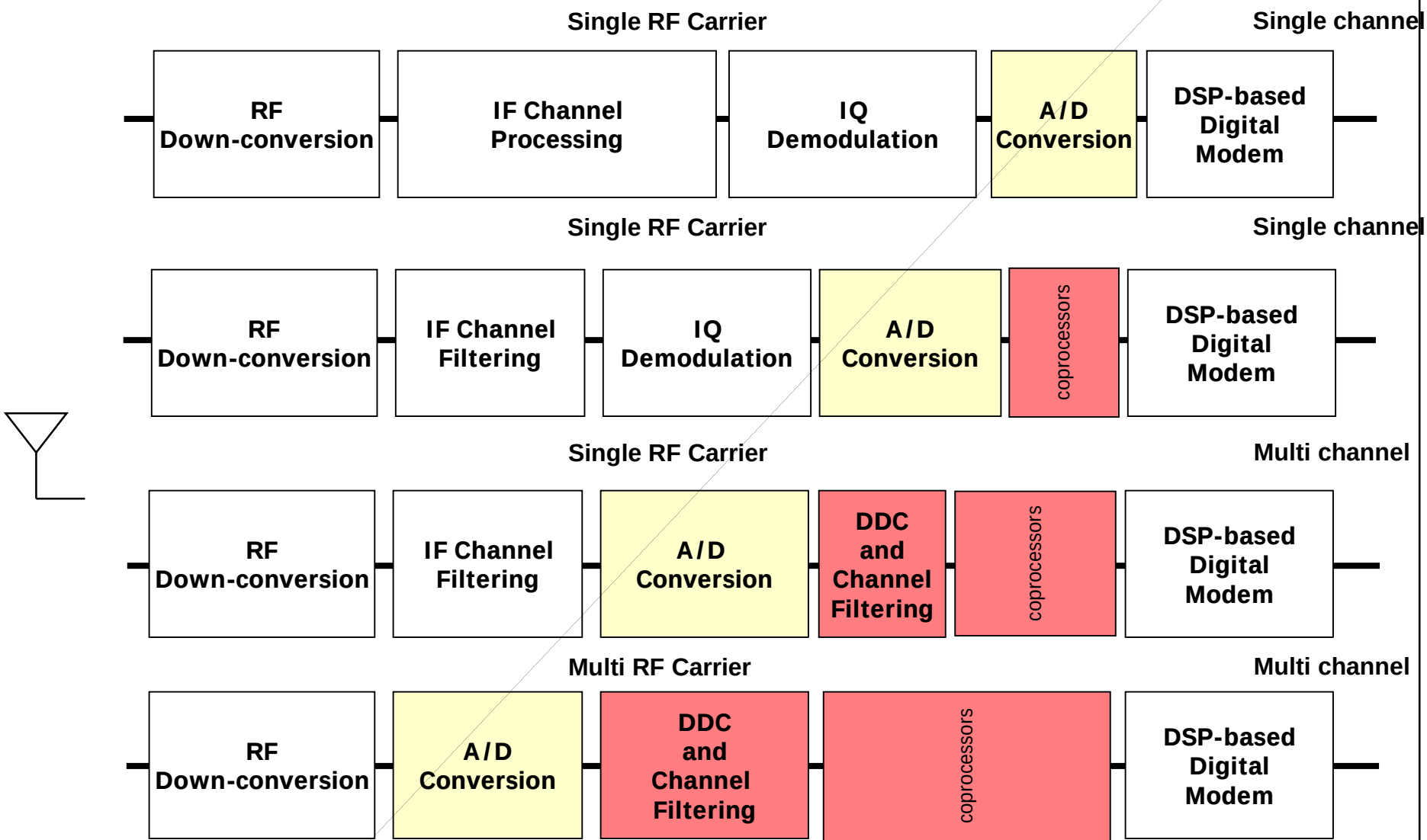
# A View of Base-Station Architecture



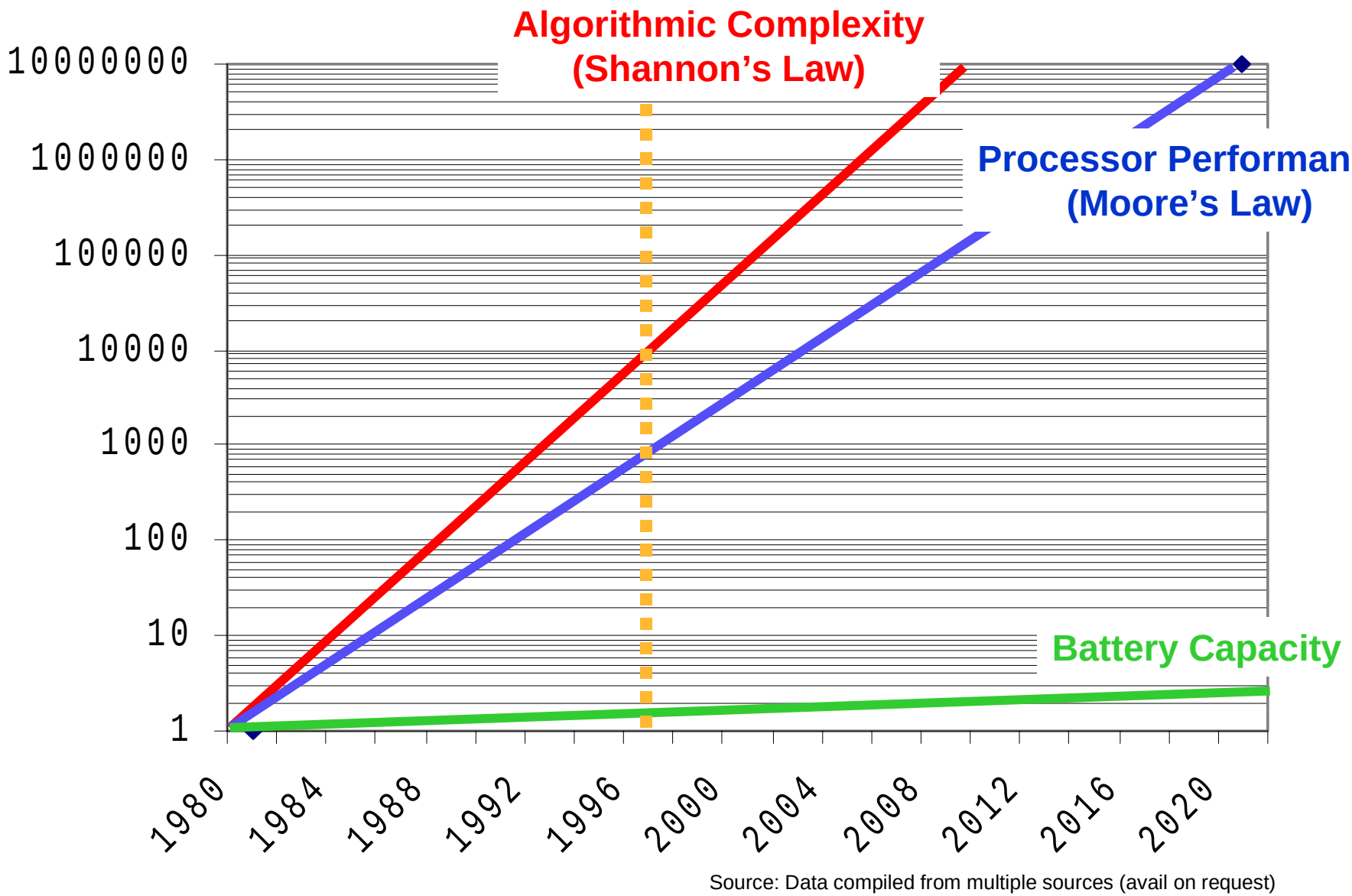
# Base-Station Architecture



# Evolution of Base-Station Architectures



# Going Wideband: Shannon vs. Moore




Source: Data compiled from multiple sources (avail on request)

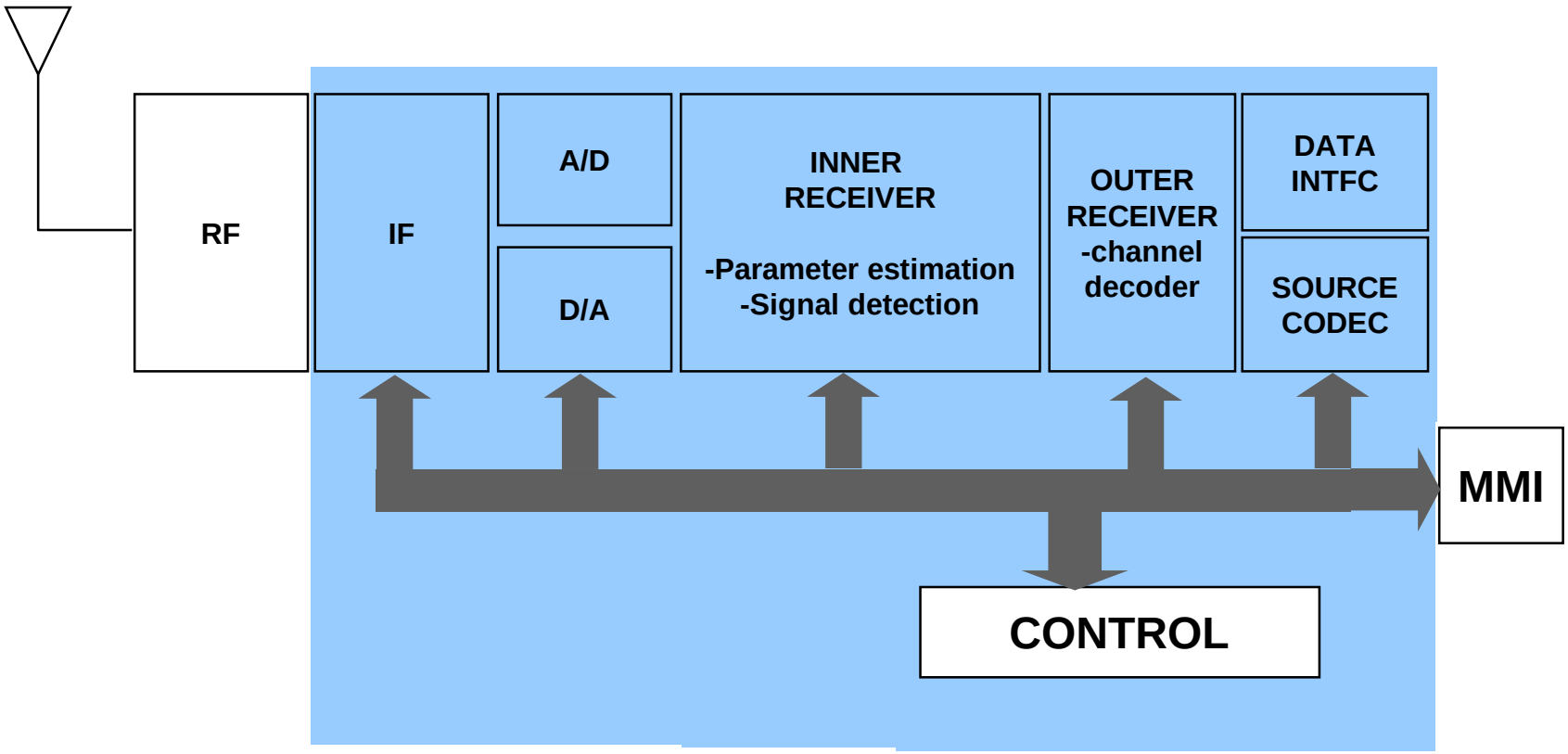
## Software Radio Is A Collection of Technologies That Enable Programmable System Architectures for Wireless Networks

- **RF- Linear wideband multicarrier RF Tx/Rx**
  - MCLPA, WBLNA, mixers
- **Conversion- Linear wideband high dynamic-range converters**
  - high SFDR, low IMD
- **High-speed digital bus communication infrastructure**
- **Modular, multi-protocol, multi-channel, multi-data-rate programmable digital modem processors**
  - per carrier, per time-slot,  per code slot
- **SW programmer's view of radio signal processing system**

# *Features of Software Radios*

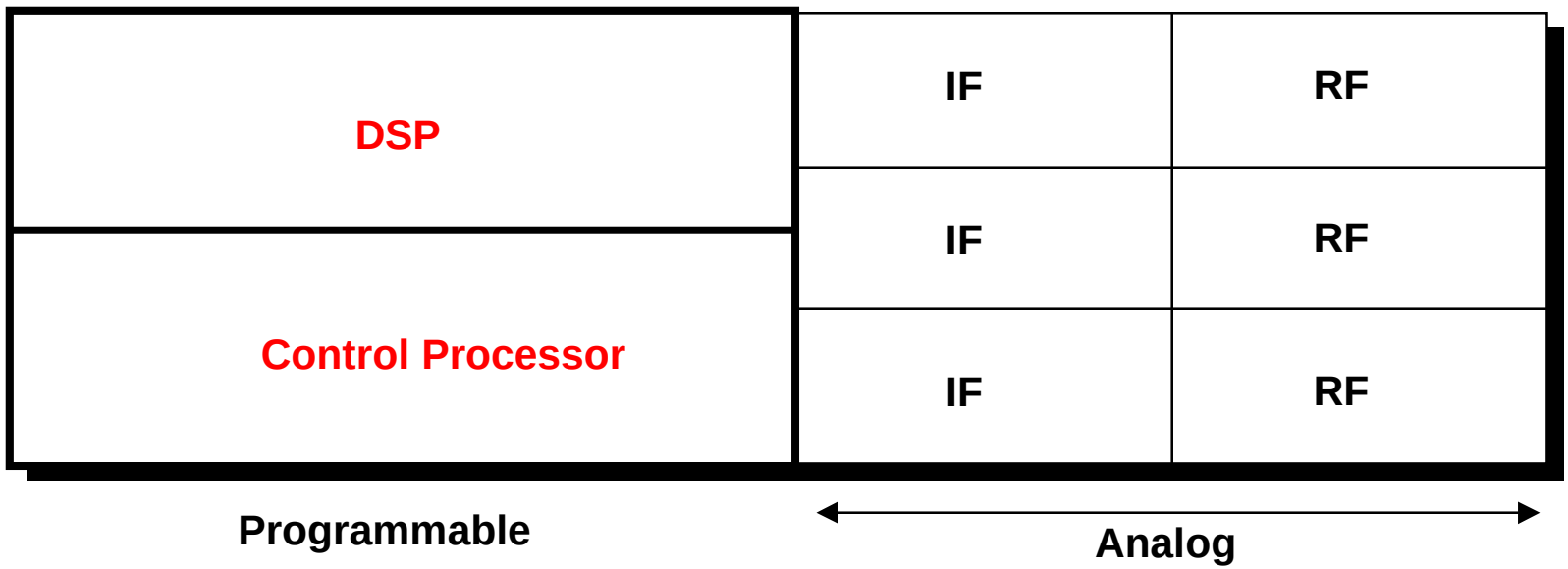
- **Offer enhanced capabilities using software-based processing**
  - Flexibility: agility across functions, services, standards
    - multimode
    - multiband
  - Adaptability: adaptive link control based on channel conditions
    - modulation
    - reception
    - interference-control
- **Realize these capabilities with a consistent SW programmer's model for a terminal**

# Evolution of Soft-Processing



# SW Multistandard Solution

**Applying instruction-set processor architectures to all baseband processing would be desireable...**




**Viable approach for some 2G systems. Not viable for 2.5 to 3G systems primarily due to:**

- **-power W/m3**
- **-cost**

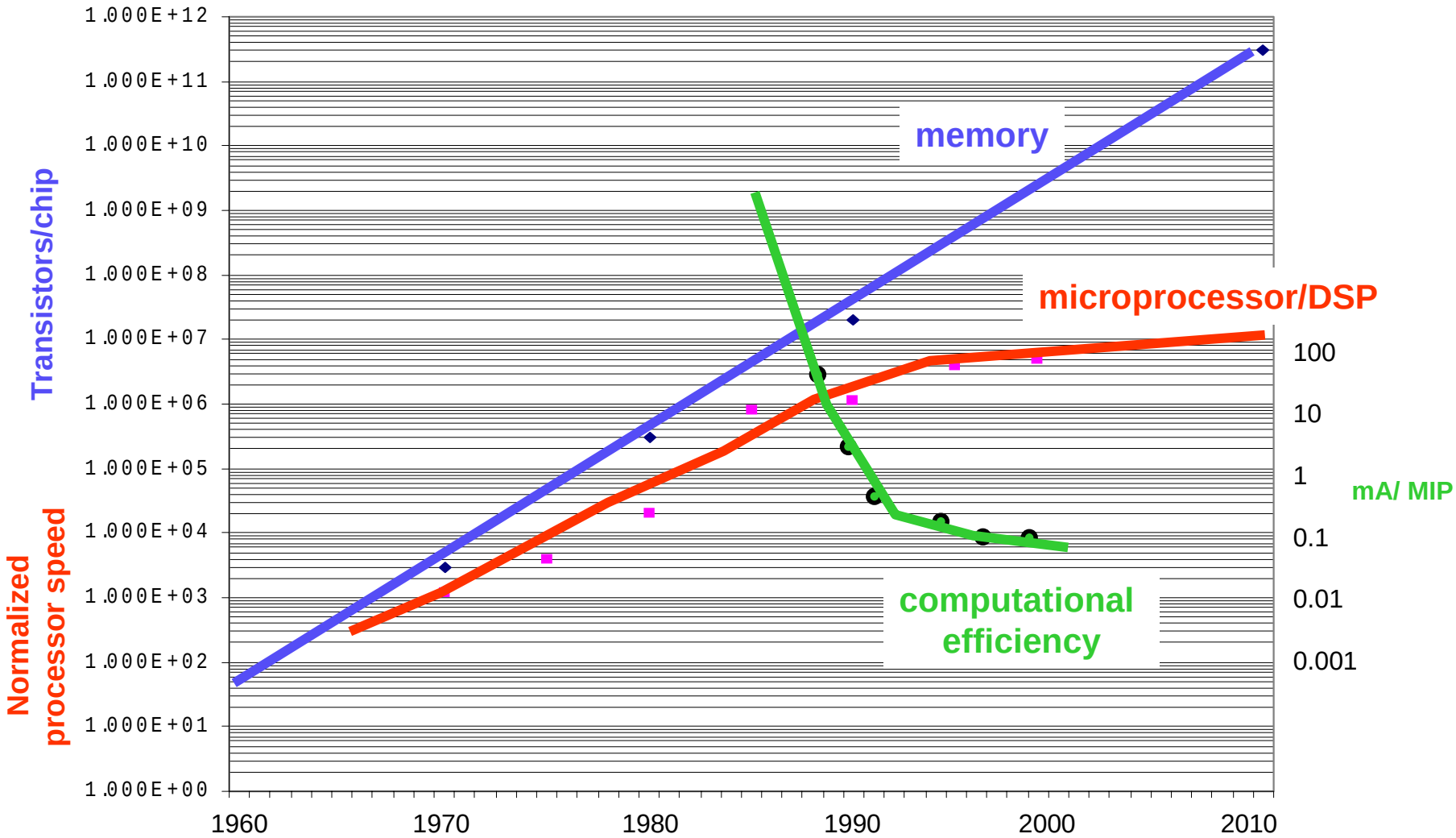
**Not a viable implementation for terminals**

# Digital Signal Processors

- **Competition has moved on from raw MIPS to architecture**
- **New criteria:**
  - the ‘power-dissipation cost” of “computational power”
  - Over the last 7 years, in DSP for wireless, the name of the game was mA/MOP
  - Today, everyone MUST focus on computational efficiency!
- **Architecture battles:**
  - RISC v CISC
  - DSP v NSP
  - Superscalar v VLIW
- **Design aiming at optimum speed, not ultimate speed [1]**

[1] C.M. Huizer, “Optimized Application of Submicron CMOS for VLSI Logic- A Systems Perspective,” Proc. CICC, 1987.

# Digital Signal Processor Performance

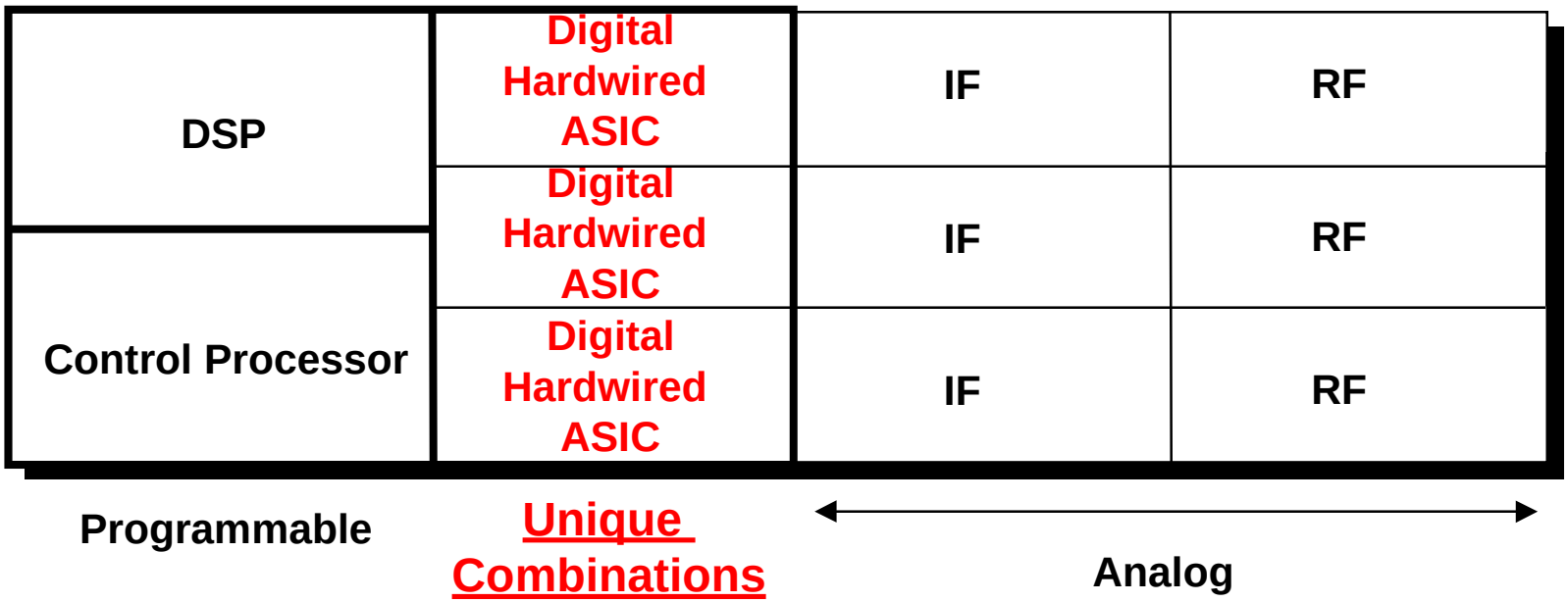



Sources: Proc ISSCC, ICSPAT, DAC, DSPWorld

# HW Multistandard Solutions

**The common approach to hardware design involves:**

**multiple ASIC's to support each standard.**

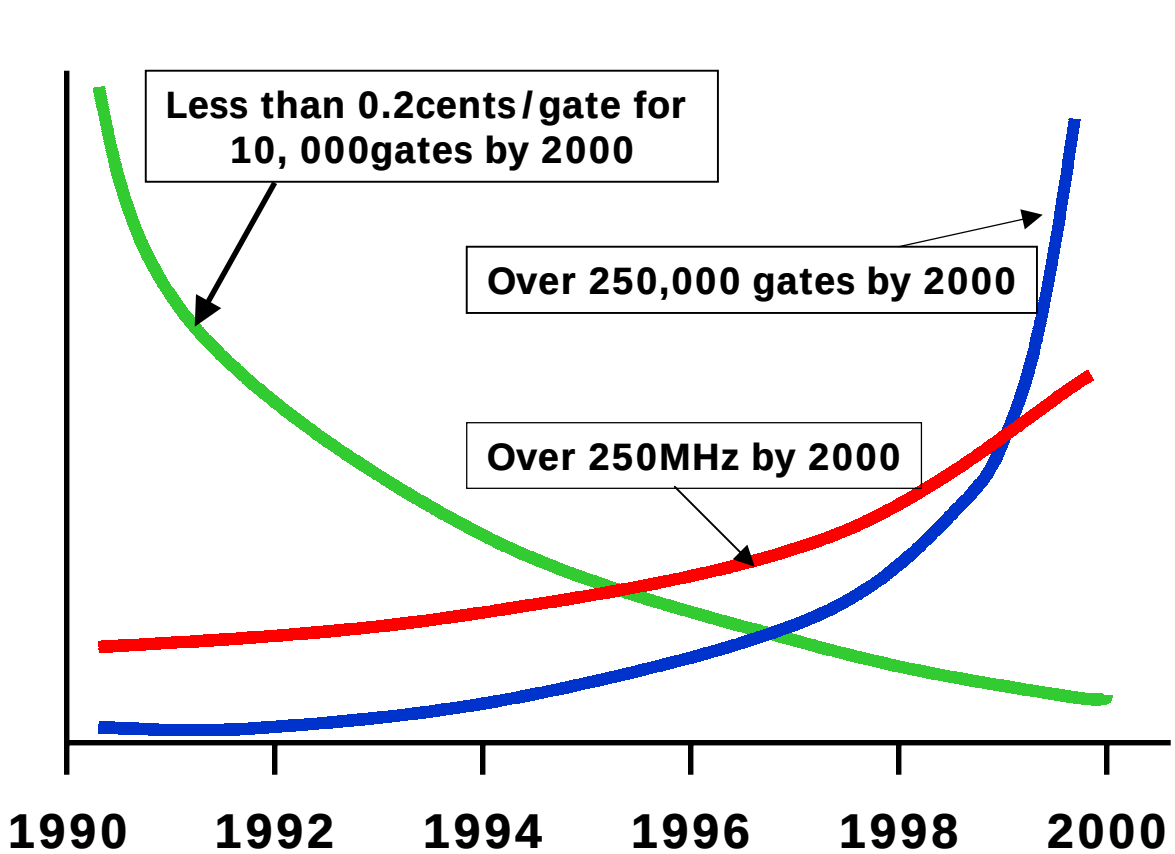



**Hardwired implementation is not flexible or upgradeable.**

**Creating new chipsets for every technology combination critically challenges available industry design resources!**

# *And Reconfigurable Systems Are Beginning To Make Economic Sense...Beyond Prototype*

- **Price, Performance, and Density Trends (eg. FPGA)**





**For designs requiring less than 100,000 gates, programable logic will become the dominant choice**

**Source: Dataquest, 1997**

# *Or Are They?*

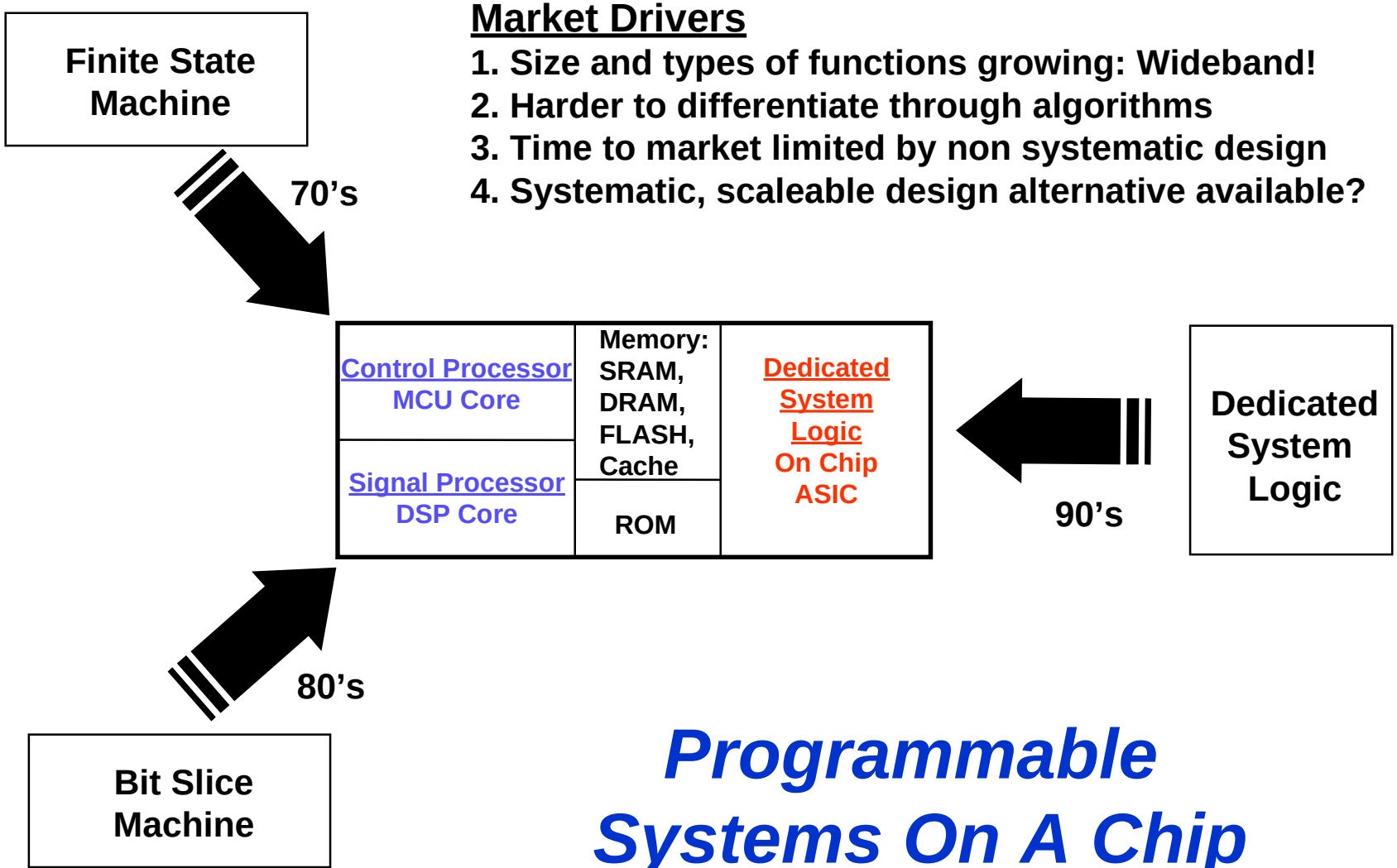
- **What has changed:**
  - Moore's Law driven improvements in density, performance, & cost
  - Design software evolving slowly away from ASIC
  - Systems integration
- **What has not!**
  - 120 transistors / gate: Ouch!!!!
  - Business model of selling tens to millions!

# Advances(?) In Reconfigurable Logic

- **Process**
  - Not free anymore.
- **Circuits**
  - Possible increased static power consumption. Possible lower capacity or higher cost than Moore's Law would give.
- **Architecture**
  - New architecture needed for speed
- **Software**
  - More problems relegated to CAD tools!

**FPGA starting to be used as a process driver!**

# Systematic & Scaleable Design Alternatives




## Market Drivers

1. Size and types of functions growing: Wideband!
2. Harder to differentiate through algorithms
3. Time to market limited by non systematic design
4. Systematic, scaleable design alternative available?

***Programmable Systems On A Chip***

***Thank You !***