Scaling Challenges and Market Opportunity for Phase Change Memory

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The unrelenting cost reduction through continued miniaturization of semiconductor memory has both enabled new generation of devices, and transformed multiple industries. Low cost NAND flash memory has replaced audio CD’s, camera film and video recording cassette tapes and is now targeting replacement of hard drives. However, as NAND memory continues to scale to smaller dimensions: electrical performance and cycle endurance is degrading significantly thus opening up an opportunity for a disruptive new non-volatile memory with improved electrical performance and cycle endurance to supplement low cost NAND as a low latency buffer memory. NAND has the potential option of going vertical to continue down the cost reduction road while bypassing lateral scaling limits, but electrical performance and reliability is anticipated to degrade further.

DRAM with no MLC capability has lagged significantly behind NAND in cost per bit and is also approaching fundamental roadblocks in continued scaling with no option of stacking multi cells in the vertical dimension. With increasing emphasis on power reduction – there is an opportunity for a new disruptive NV memory with sufficient random R/W performance and cycle endurance to displace a percentage of DRAM in power sensitive applications.

Out of all the disruptive memories proposed – Phase Change Memory (PCM) is leading the pack by almost two orders of magnitude in product density being shipped, but the amount of activity on alternative disruptive memory technologies such as STT MRAM, CBRAM and RRAM is increasing. The most critical requirement for any new disruptive memory is continued scalability to justify the technology investment. The focus of this presentation will be to review PCM status today, PCM market opportunities and future PCM scaling challenges and proposed/demonstrated technical solutions for continued PCM scaling. In particular the issue of increasing PCM cell current density with scaling and structural scaling paths for enhanced cycle endurance will be presented.
NAND’s position in the compute memory hierarchy is becoming well established. This new position in the hierarchy imposes new scaling considerations for NAND performance and reliability to smaller lithography nodes and tightly links NAND with the external controller. Planar scaling of NAND is additionally facing challenges of fundamental physics, increasing the pursuit towards 3D scaling. If successful in pursuit of 3D, NAND cost per bit scaling continues, maintaining NAND’s position in the compute memory hierarchy. However the risks in NAND scaling, the never ending demand for performance and advancements in new memory research creates a potential opportunity for future non-volatile memory technologies in computing applications. The ability of new memories to meet or beat the incumbent NAND, and also DRAM, memories with respect to cost and performance criteria will determine whether the new memories will become niche or ubiquitous in compute applications.

Among all the configurations, stackable thin-film cross point memory delivers the densest array, therefore the most compact die size and lowest cost per bit. Combining its attributes in cost, performance and reliability, cross point technologies stimulate potential opportunities in computing memory hierarchy. This talk will survey current advances in cross point memory and the integrated selector in various material systems. Lastly the attributes of the memories will be reviewed to assess gaps to solve to become ubiquitous in compute applications.
Ionic Memory

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The adoption of novel materials and device structures will be necessary to overcome the growing limitations of existing memory technologies such as DRAM and Flash in low energy computation and ultra-mobile applications. One alternative that appears to have risen to the point of implementation is resistive memory or “ReRAM”, in which information is represented by different values of electrical resistance. In one particularly promising low energy approach to this type of memory, resistance is controlled by the movement of ions coupled with electrochemical (reduction and oxidation) processes. These “ionic” resistance-change devices are generally divided into cation cells, based on the growth and dissolution of conductive metallic filaments in a relatively insulating solid electrolyte via the migration of metal ions, and anion cells, which typically utilize the formation and removal of conducting metallic or sub-oxide regions in metal oxides by the movement of oxygen ions or vacancies [1,2].

In the case of mobile metallic cations, an ion current will flow if (1) the electrolyte is placed between two electrodes, at least one of which is oxidizable, (2) the oxidizable electrode is made positive with respect to the opposing electrode, and (3) a sufficient bias is applied to overcome the internal potential barrier. The ion current feeds a reduction reaction, resulting in the formation of a metallic filament within the electrolyte. The filament has a conductivity that is much higher than the surrounding solid electrolyte and hence the resistance of the structure can decrease by several orders of magnitude. The volume of the conducting filament depends on the total number of metal ions that are reduced, which in turn depends on the charge supplied by the external circuit. Thus, the device resistance can be controlled by programming current and time, which means that it is possible to create multiple discrete resistances levels to represent more than one binary digit per cell [3,4]. In addition, it is possible to layer ionic memory cells above the substrate in passive diode-isolated arrays to further increase information storage density [5].

Ionic memory is now under investigation in some of the world’s top research institutes and companies and has gained sufficient momentum and acceptance to be included in the International Technology Roadmap for Semiconductors. This presentation will discuss the materials and operational characteristics of ionic memory and cation cells in particular, and will demonstrate, by way of examples from academia and industry, why this technology will be commercialized in the not-too-distant future.

Emerging Memory Opportunities and Challenges

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Although physical scaling is becoming increasingly difficult for conventional mainstream memory technologies such as NAND and DRAM, the forces driving cost, power and density scaling are growing relentlessly. The amount of memory in systems for example is increasing geometrically while the power budget continues to decrease. In addition, the applications and resultant memory requirements continue to diversify from handheld devices to larger data centers. Several technologies have been proposed over the years with no clear winner. Some of the critical factors which need to be considered for a successful implementation of a new technology include; why and when alternate memory technologies may be needed, what are the performance criteria and related requirements, and what needs to happen in the ecosystem to support a successful new technology. The result of this reality is that bottoms up development for a new memory technology may not feasible due to technical risks and cost and we must target application-specific solutions for new future markets.
Metal Oxide Based Nonvolatile Memories - Promises and Challenges

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The desirable nonvolatile memory devices must be both extremely scalable and capable beyond the 16nm technology generation. Metal oxide based RRAM (memristors) appear to fulfill these requirements and have recently been recommended for additional focus in research and development by the International Technology Roadmap for Semiconductor (ITRS). These devices are two-terminal devices that retain state, which provides many useful properties to complement transistors while enabling increased functionality in integrated circuits. I will first briefly describe the working mechanism of metal-oxide switches and a related family of nanodevices, along with their potential applications. Then I will focus on the promises and challenges with respect to using these devices as nonvolatile memories, together with some recent significant progress.