INTRODUCTION TO CMOS DEVICE RELIABILITY

CMOS DEVICE RELIABILITY

- RELIABILITY AT TRANSISTOR LEVEL
  - HOT CARRIERS DEGRADATION -- (HCl)
  - GATE OXIDE DEGRADATION --- (TDDB)
  - EMERGING ISSUES -- (such as NBTI)

- EARLY EVALUATION AT WAFER LEVEL

Diagram:
- DESIGN
- FAB
- PCM TEST
- SORT
- PKG/FT
- PROD REL
- WLR

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INTRODUCTION TO CMOS DEVICE RELIABILITY

- AS CMOS TECHNOLOGY SCALES DOWN DEVICE RELIABILITY ISSUES BECOME SEVERE

1) CHIP DENSITY AND PERFORMANCE INCRESSES

- SCALING FROM 0.5\(\mu\) TO 0.09\(\mu\) NODES,
  - \(\mu\) P TRANSISTORS; 5M \(\rightarrow\) 100M
  - INT. CLOCK: 200MHz \(\rightarrow\) 2 - 3 GHz

2) TRANSISTOR AND INTERCONNECT DIMENSIONS ARE SCALED DOWN
INTRODUCTION TO CMOS DEVICE RELIABILITY

CMOS TRANSISTOR SCALING TREND

<table>
<thead>
<tr>
<th>YEAR</th>
<th>L ( \mu )</th>
<th>Tox A</th>
<th>V</th>
<th>E V/cm</th>
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<tbody>
<tr>
<td>1989</td>
<td>1.0</td>
<td>180</td>
<td>5</td>
<td>3</td>
</tr>
<tr>
<td>1992</td>
<td>0.5</td>
<td>120</td>
<td>5</td>
<td>4</td>
</tr>
<tr>
<td>1995</td>
<td>0.35</td>
<td>80</td>
<td>3.3</td>
<td>4</td>
</tr>
<tr>
<td>1998</td>
<td>0.25</td>
<td>50</td>
<td>2.5</td>
<td>5</td>
</tr>
<tr>
<td>2004</td>
<td>0.13</td>
<td>25</td>
<td>1.2</td>
<td>5</td>
</tr>
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</table>

- AS CHANNEL LENGTH \( (L) \) AND GOX THICKNESS \( (Tox) \) ARE SCALED DOWN, E –FIELDS IN OXIDE AND CHANNEL INCREASE

- DEVICE RELIABILITY ISSUES \( (HCI AND TDDB) \) BECOME SEVERE
INTRODUCTION TO CMOS DEVICE RELIABILITY

- CMOS DEVICE RELIABILITY ISSUES VS. PROCESS NODES

- 1.5u
- 1u
- 0.35u
- 0.25u
- 0.18u
- 0.13
- 0.09u

WLR

HCI, TDDB, EM

WLR

HCI, TDDB, EM, NBTI, B to B TUNNELING, SOFT BREAKDOWN, Cu/ Low K, etc
CMOS DEVICE RELIABILITY

AGENDA

- BASIC HOT CARRIER RELIABILITY -- HCI
- EMERGING HCI ISSUES BELOW 0.18 μ
- NBTI

- BASIC GATE OXIDE RELIABILITY -- TDDB
- EMERGING TDDB ISSUES IN ULTRA-THIN GOX

- OVERLAPPING EFFECTS

- CONCLUSIONS
CMOS DEVICE RELIABILITY -- HCI

*Hot Electron effect*

- Channel electrons are injected
- Impact ionization creates electron hole pairs.
- Holes drift to substrate (Isub)
- Hot electrons create damage to the oxide (Nit and Not)
- Isub is a measure of H-C generation rate
Illustration of $gm$ and $vt$ degradation (NMOS)

- Electron trapping in GOX
- $Vt$ goes up
- Peak $Gm$ goes down
- **H-C lifetime**: time for 10% degradation

I_{sub} = C \cdot I_d \exp \left[ - \frac{E_i}{\lambda E_y} \right],
\text{where} \ E_i = \text{ionization energy}
\lambda = \text{mean free path}

I_{sub} = C \cdot I_d \exp \left[ - \frac{(E_i \cdot L)}{\lambda (V_d - V_{dsat})} \right]
Hot electron lifetime measurements and extrapolation

- **MODEL:** $I_{\text{sub}}$ used as a stress parameter

- $\tau = B \cdot (I_{\text{sub}}/Z)^{-m}$

Ref: T.Y. Chan, et. al. IEDM Tech Dig. 1988, p 196
CMOS DEVICE RELIABILITY - DEVICE STRUCTURES TO REDUCE HCI

- DRAIN ENGINEERING
  - PROFILE AND SPACER ADJUSTMENTS TO IMPROVE LIFETIME

- LDD PROFILES TO REDUCE HCI
  - LDD (LIGHTLY DOPED DRAIN)
  - MDD (MEDIUM DOPED DRAIN)
  - LATID (Large Angle Tilted Implant Drain)

- TO REDUCE SHORT CHANNEL EFFECT
  - HALO IMPLANT
  - APT CHANNEL IMPLANT

\[ \varepsilon_{\text{ymax}} (\text{LDD}) = \left( V_{DS} - V_{DSSat} - \varepsilon_{\text{ymax}} L_n \right) / 0.22 \cdot t_{ox}^{1/3} \cdot r_{j}^{1/3} \]
CMOS DEVICE RELIABILITY --- PMOS HCI

**PMOS HCI**

- HCI EFFECT VERY SMALL COMPARED TO NMOS
- NET NEGATIVE CHARGE CREATED IN OXIDE (like in NMOS)
- $V_t \downarrow$ CREATING SHOT CHANNEL EFFECT AND DIBL

CMOS DEVICE RELIABILITY AC LIFETIMES (HCI)

- **AC HCI** (10 YEAR DC LIFETIME HARD TO ACHIEVE IN DEEP SUB MICRON REGION)

  - \( \Delta V_t / V_t = C(L) \cdot I_{sub}^m \cdot D \cdot t \)  
  \[ \text{AC Lifetime} = (B/D) \cdot I_{sub}^{-m} \]

CMOS DEVICE RELIABILITY

EMERGING HCI TRENDS AT NODES 0.18μ OR BELOW

- **NMOS CONTINIES TO BE OPTIMIZED** (for HCI lifetime, short channel effects and performance – spacer, halo, apt, LDD profiles)

- **PMOS**: changes behavior
  - VT shift \( \uparrow \) instead of \( \downarrow \)
  - Hole injection / trapping instead of electrons
  - Temp. dependence reverses
  - Max degradation condition changes from \( V_G < V_D \) to \( V_G = V_D \)

- NBTI effect??
NBTI-
EMERGING WEAR-OUT MECHANISMS
(node 0.18u and less)

STRESS BIAS
DEGRADATION BEHAVIOR
PHYSICAL MECHANISMS
MODEL
AC NBTI
FREQ DEPENDENCE
CMOS DEVICE RELIABILITY -- NBTI

- COMPARISON OF PMOS NBTI LIFETIMES VS. NMOS AND PMOS HCI (0.13 MICRON TECHNOLOGY).

CMOS DEVICE RELIABILITY -- NBTI

NBTI BIAS ---- COMPARISON OF NBTI AND HCI BIAS
(PMOS AND NMOS)

NMOS HCI | PMOS HCI | PMOS NBTI

+Vg = Vd/2 | - Vg = low | - Vg

Vd

P-SUB | N-SUB | N-SUB
CMOS DEVICE RELIABILITY -- NBTI

- **NBTI PHYSICAL MECHANISM**

- Positive charges are created at interface (Nit) BULK (Not)
- \( V_t \) shifts up, \( G_m \) down

![Diagram showing the physical mechanism of NBTI](image)

- Bulk charge Not
- Poly
- Interface traps Nit (dissociated Si–H bonds)
- \(-V_g\)
CMOS DEVICE RELIABILITY -- NBTI

NBTI PHYSICAL MECHANISM

- POSITIVE CHARGE IS CREATED IN OXIDE AND INTERFACE BY HOLE TRAP GENERATION FROM HOLES IN INVERSION LAYER

Ref: k. Ogata et al IEEE IRPS 2005 pp 372-376
CMOS DEVICE RELIABILITY -- NBTI

REACTION –DIFFUSION MODEL (R-D MODEL)

Oxide

\[
\begin{array}{|c|c|}
\hline
\text{Si} & \text{H} \\
\text{Si} & \text{H} \rightarrow \text{H}_2 \\
\text{Si} & \text{H} \\
\text{Si} & \text{H} \\
\hline
\end{array}
\]

Ref: Yuichiro Mitani et al, p512 IEDM 2002
CMOS DEVICE RELIABILITY -- NBTI

MECHANISM OF N_{IT} GENERATION (R-D MODEL)

- Initially the process of hydrogen release/creating of Nit is reaction limited and is fast.

- Later as the presence of hydrogen grows it tends to recombine and passivate the dangling bonds. This slows down the reaction.

- Time evolution of N_{IT} is modeled by:
  \[
  \frac{dN_{IT}}{dt} = k_{fo} P [N_o - N_{IT}] - k_r N_H . N_{IT}
  \]
  \[
  \frac{dN_H}{dt} = D \frac{d^2N_H}{dx^2}
  \]

Where
- N_o = initial density of Si – H bonds
- P = Precursor for dissociation
- N_H = density of released H species
- K_{fo} = bond dissociation rate
- K_r = self anneal (passivation) rat

Ref: 1) M.A. Alam IEEE IEDM Proceedings 2003 pp 345-346
2) M. Ershov IEEE IRPS Proceedings 2003 pp 606-607
CMOS DEVICE RELIABILITY -- NBTI

- BOTH Nit AND Not (BULK POSITIVE CHARGE) ARE GENERATED

- USING CHARGE PUMPING, Vt AND SILK MEASUREMENTS Not AND Nit ARE SEPARATED

REF:  V. Huard et al IRPS 2003 pp 178-182
     S. Chakravarthi IEEE IRPS, 2004, pp173
     D.S. Ang and S. Wang, IEEE IRPS 2005 pp 706-707
CMOS DEVICE RELIABILITY -- NBTI

NBTI DEGRADATION MODEL IN DIFFERENT RANGES OF Eox AND Vg

(A) **E MODEL:** \[ \Delta V_t = C \cdot \text{Exp} (\beta V_g) \cdot t^n \] (Vg = 1.2 to 2.0; Eox < 10MV/cm)
- R-D MECH, HVB>EVB, DIFFUSION OF H2 MOLECULAR SPECIES

(B) **POWER LAW:** \[ \Delta V_t = C \cdot V_g^r \cdot t^n \] (Vg = 2.0 – 2.7; Eox > 10MV/cm)
- ENHANCED DEGRADATION RATE (1) R-D MECH, H+ ATOMIC SPECIES or (2) HH INJECTION EVB>HVB

Ref: (1) Chia Lin Chen et al, IRPS 2005 pp 704-705
(2) P. Bharat Kumar et al, IRPS 2005 pp 701
CMOS DEVICE RELIABILITY – DYNAMIC NBTI RECOVERY

- LIFETIME CAN IMPROVE BY A FACTOR OF 10 – 30
- RECOVERY IS ALWAYS SAME FRACTION OF IN EVERY CYCLE.
- BOTH Nit AND Not PARTICIPATE IN THE DEGRADATION AND RECOVERY

Ref:
- M.A. Alam IEEE IEDM Proceedings 2003 pp 345-346
- M. Ershov IEEE IRPS Proceedings 2003 pp 606-607
- S. Chakravarthi IEEE IRPS, 2004, pp173
IMPROVEMENT OF NBTI LIFETIME FOR AC (PULSED) STRESS

- LIFETIME IMPROVEMENT IS DUE TO

(1) DUTY FACTOR

(2) PARTIAL RECOVERY IN EACH CYCLE.
CMOS DEVICE RELIABILITY – DYNAMIC NBTI

- NBTI AND HCI STRESS CYCLES
FREQUENCY DEPENDENCE OF NBTI LIFETIME

- Generally a weak frequency dependence
- If $t_1$ and $t_2$ time constants during stress and off periods
- If $t_1 > t_2$ --- reduction in effective damage rate with increasing frequency
CMOS DEVICE RELIABILITY -- TDDB

**TDDB: TIME DEPENDENT DIELECTRIC BREAKDOWN**

- **TBD (Lifetime)** = TIME TO BREAKDOWN (CONST. VOLTAGE STRESS)
- **QBD** = CHARGE TO BREAKDOWN

![Diagram of FN current and oxide thickness vs. gate voltage](image)

\[ J = A_F E_{ox}^2 \exp \left( -B/E_{ox} \right) \]
CMOS DEVICE RELIABILITY -- E-field ACCELERATION

- ILLUSTRATION OF TDDB LIFETIME (Tbd) DISTRIBUTIONS for different E-field stress

- Weibull Distribution Cdf = F(t) = 1- exp [- (t/c)^m], for t >0
  - ln { ln [1- F(t)]^-1} = m ln(t) – m ln(c)
CMOS DEVICE RELIABILITY  TYPICAL WEIBULL PLOTS

ILLUSTRATION OF WEIBULL PLOTS FOR DIFFERENT STRESS

\[ \ln \left( \ln \left( 1 - F(t) \right) \right) = \beta \ln t - \ln \alpha \]

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<tr>
<th>Ft</th>
<th>Weibull scale</th>
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<tr>
<td></td>
<td>( \ln[-\ln(1-F_t)] )</td>
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<tr>
<td>0.001</td>
<td>-6.9</td>
</tr>
<tr>
<td>0.01</td>
<td>-4.6</td>
</tr>
<tr>
<td>0.1</td>
<td>-2.25</td>
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<tr>
<td>0.5</td>
<td>-0.36</td>
</tr>
<tr>
<td>0.9</td>
<td>+0.83</td>
</tr>
<tr>
<td>0.99</td>
<td>+1.52</td>
</tr>
</tbody>
</table>

In[-ln(1-Ft)] vs. log t (hrs)
CMOS DEVICE RELIABILITY  E MODEL PARAMETER EXTRATION

- $E_{\text{model}}$ (ref 1,2)
- $T_{bd} = B \cdot \exp(-\beta E_{\text{ox}})$
- $\frac{1}{E_{\text{model}}}$ (ref 4)
- $T_{bd} = A \cdot \exp \left( G \frac{X_{ox}}{V_{ox}} \right)$

1) D.L. Crook, IEEE IRPS 1979, pp1-7
2) J.W. McPherson and D.A. Baglee IRPS 1985, pp1-5
CMOS DEVICE RELIABILITY -- TEST STRUCTURES FOR OXIDE EVALUATION

**AREA CAPACITOR**

**FIELD EDGE**

**POLY EDGE**

- **GATE OXIDE**
- **POLY**
- **METAL**
- **METAL PAD**
CMOS DEVICE RELIABILITY -- ULTRA-THIN OXIDES

TDDB

TDDB ISSUES FOR DEEP SUBMICRON
(ULTRATHIN OXIDE)

BAND TO BAND TUNNELING – GATE LEAKAGE
POWER LAW FOR Vg DEPENDENCE
PMOS(INV) TDDB BEHAVIOR DIFFERENT
SOFT BREAKDOWN
CMOS DEVICE RELIABILITY -- ULTRA-THIN OXIDES TDDB

ULTRA-THIN OXIDE TDDB

- **TUNNEL CURRENT DUE TO BAND TO BAND TUNNELING**
  
  \[ J = C(V_g, V_{ox}, \Phi_b) \cdot \exp \left\{ -D \cdot \Phi_b^{3/2} / \varepsilon_{ox} \left[ 1 - (1 - qV_{ox} / \Phi_b)^{3/2} \right] \right\} \]

- **GATE CURRENT INCREASES DRAMATICALLY**


Ref Ban Wong, A. Mittal, Yu Cao, G. Starr, ‘Nano-CMOS Circuit and Physical Design’ John Wiley and Son, 2005
CMOS DEVICE RELIABILITY -- ULTRA-THIN OXIDES TDDB

**Tbd POWER LAW IN ULTRATHIN OXIDES**

- WIDE RANGE OF TDDB DATA FOR DIFFERENT $T_{ox}$, AREAS AND VOLTAGE RANGES SHOWS **POWER LAW FITS BETTER THAN E-MODEL**
CMOS DEVICE RELIABILITY -- ULTRA-THIN OXIDES TDDB

**POWER LAW BEHAVIOR OF TDDB**

- EXPONENT NMOS (INV AND ACC) AND PMOS (ACC) = 45
- EXPONENT FOR PMOS (INV) $V_g < 3.8 = 33$
- FOR PMOS INV NBTI TYPE MECHANISM OF DEGRADATION IS POSSIBLE DUE TO HVB TUNNELING
  
  - Ref. K. Ohgata et al IEEE, IRPS 2005 p375
CMOS DEVICE RELIABILITY -- ULTRA-THIN OXIDES TDDB

PHYSICAL MECHANISM OF PMOS (INV) TDDB

- FOR PMOS (INV) TDDB, POSSIBLE PHYSICAL MECHANISM
  - 1) NBTI TYPE HOLE TUNNELING (R-D MODEL OR HH INJECTION)
  - 2) CATHODE ENERGY RELEASE MECHANISM

Ref: k. Ogata et al IEEE IRPS 2005 pp 372-376
SOFT BREAKDOWN IN ULTRA THIN OXIDES

- MECHANISM FOR SOFT BREAKDOWN: A NARROW LOCALIZED CURRENT PATH FORMED BY DEFECT PERCOLATION

- MICROSCOPIC NONUNIFORMITIES

- FIELD ACC’N FACTOR: SBD – 3.0 +/- 0.3; HBD-- 4.0 +/- 0.2 cm/MV
- TEMP ACTIVATION ENERGY: SBD-- 0.15- 0.25 eV; HBD-- 0.35 – 0.5 Ev
- Ref: Yuichiro Mitani et al IEDM 2002, p512
CMOS DEVICE RELIABILITY -- ULTRA-THIN OXIDES TDDB

- UNDERSTANDING OF PROGRESSIVE BD IN PFETS (INV)
  - Ernest Wu and Jordi Sune’ IRPS 2006 pp 54-62
HfSiON

- **IMPACT ON NBTI AND HCI**
  - Charge trapping in bulk detrimental. Minimal effect of interfacial traps. (No degradation of peak Gm or subthreshold slope.)
  - Low activation energy (0.043 ev) (compared to 0.15 ev for the H bonds) implies low potential bulk traps.

- **PBTI OR HCI IN NMOS**: Vt shift enhanced due to shallow electron traps in bulk. (Ref 3)

- **IMPACT ON TDDB**: Suitable model for TDDB lifetime not developed yet.
  - E model rather than 1/E model explains results (Ref 2)

- **DEUTERIUM** ambient improves reliability (Ref 4)
  - Effect is to reduce Nt but not Nt. There is isotope effect on chargepumping but not on Silk

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Ref 1: H. Rusty Harris et. al. IRPS 2005 pp 80-83
Ref 2: T. yamaguchi et al IRPS 2005 pp 67 – 74
Ref 3: M. Inoue et al. IRPS 2005 pp 644-645
Ref 4: H. Park et al IRPS 2005 PP 646-647
CMOS DEVICE RELIABILITY—OVERLAPPING EFFECTS

- **HCI-NBTI**: FOR PMOS HCI, HOLE TRAPPING EFFECT \((V_g = V_d)\) CAN BE DUE TO NBTI LIKE R.D MECHANISM

  ![Diagram showing HCI-NBTI effect]

- **TDDB-NBTI**: FOR TDDB IN PMOS (INV), LOWER POWER LAW EXPONENT \((33)\) CAN BE DUE TO NBTI LIKE HOLE TRAPPING MECHANISM MIXING WITH Vox DRIVEN MECHANISM  Ref K. Ohgata et al IEEE, IRPS 2005 p375

<table>
<thead>
<tr>
<th></th>
<th>ACC</th>
<th>INV</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS</td>
<td>~ Vg (^{-44}) ECB (Gate to substrate)</td>
<td>~ Vg (^{-44}) ECB (substrate to poly)</td>
</tr>
<tr>
<td>PMOS</td>
<td>~ Vg (^{-44}) ECB (substrate to poly)</td>
<td>~V (^{-33}) HVB&gt;EVB (Vg&lt;3.8) NBTI LIKE DEG EoxVox driven</td>
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CMOS DEVICE RELIABILITY -- CONCLUSIONS

CONCLUSIONS

HCI
- NMOS HCI CONTINUES TO BE OPTIMISED (ADJUSTING DOPING PROFILES)
- PMOS HCI BECOMES SIGNIFICANT AND CHANGES BEHAVIOR BELOW 0.18μ
  - (1) PHYSICAL MECHANISM HOLE TRAPPING, (2) WORST CASE BIAS CONDITION CHANGES AND (3) TEMP DEPENDENCE REVERSES

NBTI
- NBTI BECOMES A SERIOUS ISSUE, BEING INVESTIGATED THOROUGHLY.
  - RESONABLE UNDERSTANDING OF PHYSICAL PHENOMENA AND MODELS
  - NBTI RECOVERY MECHANISM IMPROVES LIFETIME

TDDB
- TDDB MODEL CHANGED FROM E OR 1/E TO POWER LAW DEPENDENCE
  - SOFT BREAKDOWN MUST BE CONSIDERED
  - SOME OVERLAPPING EFFECTS OF PMOS TDDB AND HCI MECHANISMS WITH NBTI