IEEE EDS DL Talk, Santa Clara Chapter

Development and Challenges on Reliability Characterization of CMOS Devices with Gate Oxide in the Tunneling Regime

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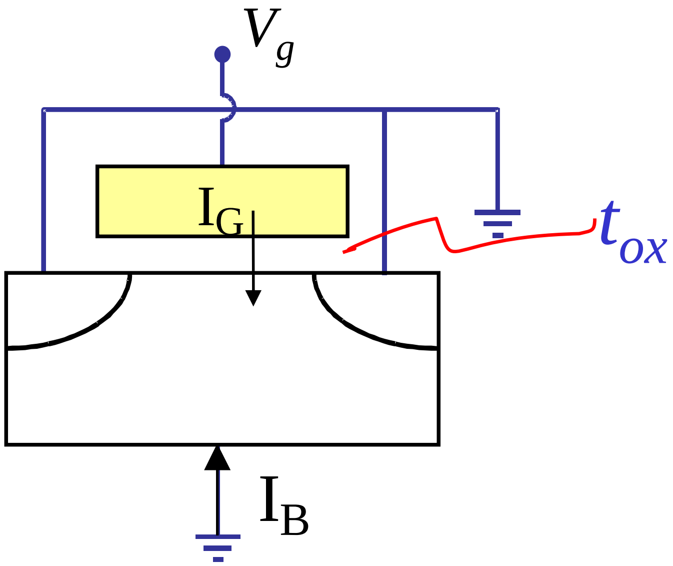
OUTLINE

- Introduction
- Charge Pumping Method
- Gated-Diode Method
- DCIV Method
- Applications to Oxide and HC/NBTI Reliabilities
- Recent Results on the Issues of Strained-silicon CMOS
- Conclusion

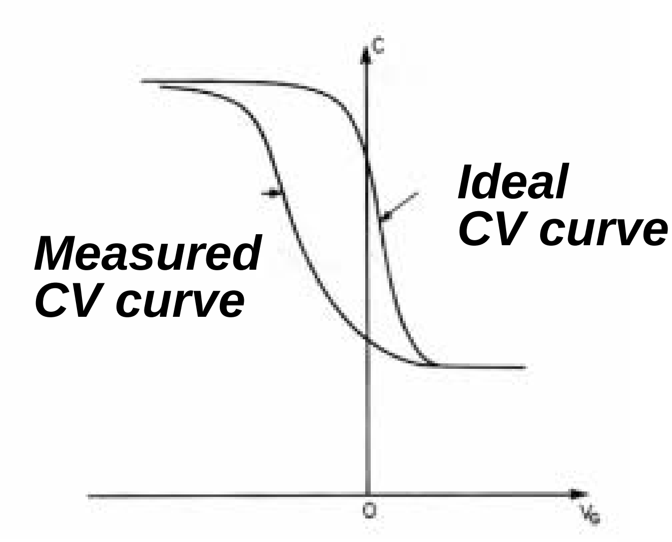
Motivation

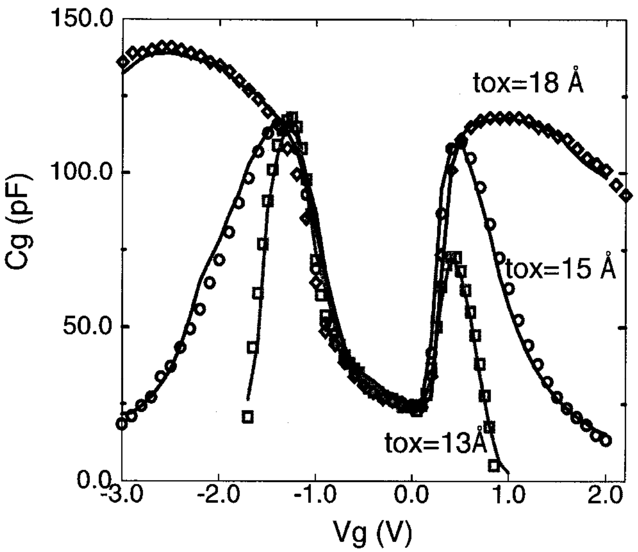
- **For the future 25-90nm CMOS Technology**
  - ***SION-based* thin-oxide and *high-k* are two possible candidates**
  - ***Reliable measurement techniques***
    - ***Need further development for process and device monitoring purpose***
  - ***need to overcome the measurement leakage for ultra-thin gate oxide***

I_G increases exponentially with t_{ox} scaling



Interface Traps Distribution - Calculated from CV Measurement





- **HF CV for thick gate oxide**
- **Large capacitor sample required**

- **CV for very thin gate oxide**
- **Tunneling leakage exists**

Ref: Choi et al., Symposium on VLSI Technology, pp. 63-64, 1999

Interface Characterization Techniques

- **Interface Oxide/Traps measurements**
  - **Conventional Methods**
    - ***CV method***
    - ***Charge pumping method (CP)***
    - ***Gated-diode method (GD)***
    - ***DC-IV method***
- **Limitations of the above methods**
  - ***CV method - for capacitors with thick gate oxide and large size***
  - ***GD, CP, DC-IV are limited by the gate leakage (tunneling) current***

(for very thin gate oxide)

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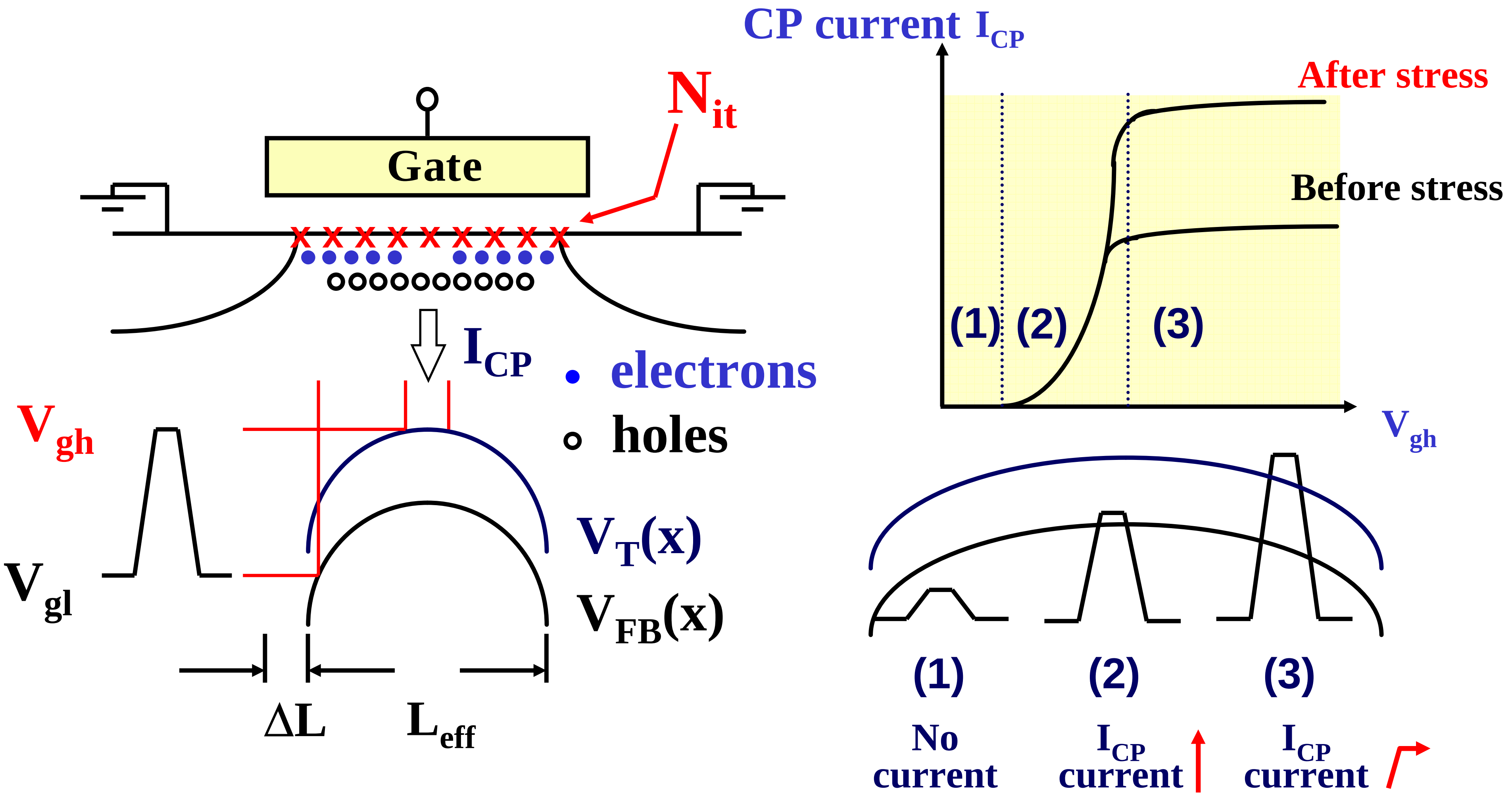
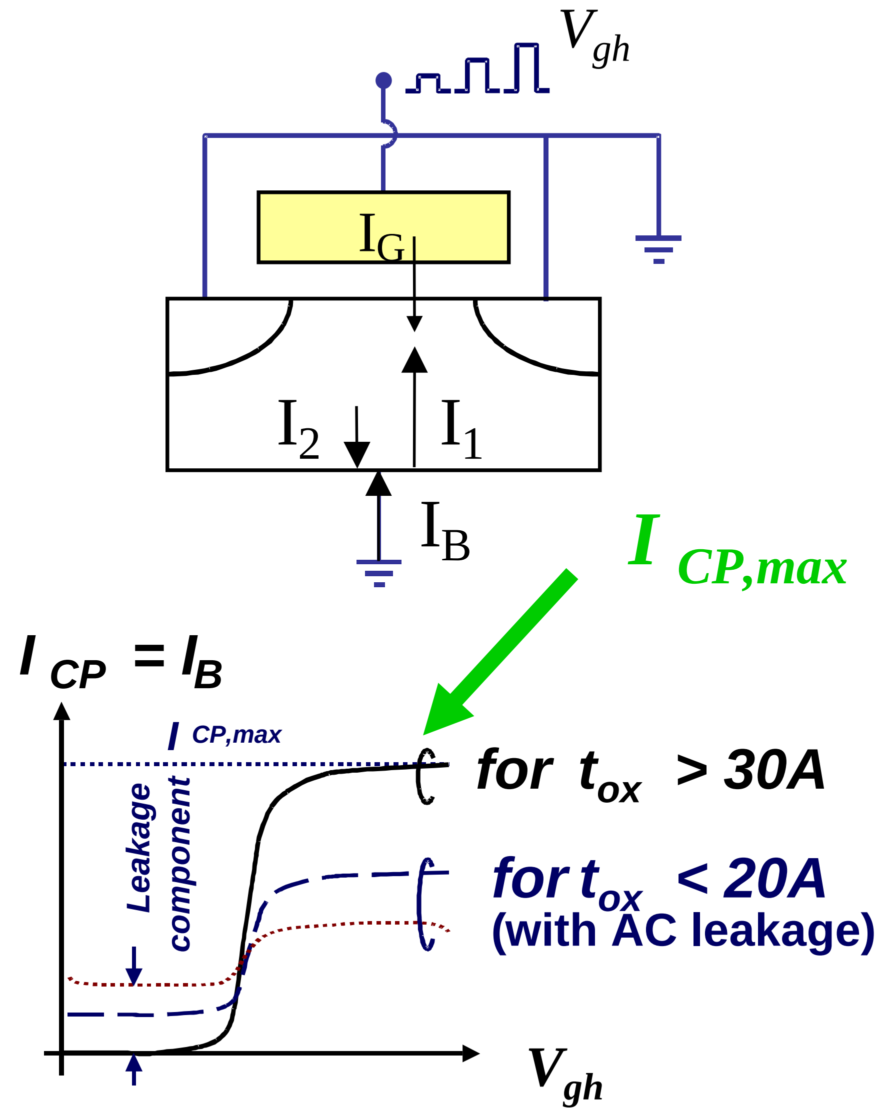
Basic CP Measurements

- CP Measurement with a Fixed Base-Level



Gate Leakage Current
During Experimental Measurement



1. From the measurement

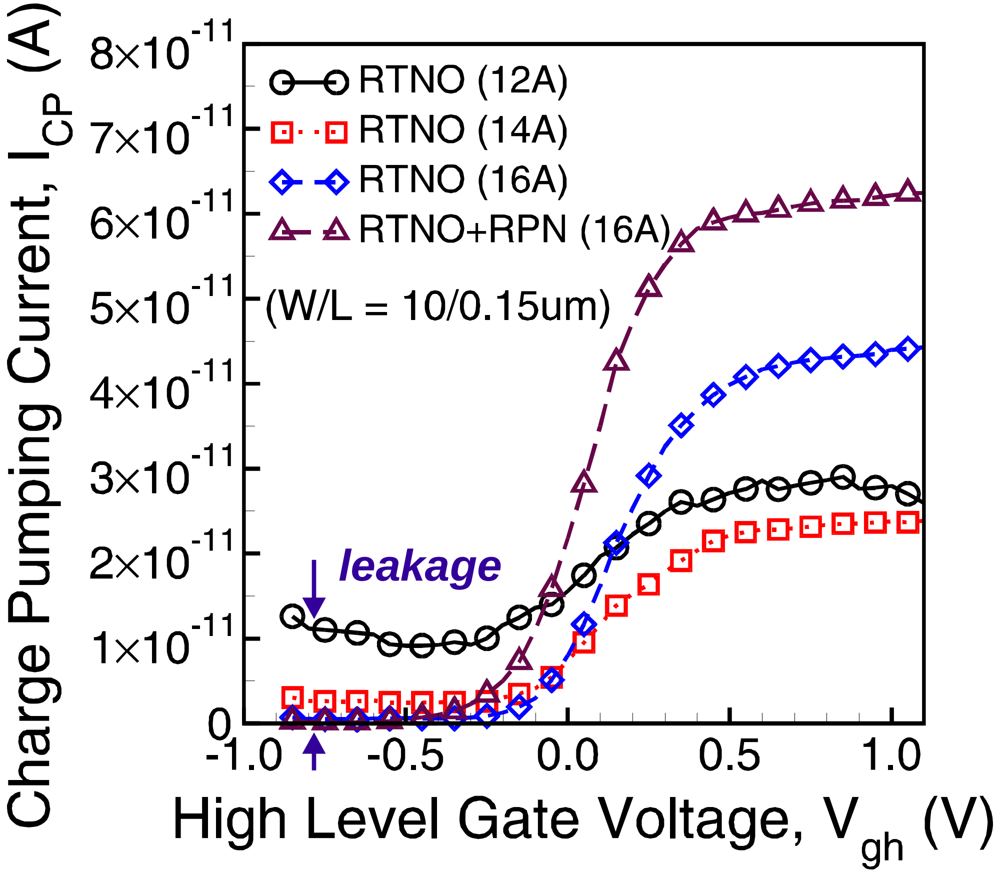
$$I_{CP} = I_B = I_1 - I_2$$

2. As gate oxide thickness reduces, I_G increases.
3. Measured charge pumping current consists of a leakage component.

$$I_{CP,max} = qfWN_{it}$$

Calculation of N_{it} will be wrong for ***tox< 20***Å if leakage is no taken care of.

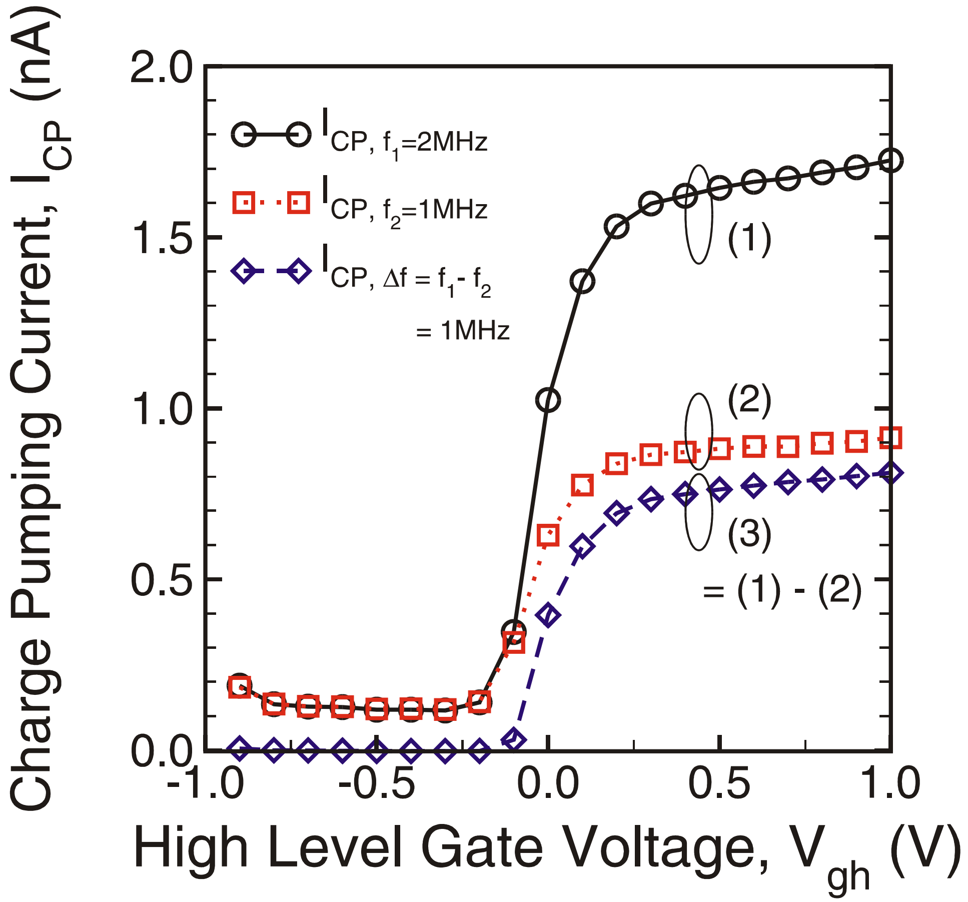
Measured Leakage Currents for Ultra-thin Oxide



- ***The 12A gate oxide has huge leakage component.***
- ***The leakage current level is almost equal to DC bulk current level.***
- ***RPN treated oxide has largest interface traps.***

The IFCP Method

(Incremental Frequency CP Method)



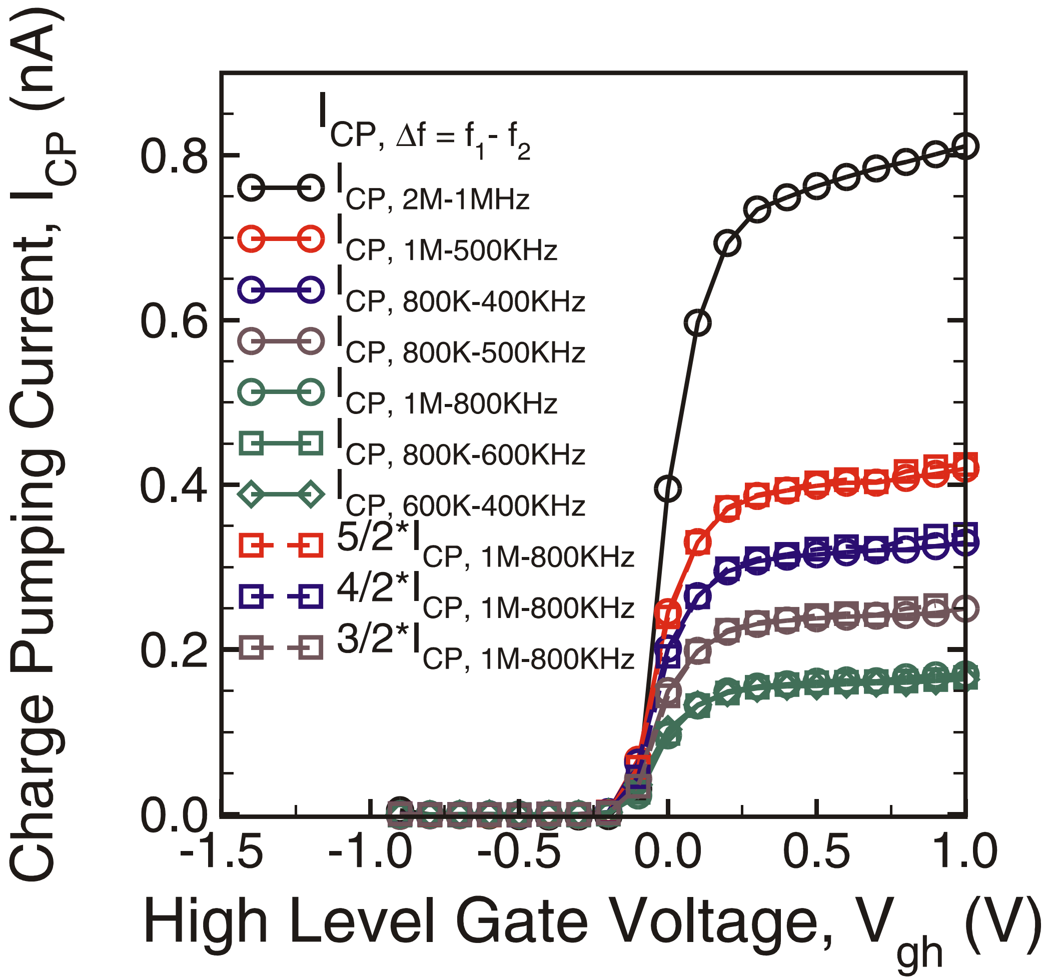
- **$I_{CP(f1,\ leakage)}$** **(1)**
  $= I_{CP(f1,\ correct)} + I_{CP\ (leakage@f1)}$
- **$I_{CP(f2,\ leakage)}$** **(2)**
  $= I_{CP(f2,\ correct)} + I_{CP\ (leakage@f2)}$

$\therefore \Delta I_{CP(f1-f2)}$ **(3) = (1) - (2)**
$\cong I_{CP(f1,\ leakage)} - I_{CP(f2,\ leakage)}$

$\therefore$ as f $\Uparrow$ and $f_1 \cong f_2$
$\rightarrow \Delta I_{CP(f1-f2)} \cong I_{CP(f1-f2)}$

Ref: S. S. Chung et al., Symposium on VLSI Technology, p. 74, 2002

Incremental Frequency CP Method



- ***Charge pumping current (I_{CP}) is proportional to frequency (f).***
- ***Using two adjacent frequencies to calculate the corrected CP curve.***
- ***e.g.,***
  $I_{CP(800KHz)} - I_{CP(600KHz)} \cong I_{CP(600KHz)} - I_{CP(400KHz)} \cong I_{CP(200KHz)}$

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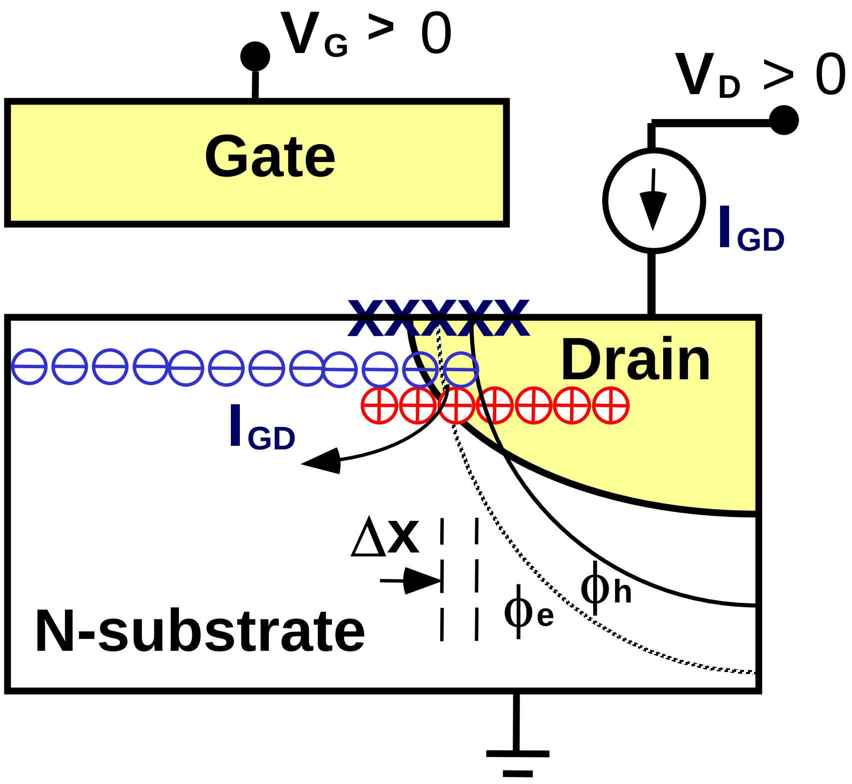
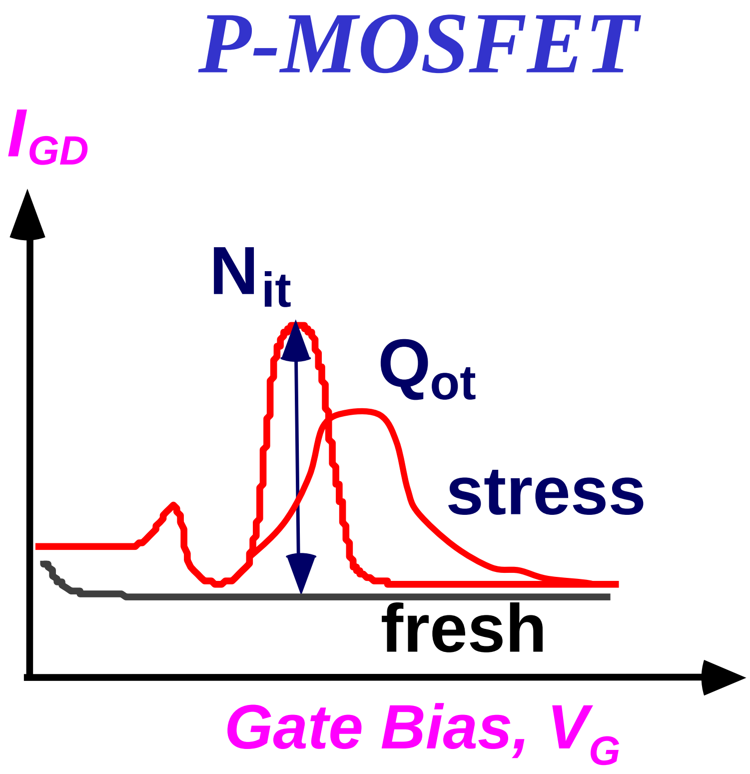
Gated-diode Measurement Technique



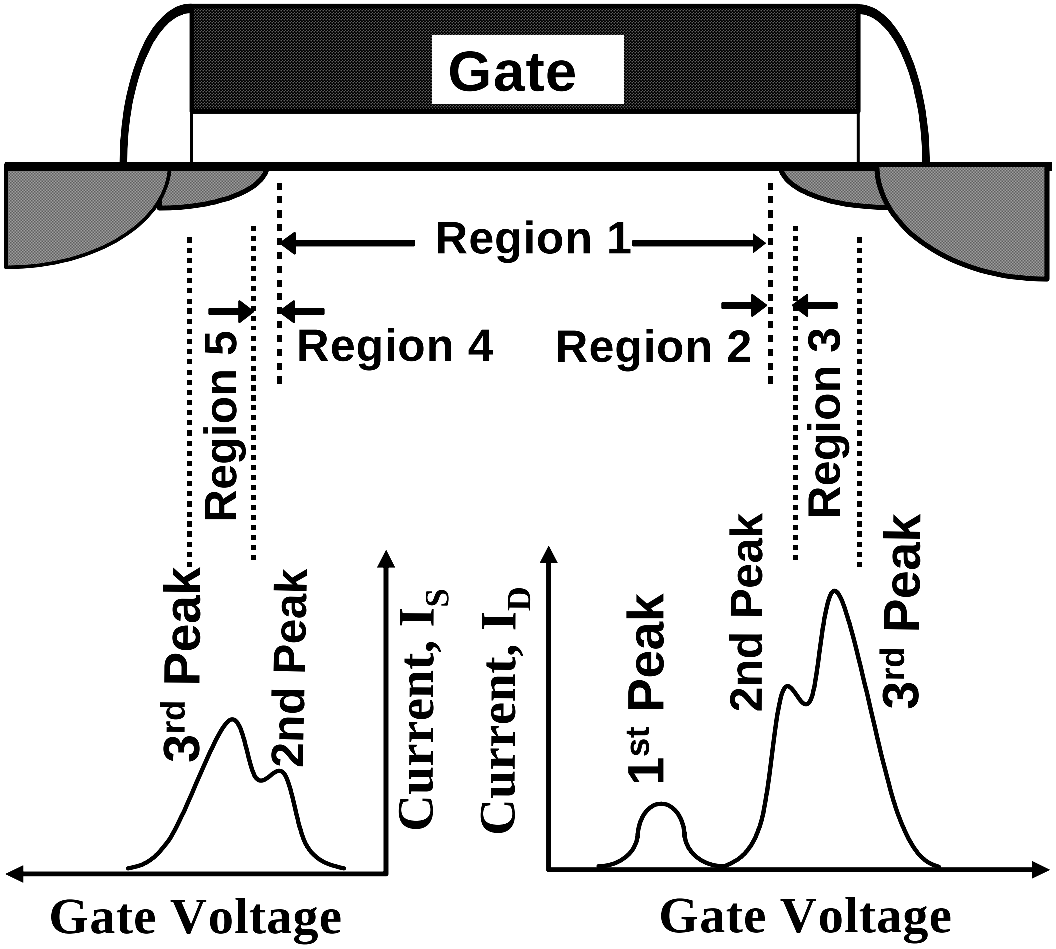


- Drain junction is forward-biased, V_G is applied, and I_{GD} is measured.
- If N_{it}/Q_{ot} exists, the recombination current increases.

Ref: S. S. Chung et al., Symposium on VLSI Technology, p. 111, 1997

Demonstration of Gated-Diode Method

- Measure drain and source current peaks *

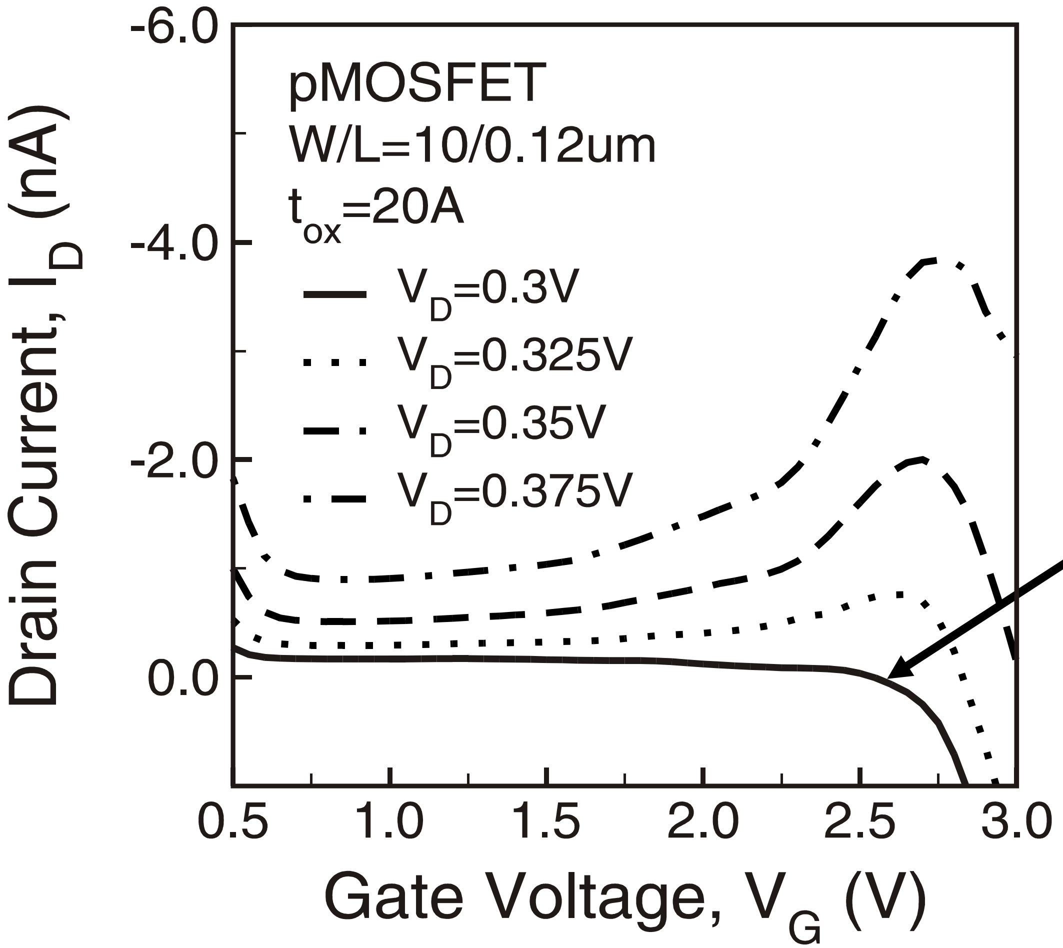


- ***Peaks represent the** interface trap(N_{it}) or oxide trap (Q_{ot}).*

- ***1st peak-** in channel region (1)*
- ***2nd peak:** at junction region (2 & 4)*
- ***3rd peak-** at S/D extension region (3 & 5)*

- **Results similar to DCIV method-** **[ref] C. –T. Sah, Invited talk at 6th ICSICT, Shanghai, October 23, pp.1-15, 2001**

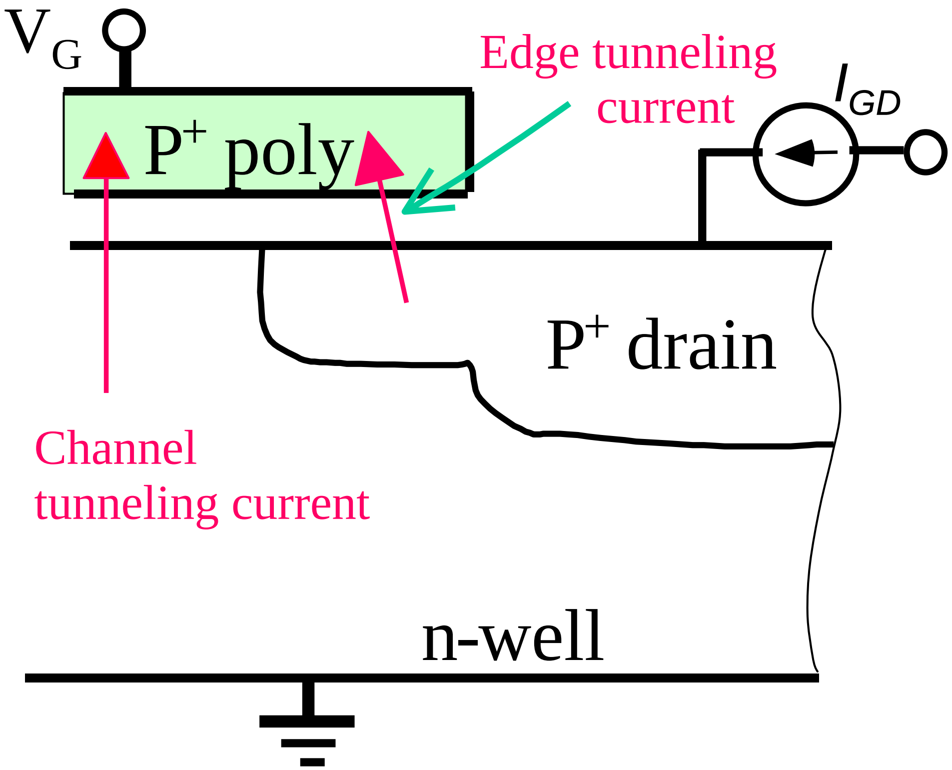
A typical result for ultra-thin gate



Edge tunneling dominates

- At low V_D bias and high V_D, edge tunneling current is dominant.
- Peak can be seen by raising V_D.

Why low leakage Gated-Diode Measurement ?



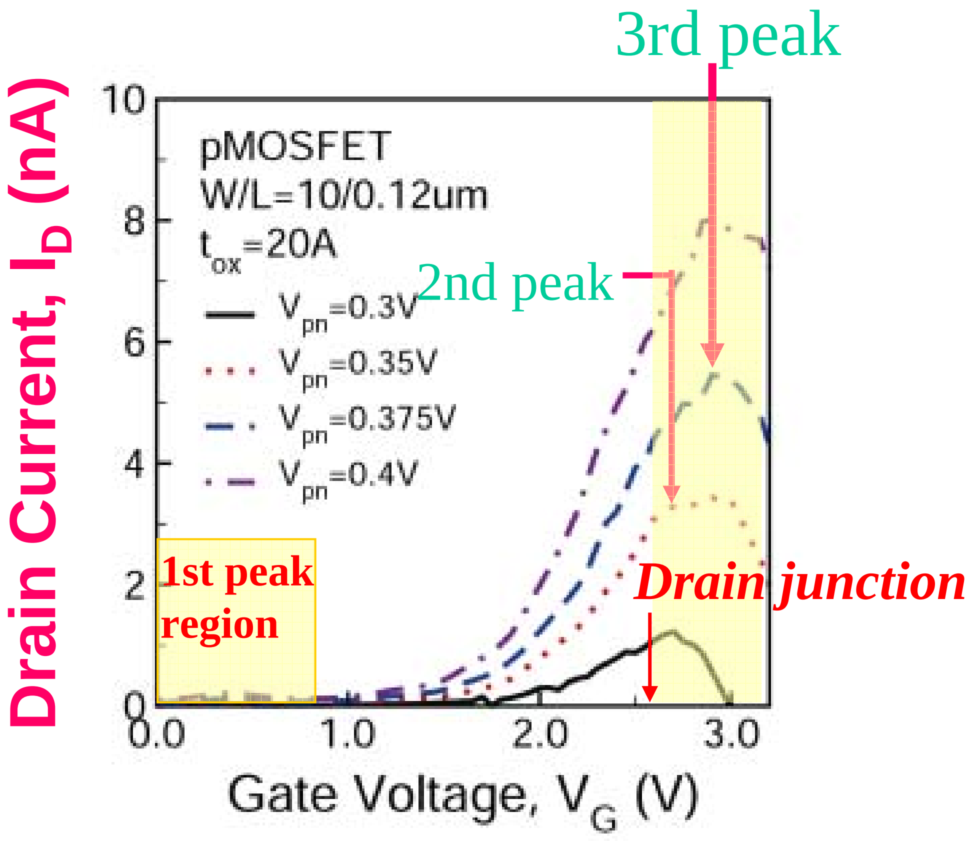
$V_D < 0.2V$
(previous approach)

Changed to 0.3V~0.5V

- 2 leakage components
- currents need to be suppressed
  - *Edge tunneling current can be prevented by raising V_D.*
  - *Channel tunneling has minor effect to I_{GD}.*

Gated-diode Measurement Results

(for a pMOSFET after 5000s stress at $V_G = V_D = -2.5V$)

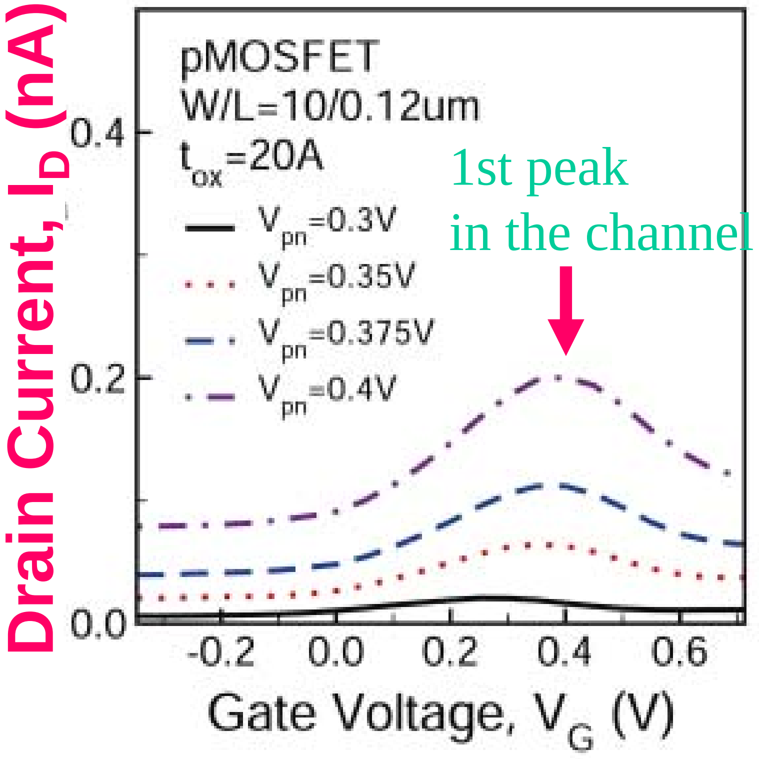


3rd peak

2nd peak

1st peak region

Drain junction



1st peak
in the channel

- For a sensitive measure of the I_D, a little larger V_{pn} at the drain junction can be used.

Ref: S. S. Chung et al., in IEDM Tech. Digest, p. 513, 2002

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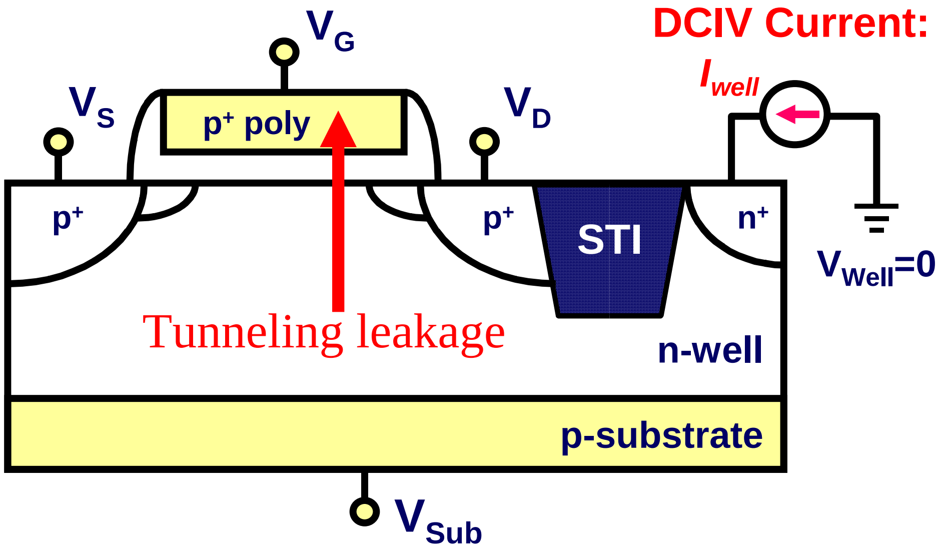
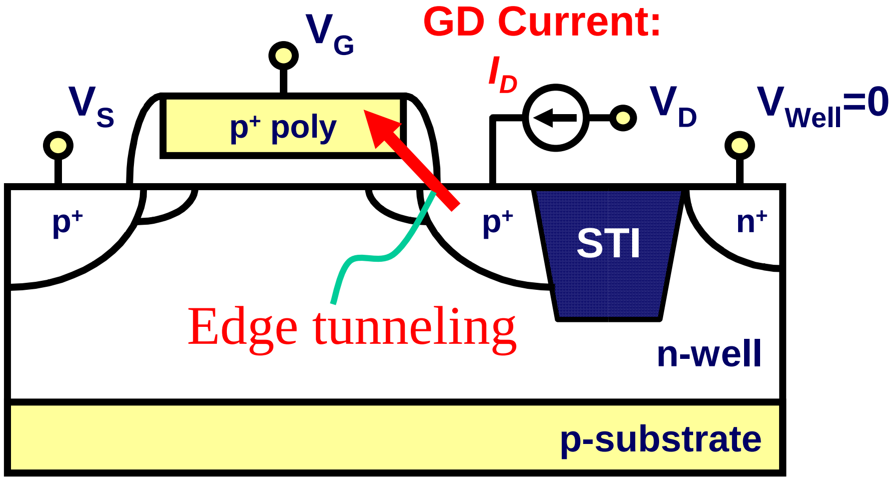
Comparison Between DCIV and Gated-Diode Measurements (continued)



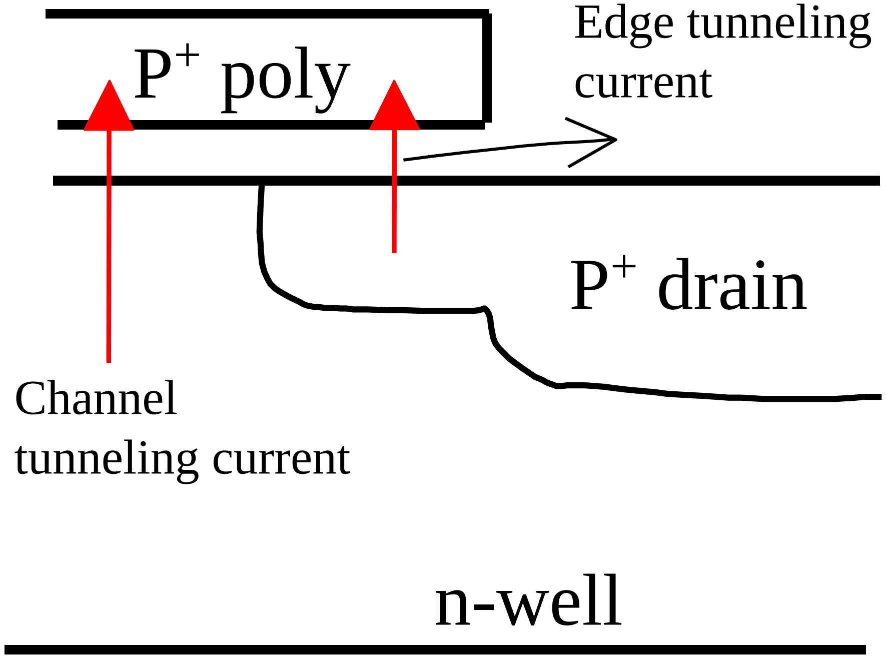


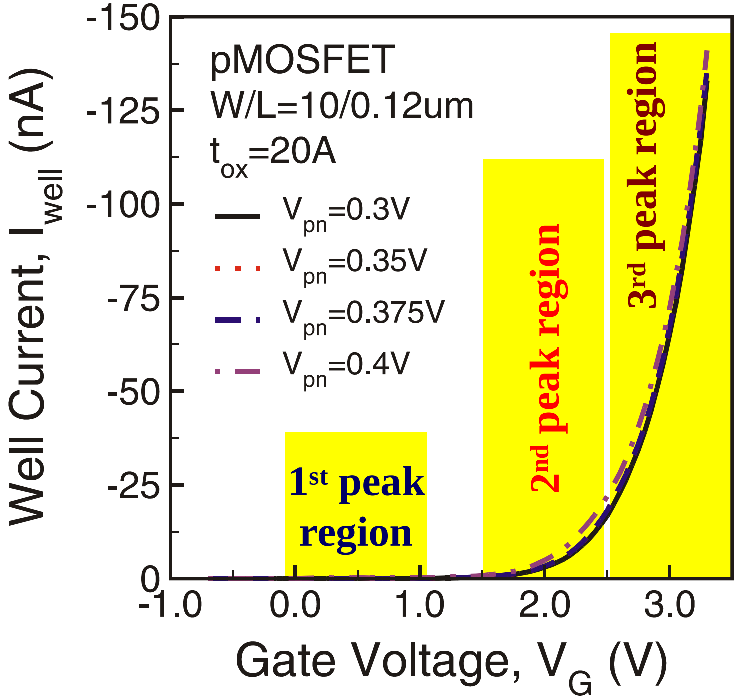
DCIV method

Gated-Diode method

*[8]: A. Neugroschel and C. T. Sah,
T-ED, p. 1657, 1995.*

Leakage Components in Ultra-Thin Gate Oxide





- As gate oxide thickness reduces, two leakage currents occur.
- First peak is invisible due to channel tunneling current.
- The second and 3rd-peak are invisible due to edge tunneling current. (right figure)

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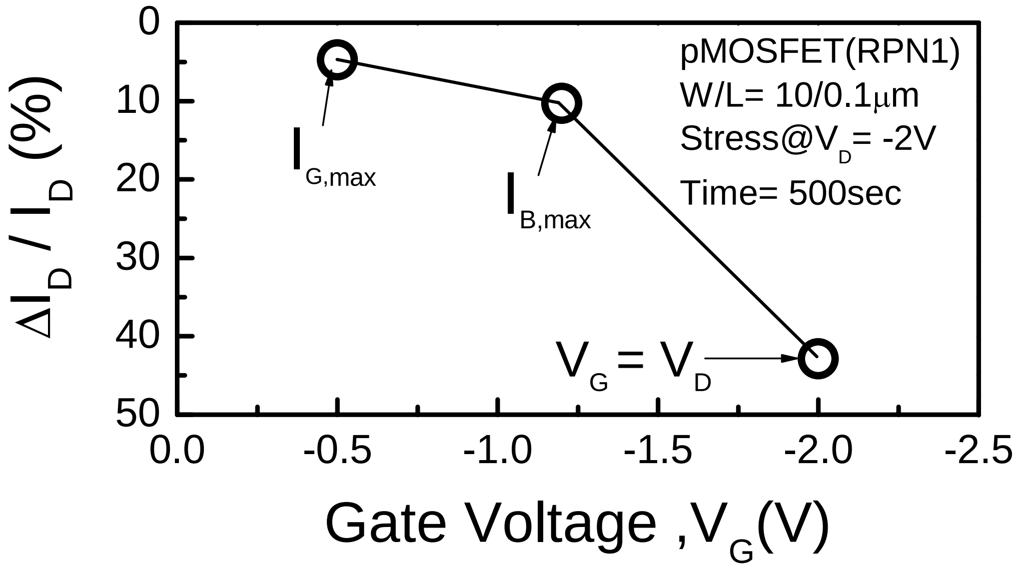
Charge Pumping Method

The Observation of Hot Carrier (HC) Degradation Effect

- Drain current degradation after various HC stresses



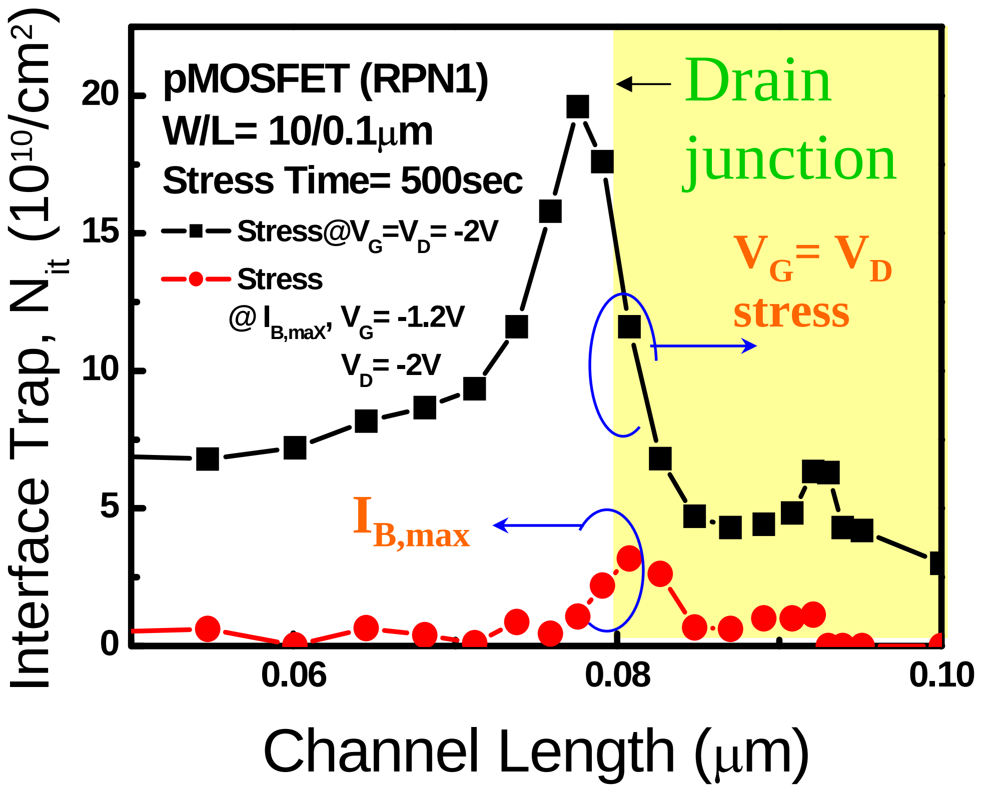
- ***For p-MOS Devices***

➔ **Max. degradation: V_G=V_D stress**

➔ **Both N_{it} and Q_{ot} affect device degradation.**

Charge Pumping Method

Lateral Profiling Results for L_{eff}= 60nm, EOT= 16Å pMOSFET

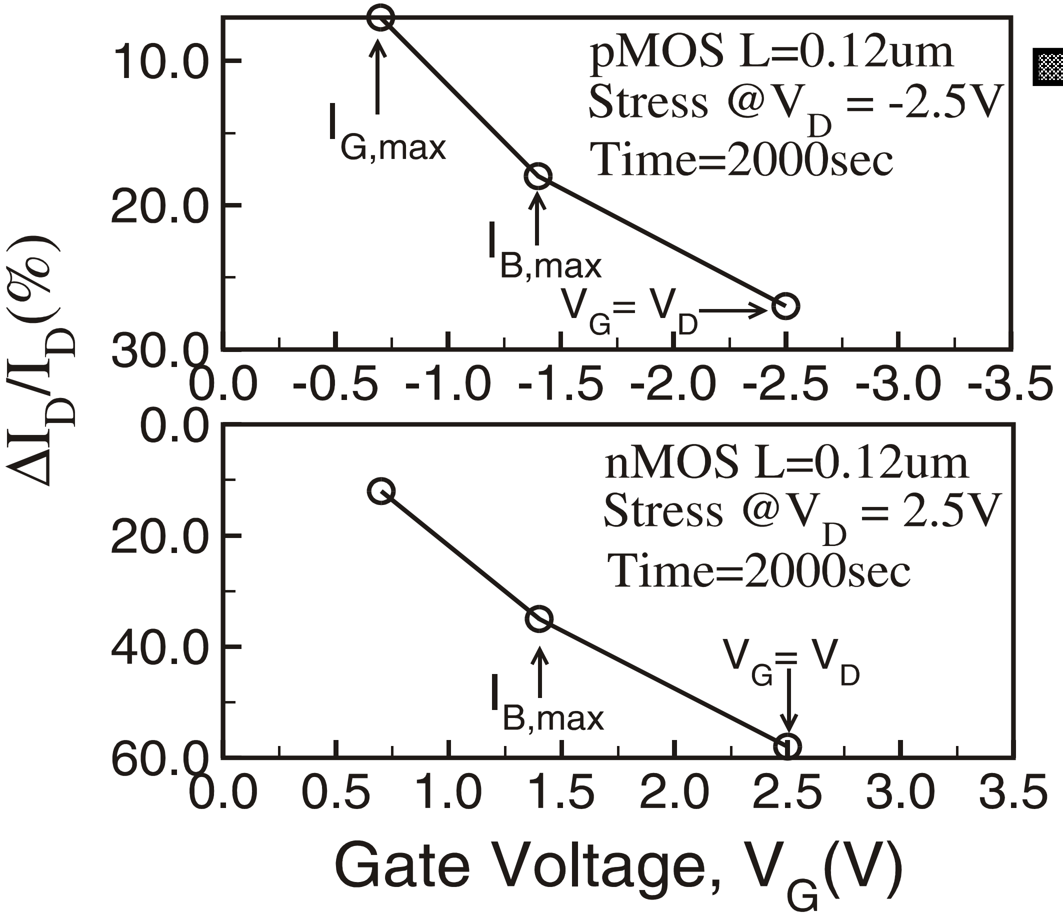


- ■ ***Comparison between $I_{B,max}$ and V_G= V_D stresses***
- ➔ **Max. degradation: V_G=V_D stress**
- ➔ **The generated N_{it} at *$I_{B,max}$ is smaller.***

Gated-Diode(GD) Method

The Observation of Hot Carrier (HC) Degradation in CMOS Devices

- Drain current degradation after various HC stresses



- ***Both in n- and p-MOS Devices***

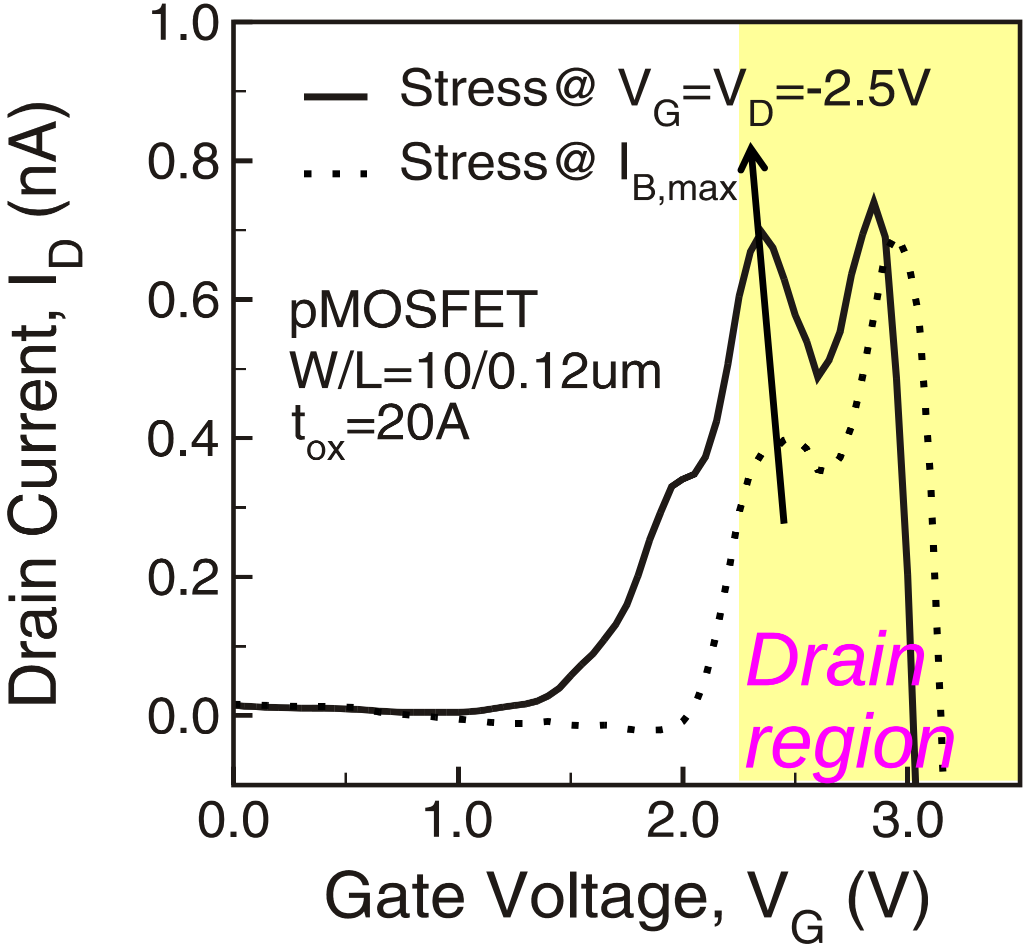
➔ **Max. degradation: V_G=V_D stress**

- ***HC effect in nMOS device is more serious than that of pMOS device.***

Gated-Diode(GD) Method

Examination of GD currents(continued)

- Comparison between HC (V_G = V_D) and $I_{B,max}$ stress

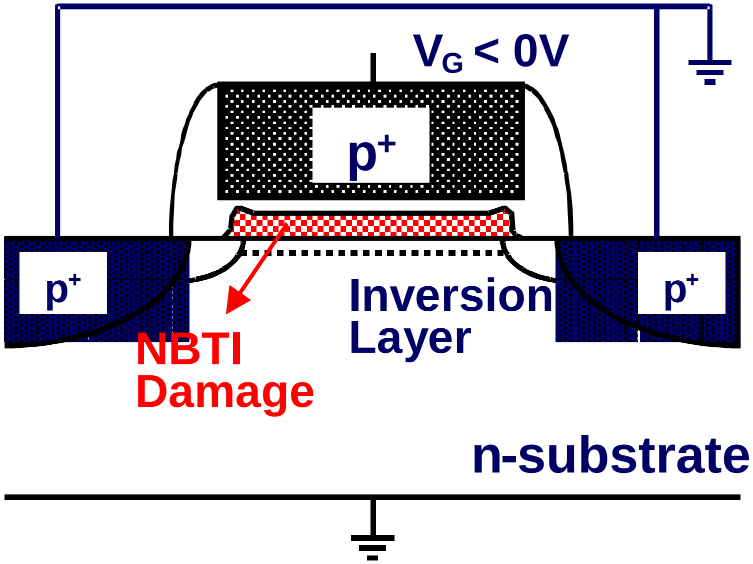


■ ***HC-induced damage***

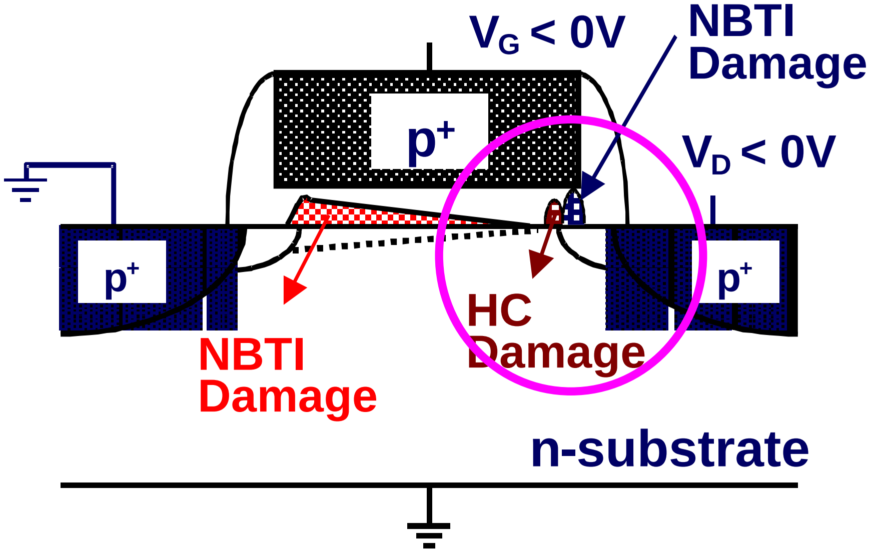
- **V_G= V_D stress generates larger degradation than $I_{B,max}$.**
- **Interface trap generation increases rapidly at the junction region at V_G=V_D stress.**

Ref: S. J. Chen et al., in Proc. IRPS, p. 203, 2003

Comparison Between NBTI and NBTI-Like



(a) NBTI Stress

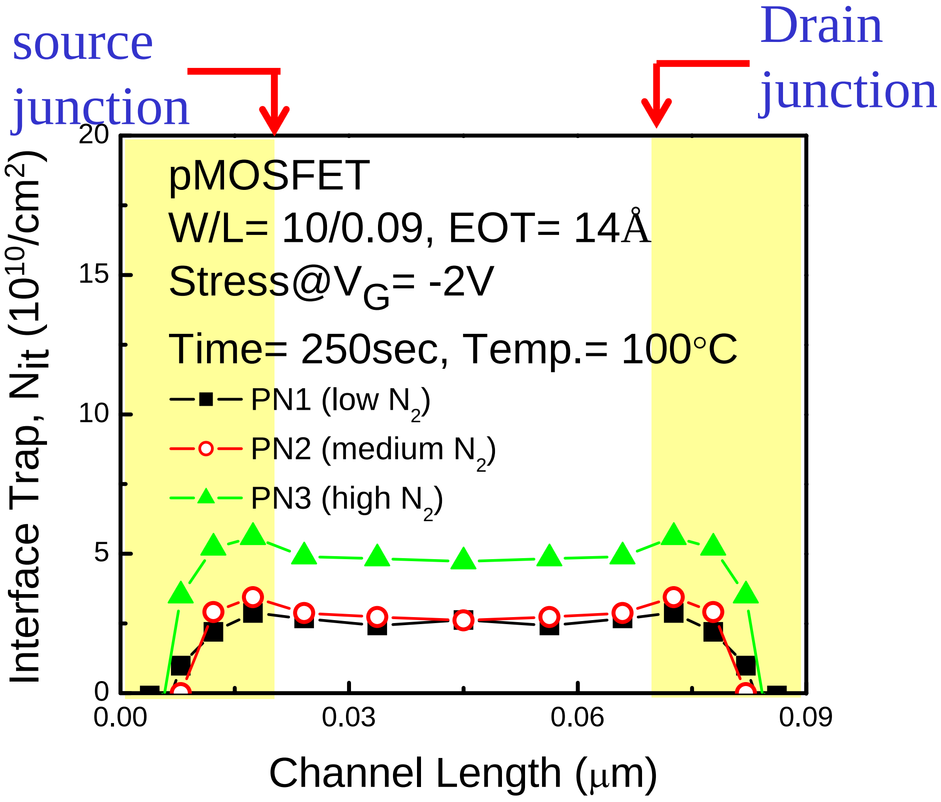


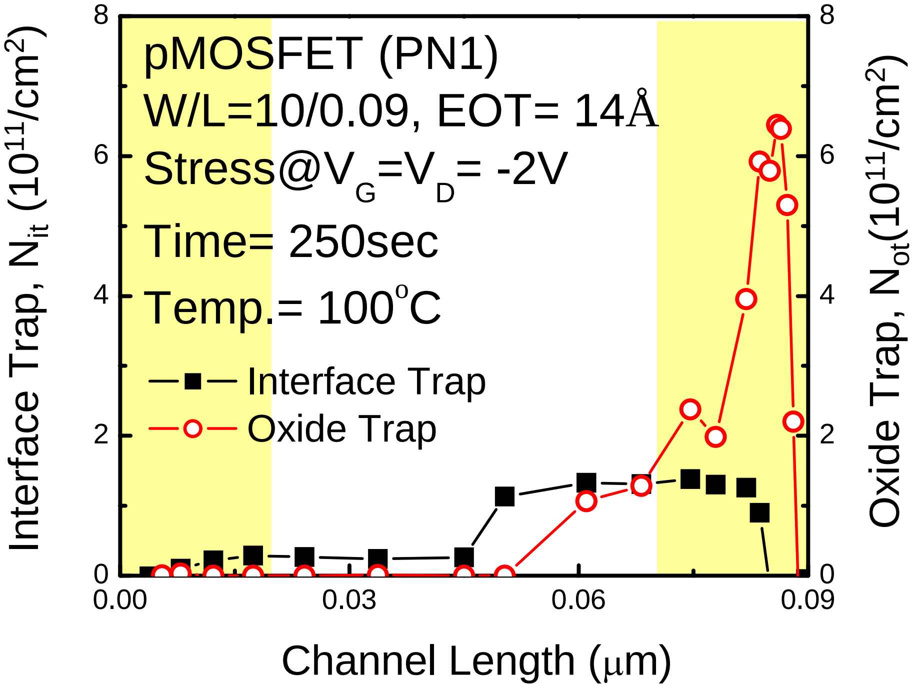
(b) NBTI-like HC Stress

- ***NBTI (symmetrical)– damage occurs at both sides of S/D region.***
- ***NBTI-like(asymmetrical)- Extra damage is observed inside the drain junction region.***

Ref: S. S. Chung et al., in IEDM Tech. Digest, p. 513, 2002

Profiling Results for NBTI and NBTI-Like



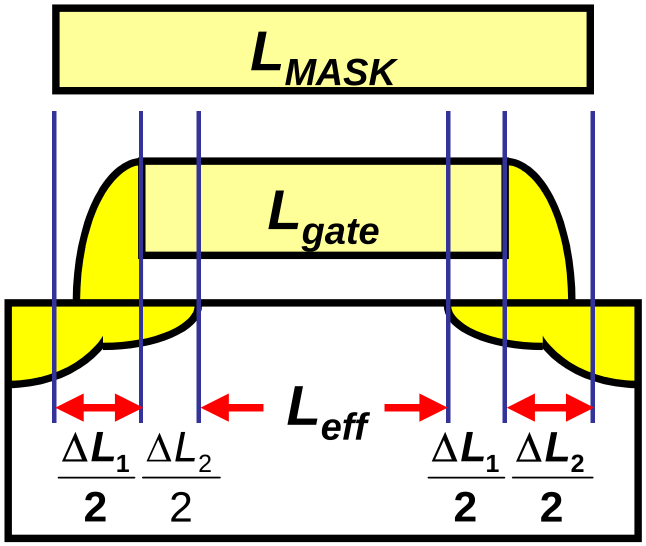


- The heaviest plasma nitrogen density has the worst reliability after NBTI stress.
- The N_{it} is dominant of the device degradation since N_{it} has larger values inside the channel region.

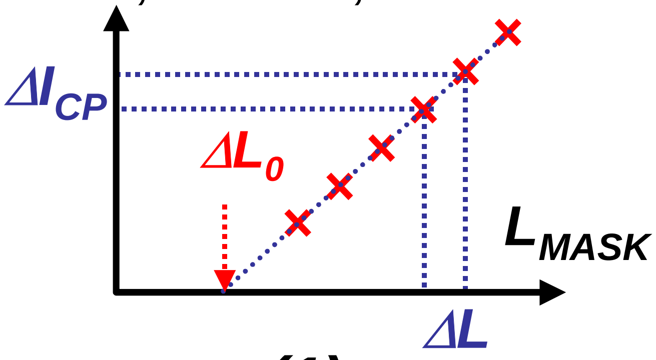
Ref: S. S. Chung et al., in IEDM Tech. Digest, p. 477, 2004

Process Monitors by CP Method

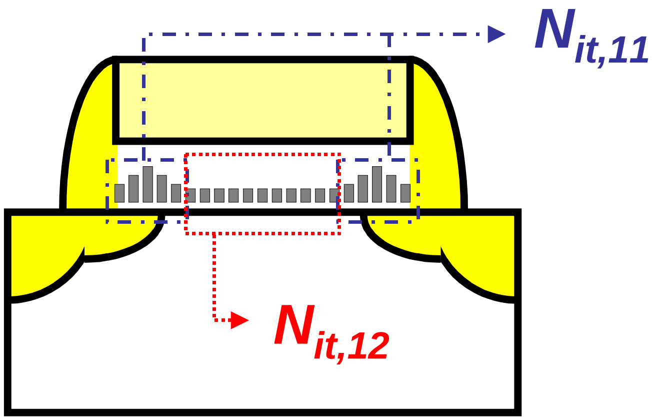
Extraction of Lateral Diffusion Length ΔL



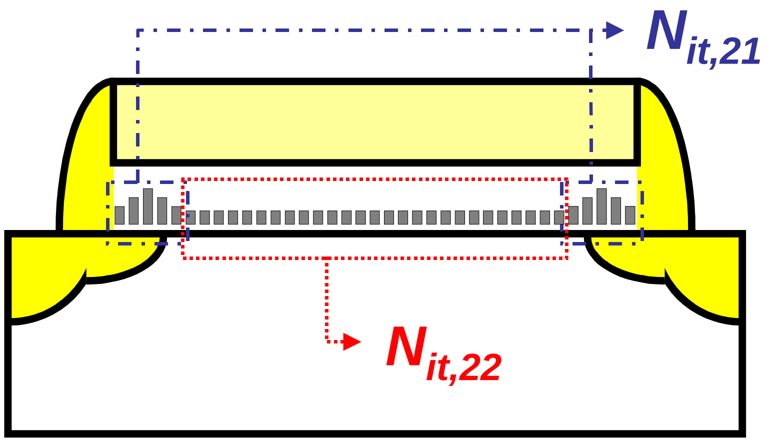
$I_{CP,max} \propto N_{it,total}$



(1)



Short Channel Device

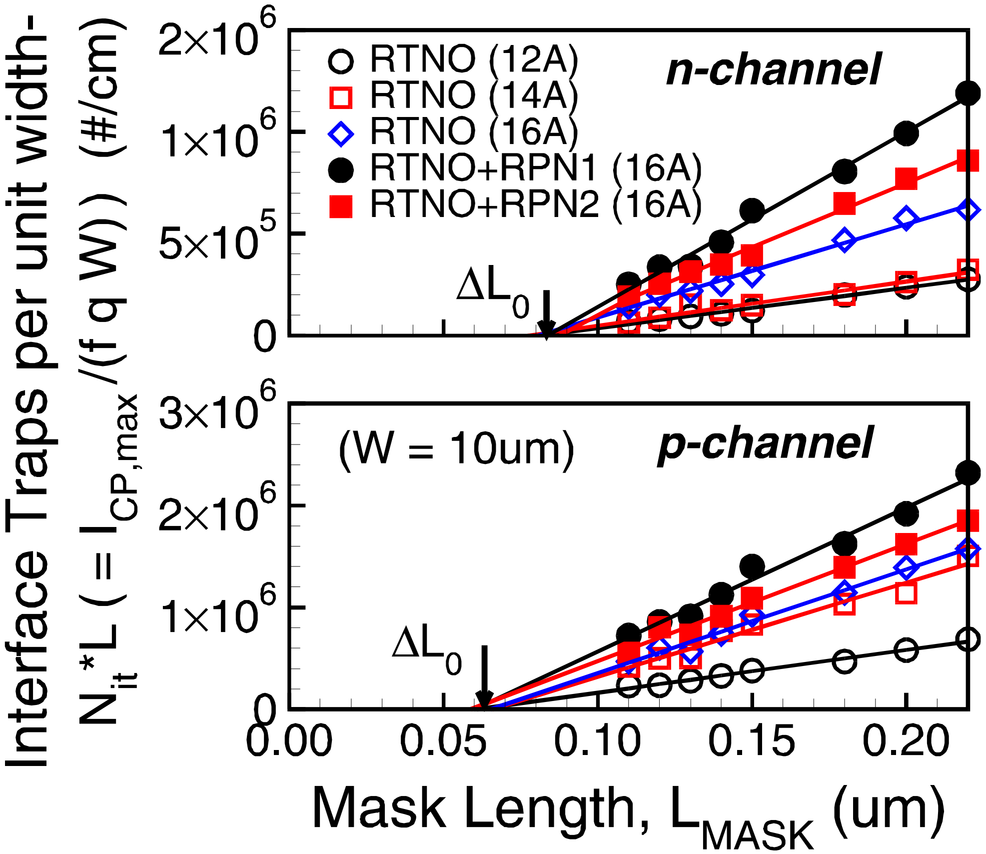


Long Channel Device

(2)

Process Monitors by CP Method

Oxide quality monitor- from the slope



- ***Effective channel length is independent of oxide quality.***
- ***ΔL_0 - the S/D lateral diffusion length***
- ***16A RPN treated oxide has larger amount of interface traps.***

Ref: S. S. Chung et al., Symposium on VLSI Technology, p. 74, 2002

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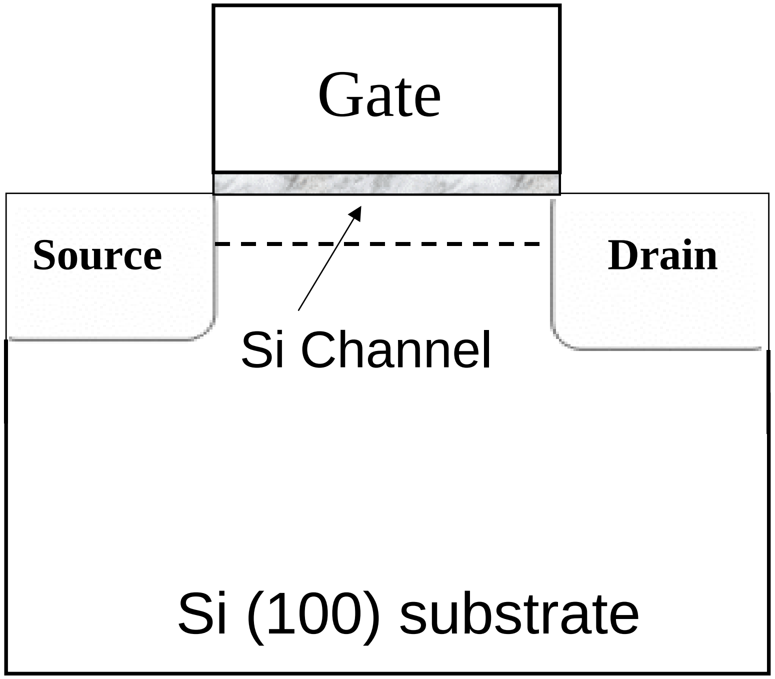
Challenging of Reliability in Strained-silicon CMOS

- **Mobility enhancement**
  - *Can be achieved with Si/SiGe, CSEL(nitride-capping layer, and hybrid substrate technologies*
  - *Provide mobility enhancement with a factor of 50% to 100%*

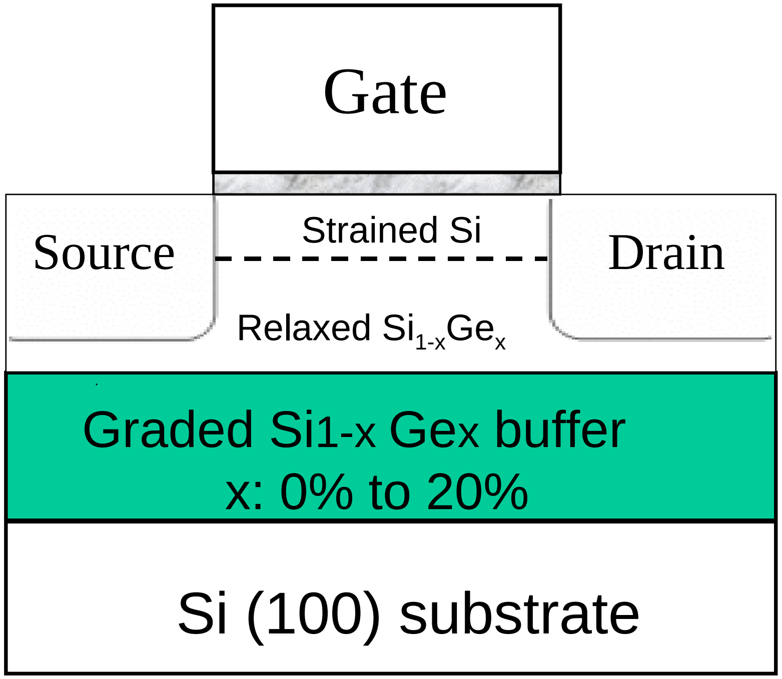
- **What we see from previous studies**
  - *Most of the studies were focused on device performance*
  - *Not until 2005, it was found that a large enhancement in mobility may* <u>*degrade the device reliability*</u>*.*

S. S. Chung et al., Symp. on VLSI Tech., p. 86, 2005.
S. S. Chung et al., in IEDM Tech. Dig., p. 567, 2005.

Biaxial-strained SiGe vs. Bulk-Si nMOSFETs



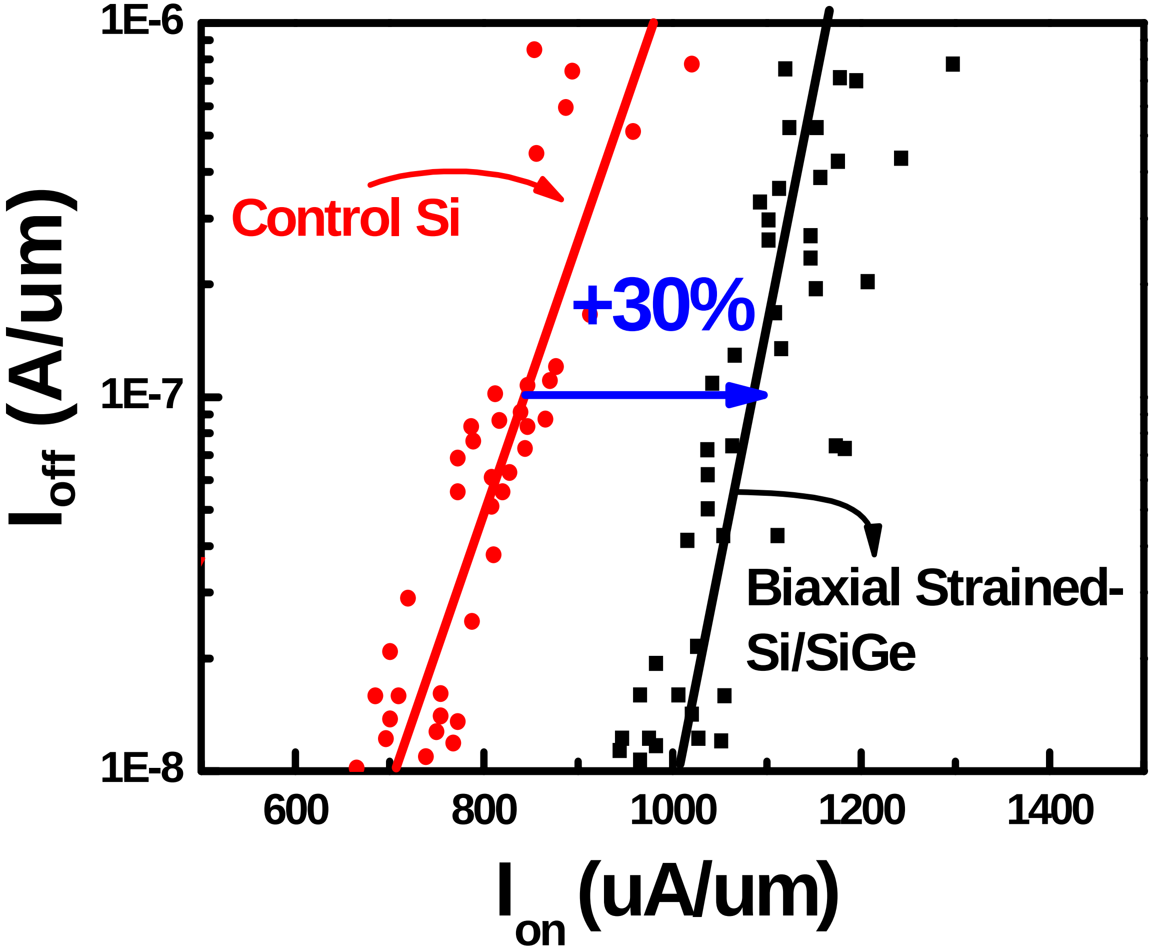
(a) control-Si



(b) Bulk strained-Si/SiGe

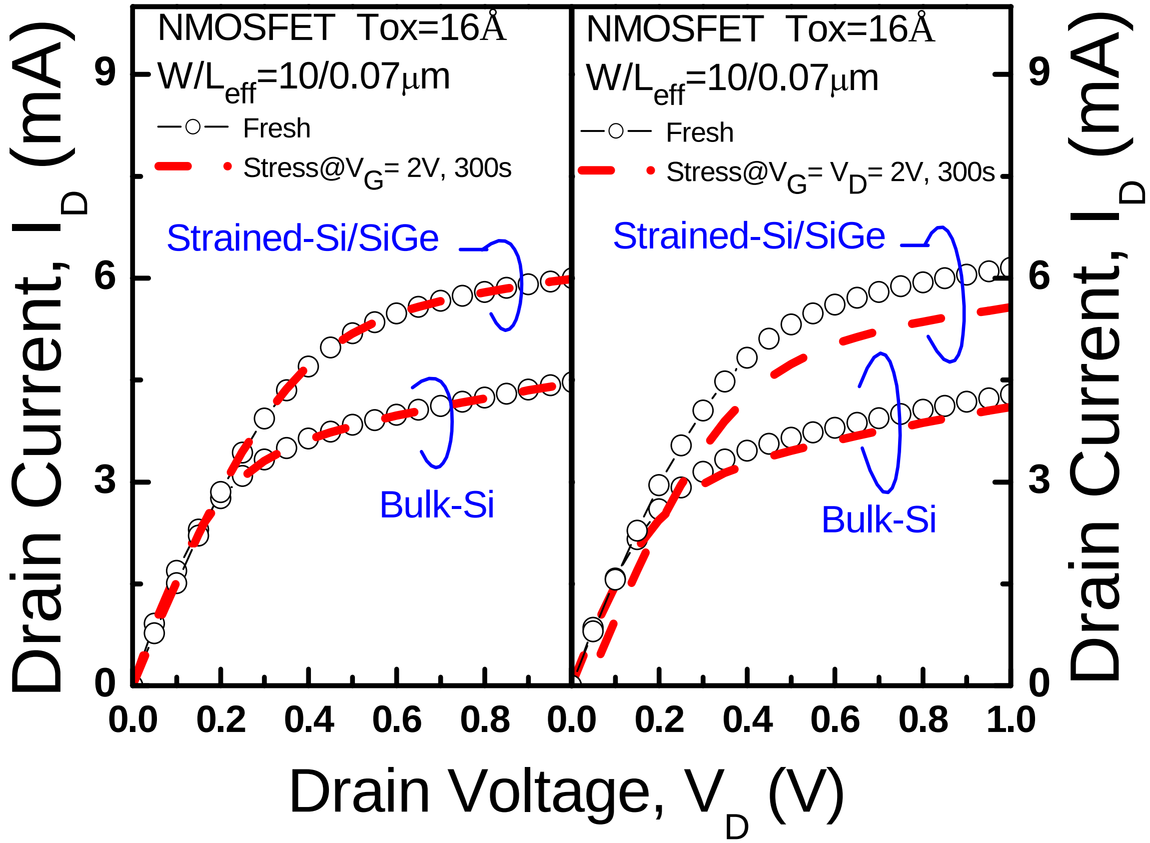
S. S. Chung et al., p. 86, Symp. on VLSI Tech., 2005.

Driving Current Enhancement-Si/SiGe Devices



- ❑ *Enhancement of the driving current is 30% for biaxial-strained Si/SiGe n-MOSFETs.*

Observation of the Hot Carrier Degradation-
(biaxial) Strained-Si vs. Bulk-Si Devices

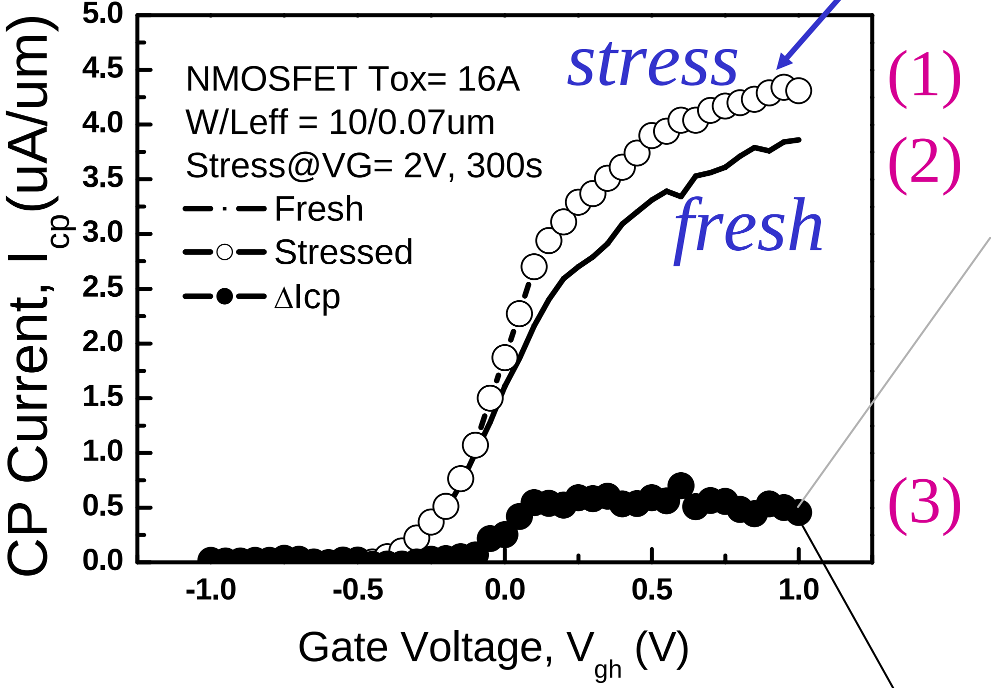


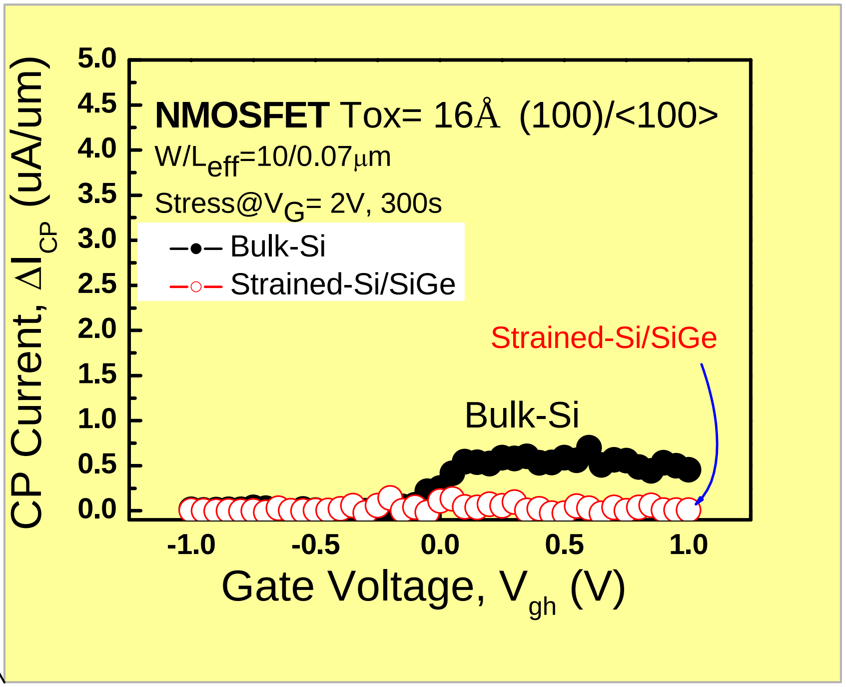
- *After the HC stress at $V_G = V_D$, the ΔI_D in strained-Si devices is enhanced comparing to bulk devices.*

Observation from charge pumping measurement -

FN Stress at V_G= 2V

$$I_{cp,max} = qWLfN_{it}$$

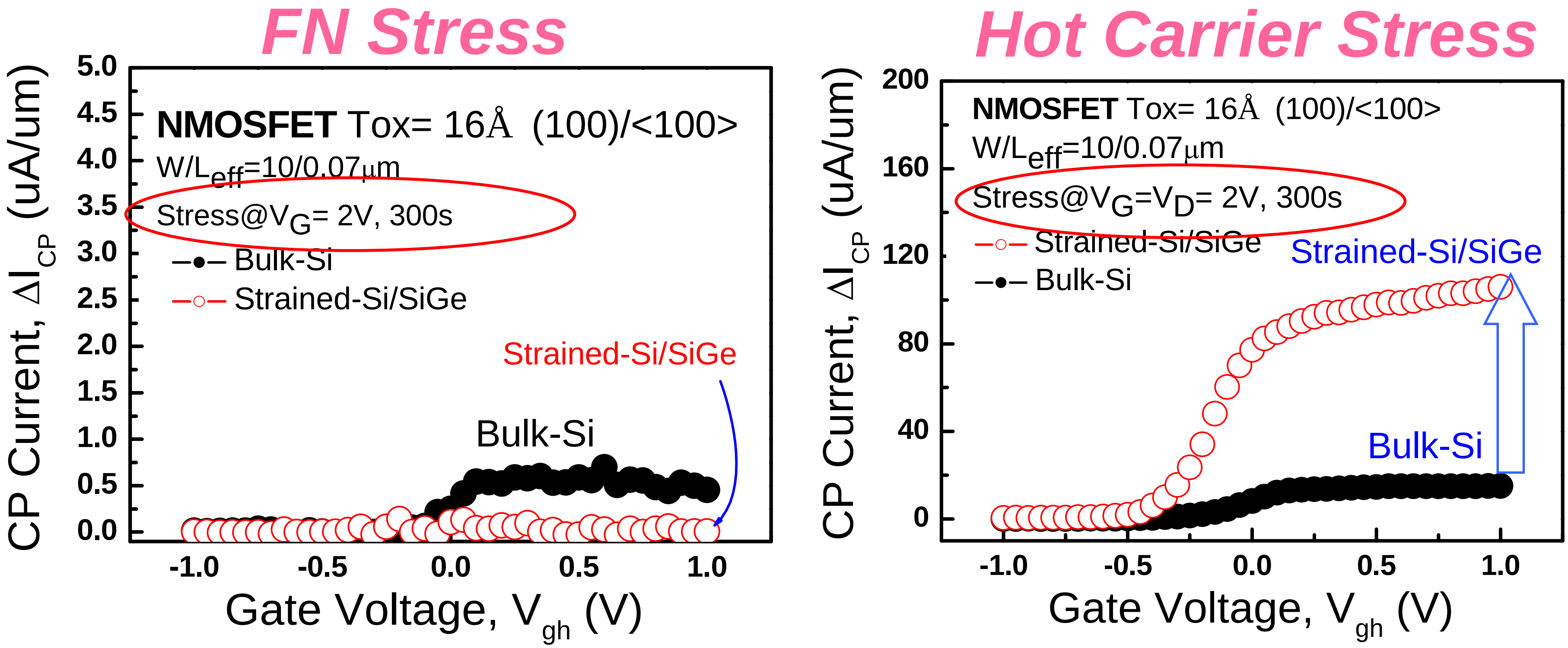




(1) - (2) = (3)

Stress *fresh* ΔI_{CP}

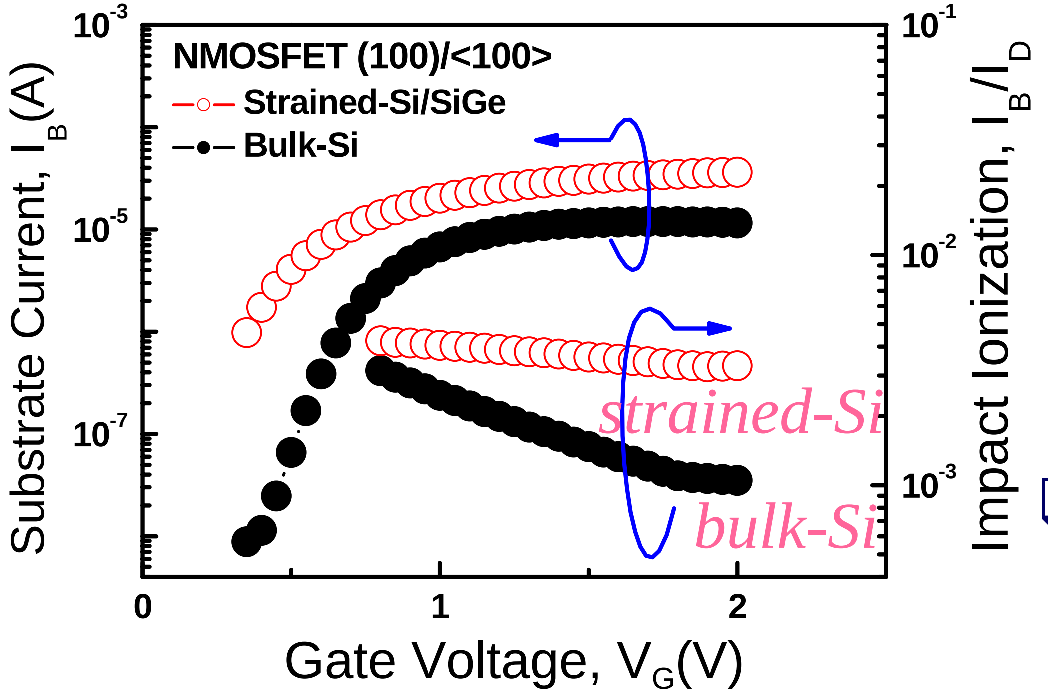
FN Stress Vs. Hot Carrier Stress



- *FN stress, $\Delta I_{CP's}$ are about the same.*
- *HC stress, the increase of CP current is larger in strained-Si/SiGe devices, which means a huge generation of N_{IT}.*

- *Mechanism* → *induced by lateral field effect*

A much larger degradation in strained devices can be explained from-
Impact Ionization Rate



- ❑ *Impact ionization substrate current is much larger in strained-Si devices, as a result of the narrower band gap and higher lateral field.*
- ❑ *This enhancement is the key factor to severely degrade the strained-Si devices.*

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Conclusions

- The leakage current for the thin gate oxide device measurement has been a major roadblock for 90nm and beyond CMOS device development.
- Two low leakage methods have been demonstrated for the characterization of CMOS devices with thin-gate oxide down to the 1nm range:
  - The IFCP is simple and easy to implement, which can replace the conventional CV method for interface characterization.
  - Gated-diode method allows a sensitive measure of interface/oxide traps along the channel.

Conclusions(continued)

- Charge pumping method is most suitable for HC reliability measurement. While, gated-diode measurement is suitable for NBTI reliability measurement.
- To design a high mobility scheme in CMOS while keep good reliability is challenging for the high-end logic device technologies.

Acknowledgments

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