



# Crystalline-Silicon Photovoltaics: Maximizing Cell and Module Performance

*PV Technology to Change the World*  
*IEEE SCV-EDS and Applied Materials*  
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# Agenda

- Company Background
- What is a *Technology Architecture*
- Technology Overview
- Roadmap
- Summary

# About Advent Solar

- Six year old, privately funded solar company
- HQ in Albuquerque, NM, USA
- Experienced management team
  - Solar technology expertise
  - Semiconductor expertise
- Advent Solar® Ventura™ Technology
  - The industry's only comprehensive cell-to-module solar architecture
- Applying semiconductor technologies to solar
- Accelerating the PV silicon learning curve
- Bringing grid parity economics sooner



***Best blueprint for the industry's leading solar modules***

# What is a *Technology Architecture*?

- Architecture refers to the platform of materials, processes, design, and standards that defines the technology product generation.
- Term common in software, semiconductor, and IT industries.
- Example: Intel microprocessor requires a set of chips for supporting functions, embedded software, operating system software, and large set of standards to maximize system performance.

# *Technology Architecture of PV ca. 2008*

- Entire PV value chain has few standards between links.
- Inefficiencies in material supply, equipment vendors, manufacturing, and system integration.
- *Conventional* c-Si cell/module technology still dominates market.
- Conventional c-Si cells, modules, and system use basic design and approach that is well over 20 years old.
- No explicit integration of design and features between c-Si solar cells, modules, and systems.
- Architecture for *non-conventional* PV technologies is even less defined.

# Conventional Crystalline-Silicon PV

## ■ Cell Technology

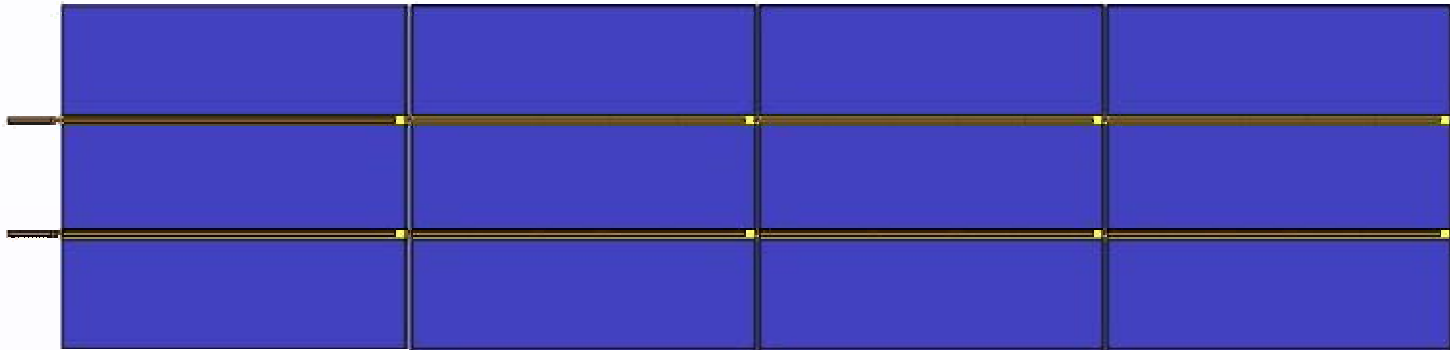
- Screen-printed Ag grids on front surface
  - Low processing cost and ease of manufacturing
  - Poor contact and grid resistance
  - Poor emitter performance (voltage and current)
  - Optical loss
- Al-alloyed back-surface field (rear contact)
  - Low cost processing and ease of manufacturing
  - Modest electrical & optical performance limits thin cell efficiency
  - Significant stress
- Limits obtainable efficiency and wafer thickness despite continuous improvements from large user base
- Example: Best lab mc-Si cell around 20% and typical commercial production between 15 and 17%.

# Conventional c-Si Module Technology

- Manufacturing process driven by front-gridded design of solar cell.
  - Solar cells are “strung” in electrical series with soldered flat Cu ribbon wires (“interconnects”).
  - Cu ribbon is connected from front to rear surface of adjacent cells.
  - Process is serial and difficult to automate due to inherently 3D structure.
- Stress relief between cells limits packing density.
- Non-planar interconnect geometry introduces stress and limits wafer thickness.

# But, conventional PV Module Assembly is slow and labor intense

and strung... and strung... Cells are strung



Cells are manufactured with metal contacts

Each cell is soldered to metal interconnects

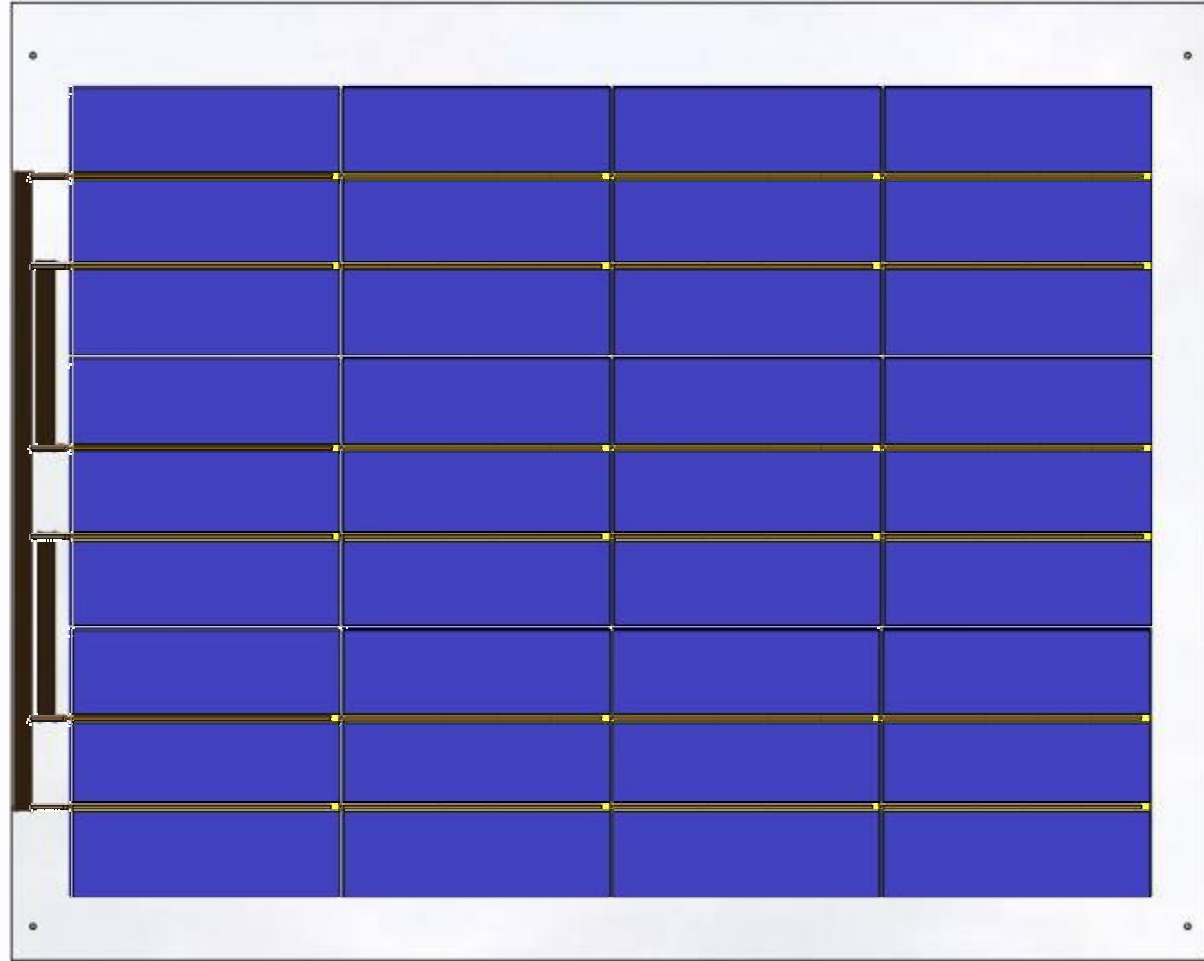
***Slowing gains in cost, quality, and availability***

# Conventional Module Assembly

**Laminate films and glass are prepared to host the strings**

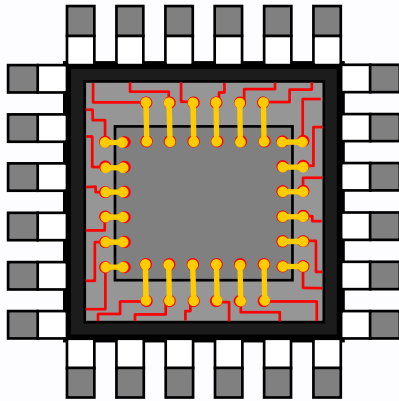
**Strings are placed into laminates**

**And are soldered together**

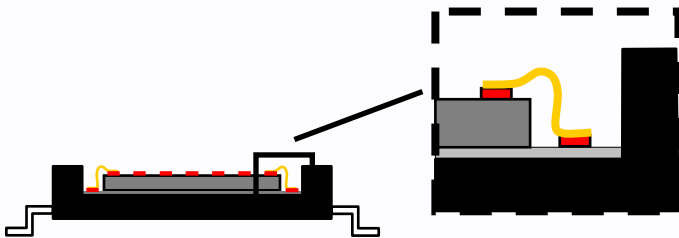


# Semiconductor Assembly Analogy

## Circa 1985

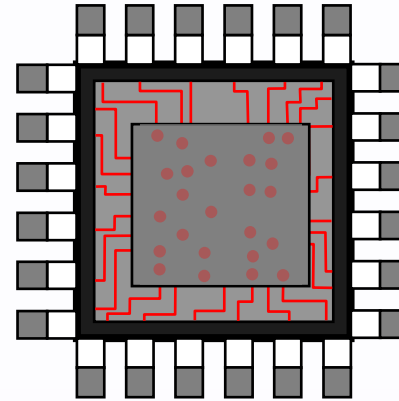


“Wire Bond” – analogous to existing crystalline PV “stringer type” production

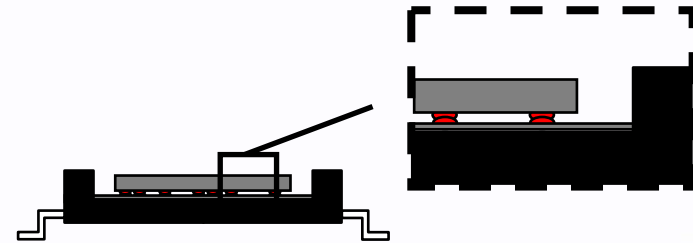


Bond wires: high complex impedance and unstable

## Modern



“C4,” “solder bump,” or “flip-chip” – analogous



Bumps: lower complex impedance and current density. Better thermal dissipation.

# Reduced Losses with Interconnection in Modules

- Conventional c-Si cells suffer electrical power losses of between 2.5 and 3% relative on top of around 3 to 5% optical loss due to the interconnect:
  - Limited Cu ribbon width to minimize optical losses
  - Limited Cu ribbon thickness due to stress
  - Production c-Si PV modules with conventional cells lose around 2% absolute in FF between cells and modules.
- Back-contact c-Si cells do not have same engineering tradeoff – thin Cu foil can be used to minimize stress and electrical resistance.

# Reduced FF Loss in Modules

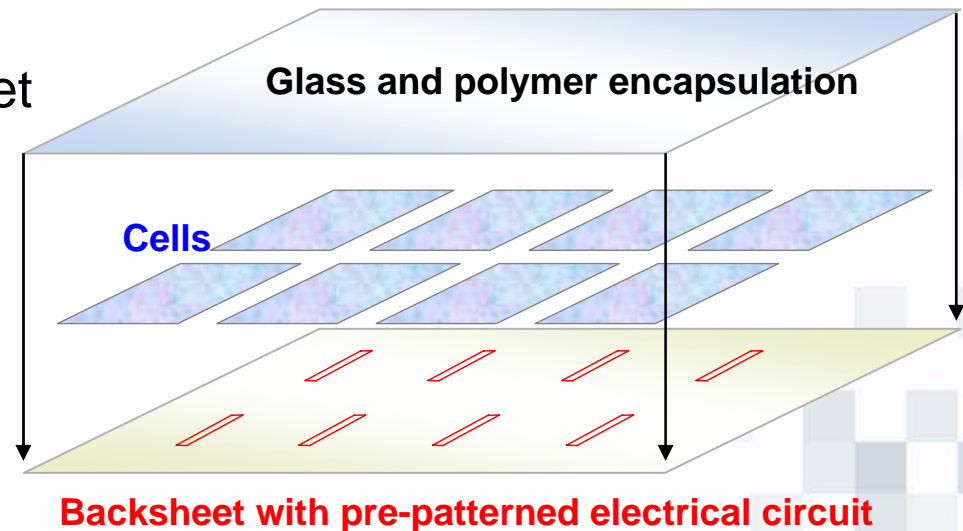
- “H-pattern” refers to conventional Al-BSF c-Si cells.
- “PUM” refers to metallization wrap through (MWT) back-contact cell.
- FF for conventional cells degraded from around 75% to 72% due to interconnection losses.
- ***Back-contact cells had 0.8% absolute higher efficiency in module!***
- Ref: A.W. Weeber, *et al.*, “How to achieve 17% cell efficiencies on large back-contacted mc-Si solar cells,” 4<sup>th</sup> WCPEC (Hawaii 2006).

Table 2: IV characteristics averaged over the groups of neighboring wafers.

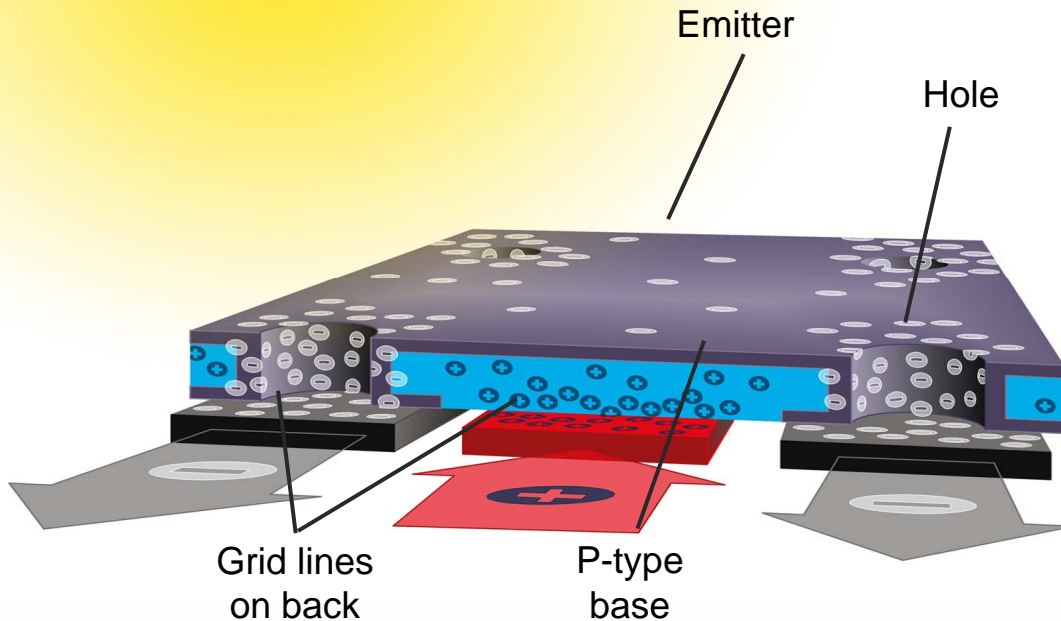
		$J_{sc}$ (mA/cm <sup>2</sup> )	$V_{oc}$ (mV)	FF (%)	$\eta$ (%)
H-pattern	dual-probe	34.2	607	71.8	14.9
H-pattern	dual-probe on tab	34.2	608	75.5	15.7
H-pattern	multi-probe	34.2	607	75.4	15.7
PUM	multi-probe	34.9	612	74.8	16.0
H-pattern	tab 57mΩ/m	34.2	608	72.0	15.0
PUM	foil 29mΩ/m	35.0	612	74.0	15.9
H-pattern	laminated	35.0	609	72.4	15.4
PUM	laminated	35.8	613	73.9	16.2

# Monolithic Module Assembly (MMA)

- Semiconductor industry made huge advances in packaging technology that required changes in the semiconductor chip design.
- MMA single-step assembly of laminate and solar cell circuit eliminates slow stringer/tabber operation.
- Planar geometry works better with thin cells and with cells of arbitrary size.
- Planar processing of backsheet more easily scaled for GW-scale manufacturing volumes.
- Cu foil has lower electrical resistance losses.



# Emitter Wrap-Through (EWT) Cell

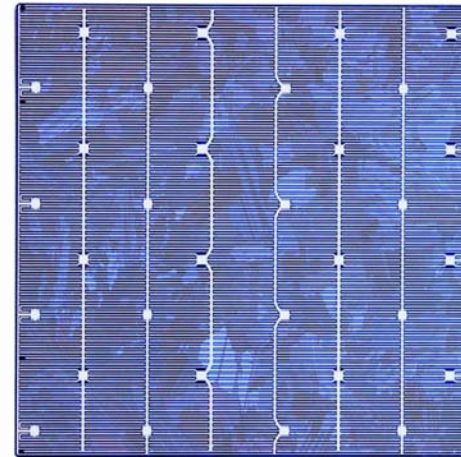


- Electrical grids on the front are eliminated, improving light absorption and aesthetics.
- The laser-drilled holes enable the emitter (in gray) to be formed on the front, in the holes, and on the back surface.

- The electrons are transported by the emitter through the holes to the negative grid.
- Electrons are also created at the emitter on the rear surface, increasing total energy generation.

# EWT

- EWT structure integrates very well with SMT-style assembly.
- Allows for very arbitrary contacting geometries.
- Limit of engineering optimization is that all lateral current flow carried in flexible circuit rather than in expensive solar cell metallization.



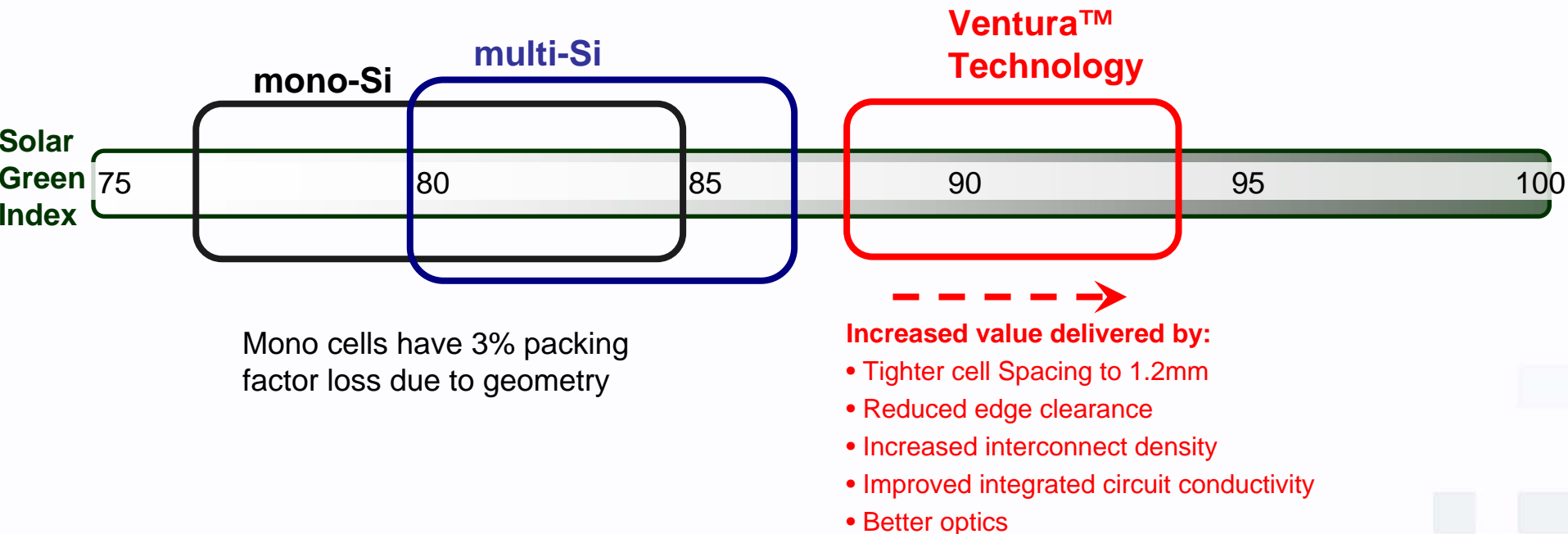
# Solar Green Index

## Introduced by Advent Solar

$$\text{Solar Green Index} = \frac{\text{Module Efficiency}}{\text{Cell Efficiency}} \times \text{Manufacturing Precision Factor}$$

A measure of “goodness” of a Solar Architecture – higher value is better.

# Solar Green Index – Measured Values



Manufacturing Precision Factor not included in above measurements

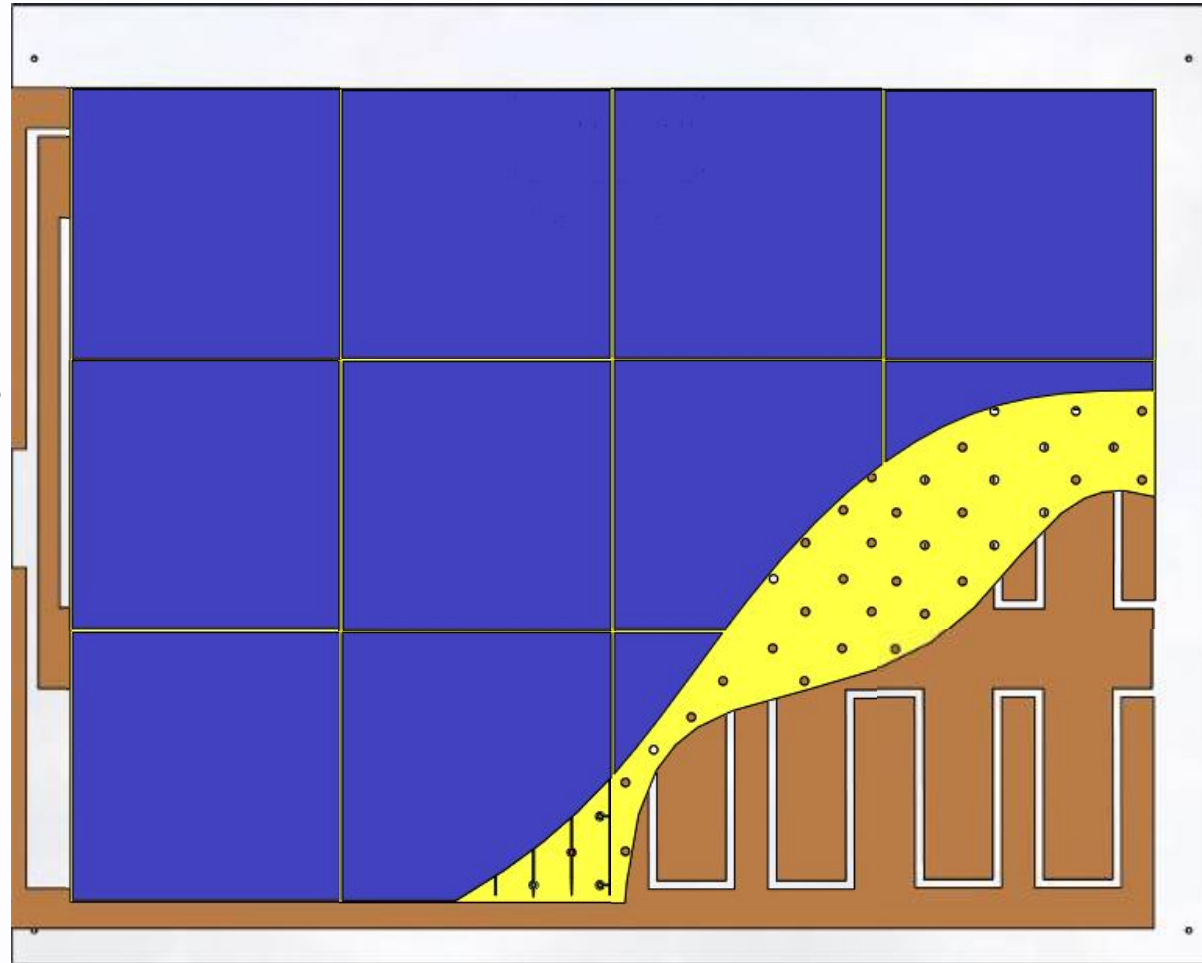
# Announcing Ventura™ Technology from Advent Solar

**Laminate films are  
pre-manufactured  
with a circuit**

**A dielectric layer  
selectively isolates  
contacts**

**Cells are placed  
onto the laminate**

**EWT cells ideal  
for SMT-style  
optimization.**



# Ventura™ Technology

## ■ Better Cells

- Proven emitter wrap-through (EWT) solar cell
- Higher light conversion efficiency due to front grid elimination
- Laser drilling for EWT cell processing means higher energy performance at lower cost

## ■ Better Modules

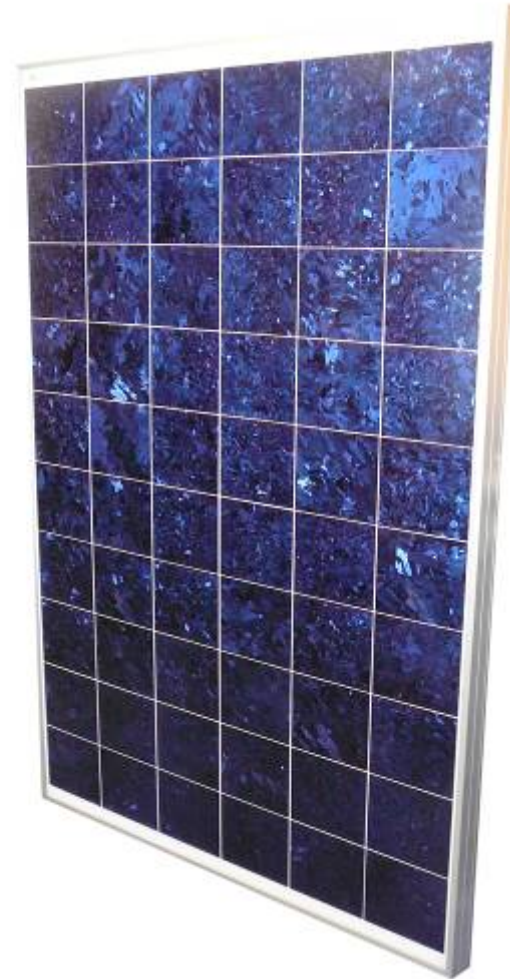
- Precision cell placement and MMA approach minimizes module surface area resulting in better efficiencies and higher value
- Better interconnectivity leading to lower resistive losses
- Thinner wafers because of automated assembly

## ■ Better Manufacturing

- Faster production because of semiconductor style back sheets
- Increased factory capacity and faster production
- Design for automation creates higher yields, less breakage

## ■ Better Aesthetics

*Beautiful by Design™*



***Industry's best blueprint for the leading solar modules***

# Summary

- *Technology Architecture* matters!
  - Improvements in technical performance, cost, and ease of integration for integrated architecture at cell and module level
  - Eliminates efficiency bottlenecks inherent in conventional approaches
  - Architecture is scalable across silicon types and wafer thicknesses

