Wafer bonding for Heterogeneous Integration*

By

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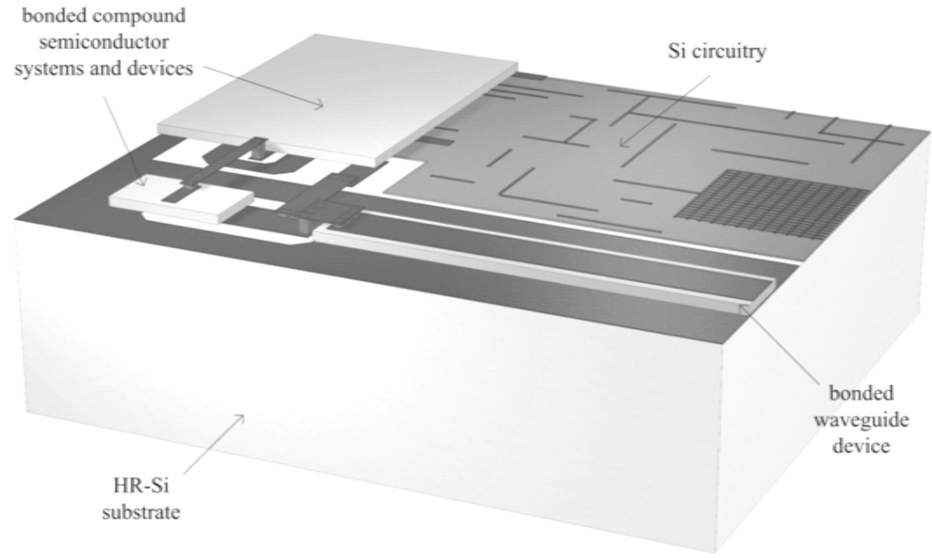
Outline

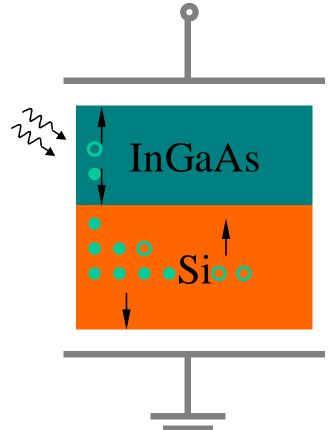
- Motivation for Heterogeneous Integration
- **Types of wafer bonding**
- **Direct bonding**
  - LTS versus HTS
  - Device Results
- **Metal bonding**
  - Bonded HMMIC Capabilities
  - Isothermal Solidification (ITS) Metal bonding
  - Characterization of bonded interfaces
- **Summary**
- **Acknowledgements**

Motivation of Heterogeneous Integration

- Integration of ICs made on different substrates



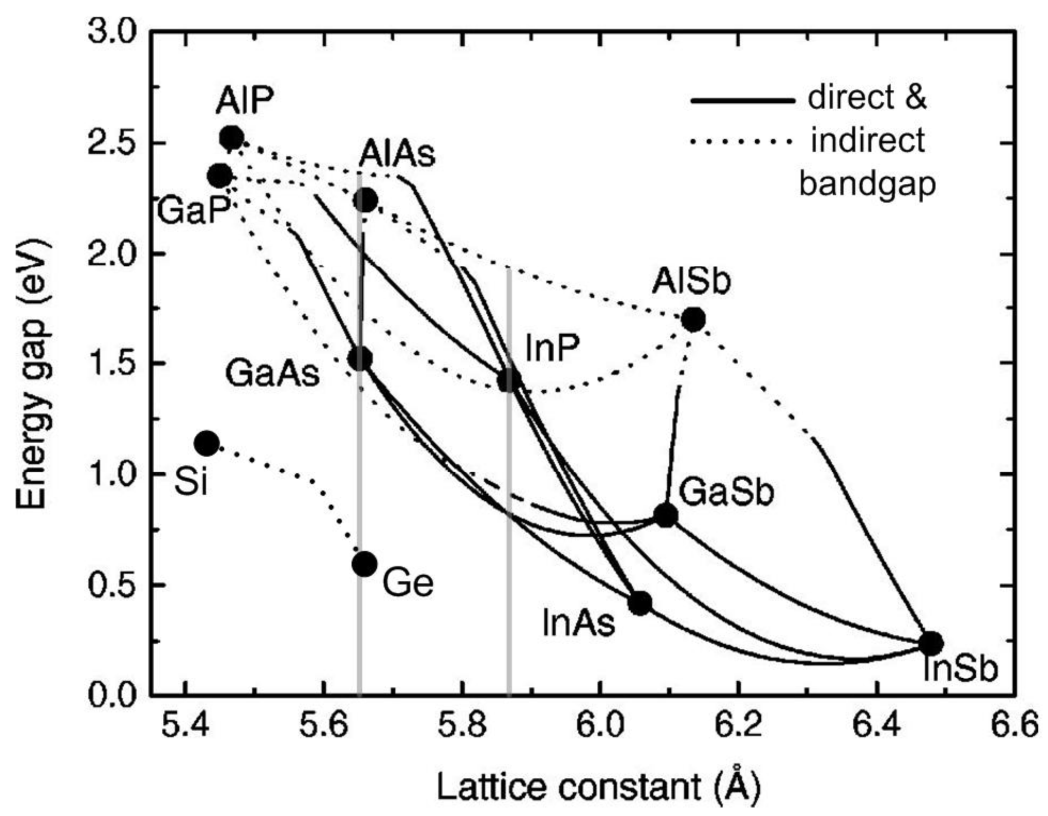
- Photonic devices whose functions rely on two different materials



Wafer fused InGaAs/Si Avalanche Photodiode

Integration Methods

- **Growth (III-V on Si)**
  - Well established
  - Restricted by lattice mismatch
  - Not compatible with Si presently
- **Wafer Bonding**
  - Freedom to integrate compound semiconductors with Si
  - Limited by thermal stress

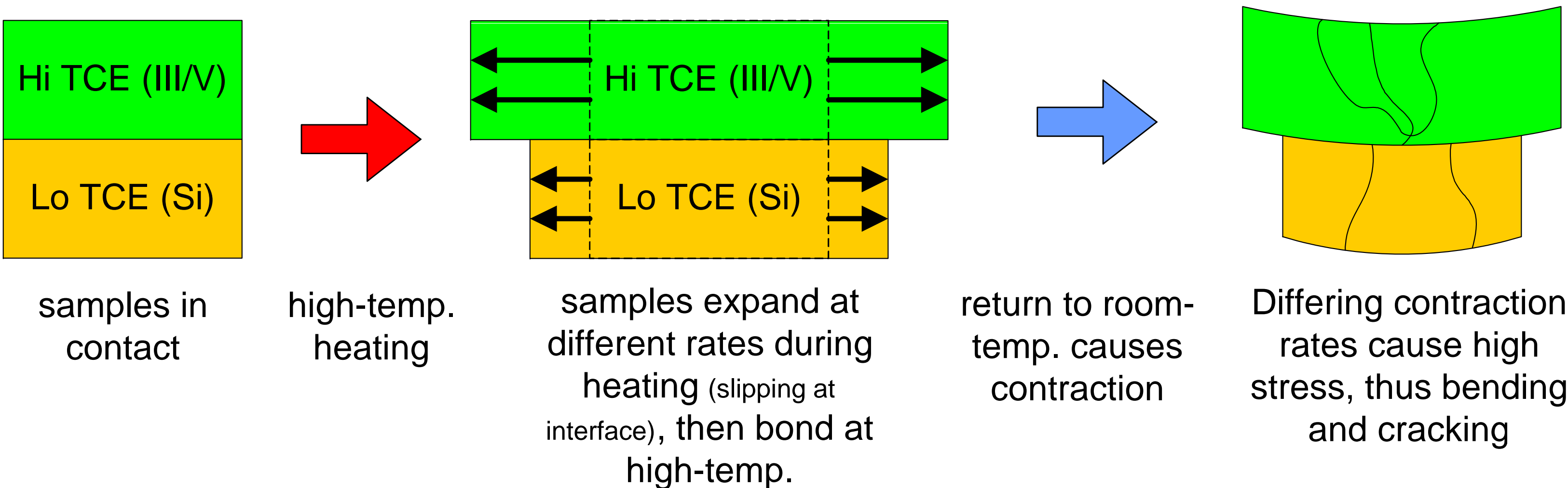


General Integration Issues

- Large difference in lattice constant between III/V and Si (strain ~5-20%):

  traditional epitaxial growth always produces highly stressed material due to large strain:

- Difference in Thermal Coefficient of Expansion:



- Device fabrication chemistry is generally incompatible.

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Types of Bonding

- **Direct bonding** (no interface material)
  - High thermal stress
  - Heterojunction electrical interface → peripheral interconnect
  - Good thermal conduction across the interface
  - Not particle compliant (i.e. it is sensitive to tiny bumps)
- **Insulator bonding** (oxide, nitride, adhesive interface material)
  - Potentially low thermal stress
  - Insulating electrical interface → peripheral interconnect
  - Poor thermal conduction
  - Particle compliant
- **Metal bonding** (metal interface material)
  - Potentially low thermal stress
  - Potential ohmic electrical interface → embedded interconnect
  - Potentially high thermal conduction
  - Particle compliant

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Example of Direct Bonding: Fused InGaAs/Si APD

Motivation: •**Operate in the 1.0-1.6μm wavelength range**.

-- InGaAs has the high absorption coefficient in the wavelength region for fiber-optics, and is lattice-matched to InP.

- **Low-noise multiplication in Si**

-- Si has the largest difference in the impact ionization coefficients for electrons and holes.

- **Low band-to-band tunneling dark current in high E-field region**

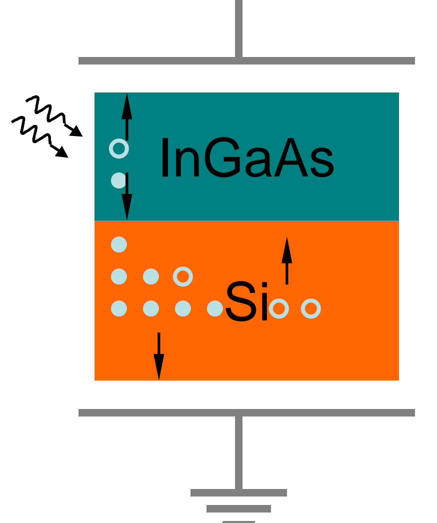
-- Wide, indirect bandgap structure of Si.

- **Potential high frequency operation**

-- Ordered electron initiated multiplication process.

- **High thermal stability**

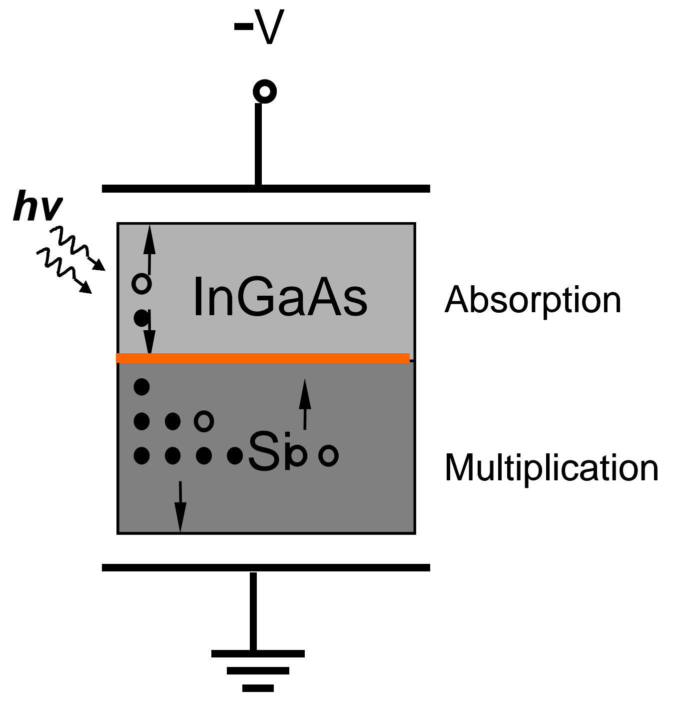
-- Impact ionization coefficients of Si less thermal sensitive.



Challenge: Lattice/TCE mismatch between Si and III/V:

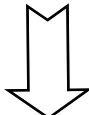
Properties	Si	InGaAs	Mismatch
Lattice structure	Diamond	Zinc blende	-
Lattice constant (Å)	5.4309	5.8694	8%
Thermal expansion coefficient (10^{-6} °C^{-1})	2.6	5.6	113%
Thermal conductivity (W/cm °C)	1.5	0.7	56%

Wafer Fusion Interface Requirements



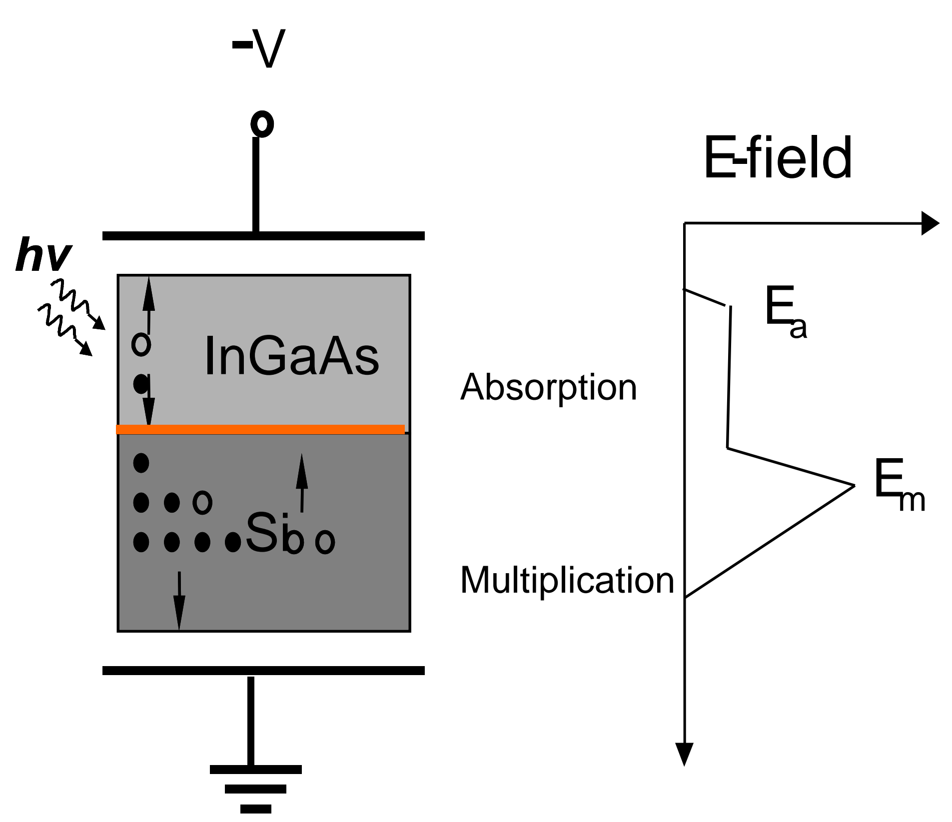
Wafer Fused InGaAs/Si APD

The InGaAs/Si interface is right in the middle of the APD!



- No interaction between the interface and carriers passing through the interface.
- The electric field distribution should not be affected by the interface.
- The dark current generated by the generation-recombination centers at the interface should be negligible.

Wafer Fused InGaAs/Si APD design



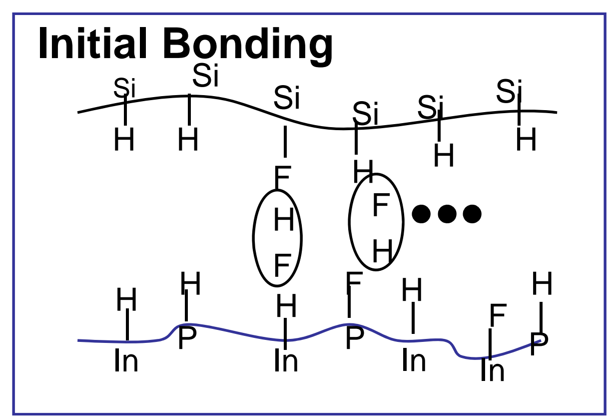
Separate Absorption Multiplication Structure

p-InP/i-InGaAs/p-Si /n-Si

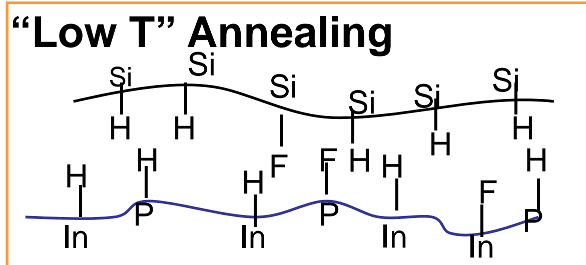
Assumption: The fused interface has negligible impact on the E-field profile.

1. $E_a > 4 \times 10^3$ V/cm
   Ensure carriers drifting at saturation velocity in InGaAs
2. $E_a < 1.5 \times 10^5$ V/cm
   Suppress tunneling current in InGaAs to a negligible level
3. $E_m > 4.5 \times 10^5$ V/cm
   Ensure the occurrence of carrier multiplication in Si
4. $E_m < 7 \times 10^5$ V/cm
   Suppress tunneling current in Si to a negligible level
5. Low dark current ➔ good interface
   Achieve high sensitivity

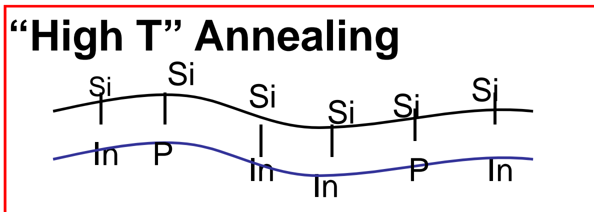
III/V – Si Wafer Fusion



- Initial bonding: Van der Waal bonding- electronic dipole attraction, reversible

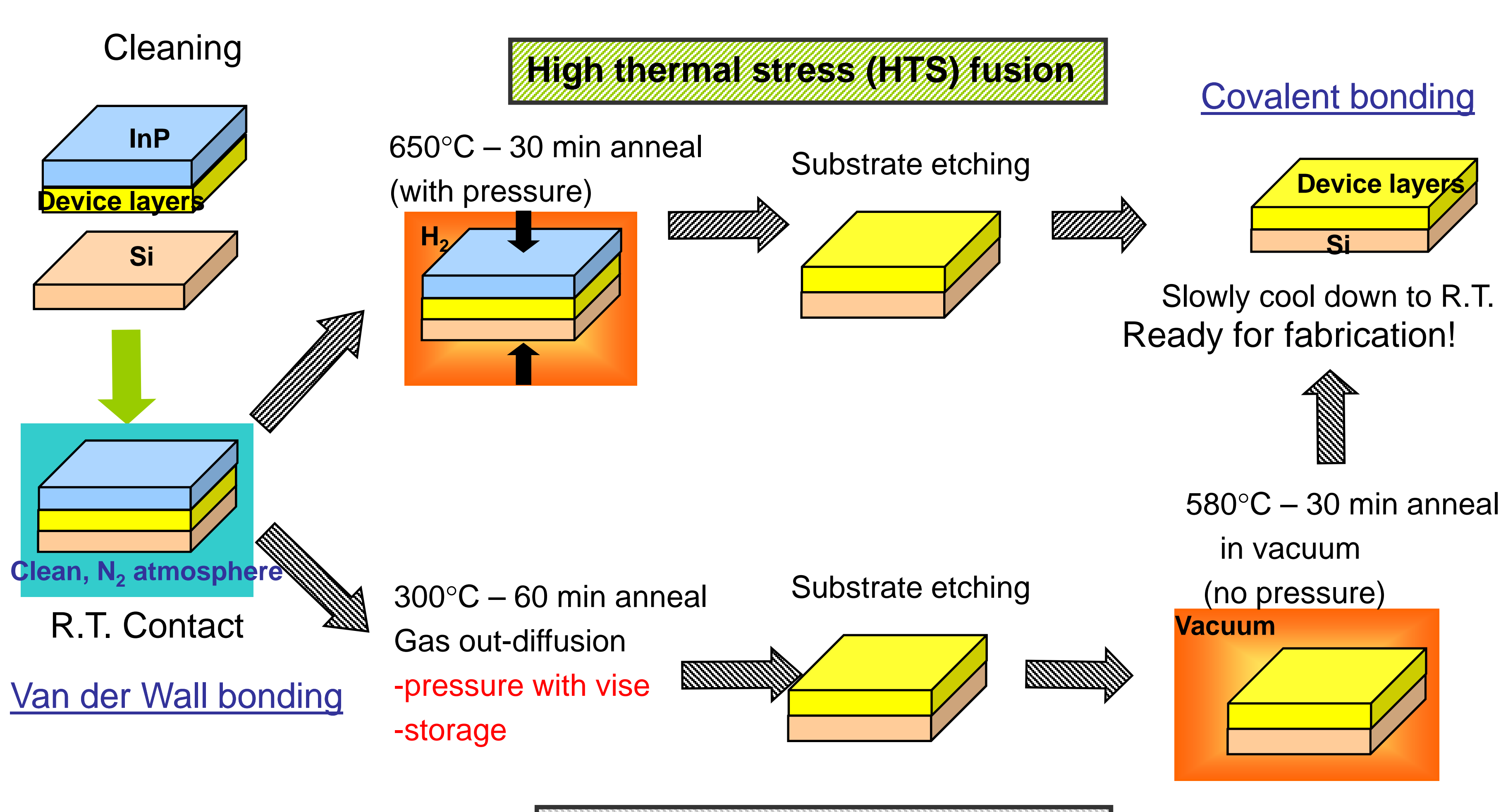


- Release physically attached solvent molecules.
- ~350°C begin Group V Evaporation
- Freed Group III atoms are mobile

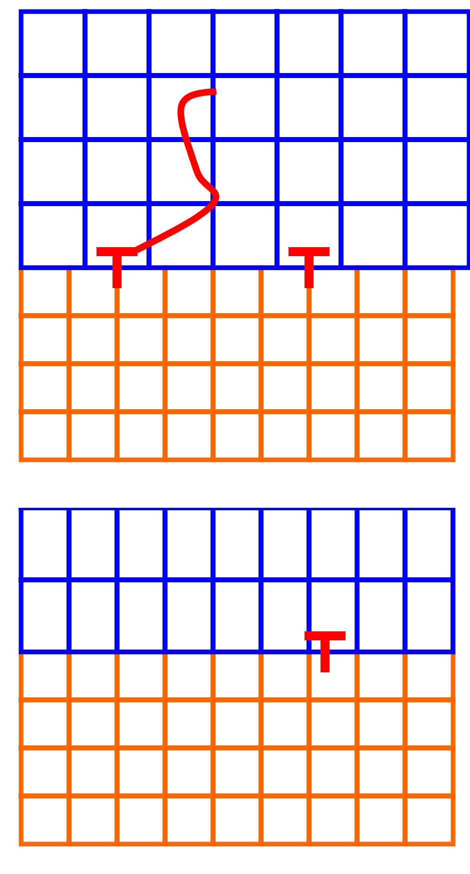


- Covalent bonding: shared electrons, permanent.

Direct Bonding/Wafer Fusion Processes



HTS vs. LTS



- **HTS**

  Both Si and III/V are too thick to have elastic deformation. When the thermal shear stress larger than a certain level, dislocations form.

  Dangling bonds sheet density is on the order of 6.5 x 10^{12}cm^{-2}

- **LTS**

  The III/V film is thin enough to have elastic strain to accommodate thermal stress. Therefore, LTS samples have low dislocation density.

InP/InGaAs Si Edge dislocation

The good, the bad, and the ugly…

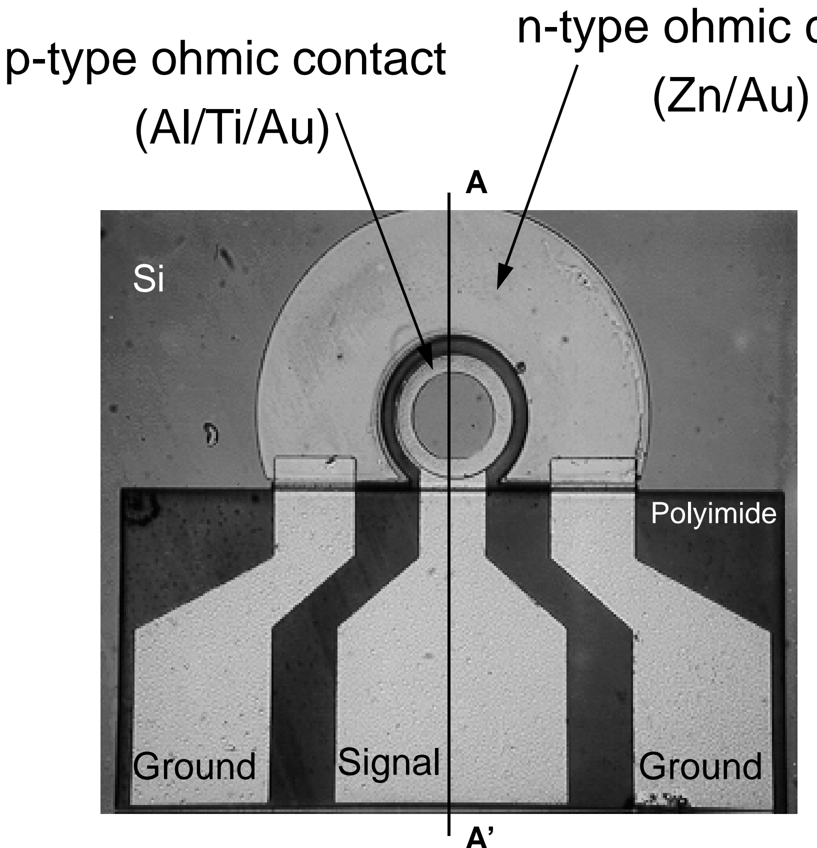
- Stress lines shown on **HTS** samples.
- Difficult to apply large pressure evenly.

- Gas trapped at the interface forms bubbles on the **LTS**(w/o any low temperature anneal) samples.

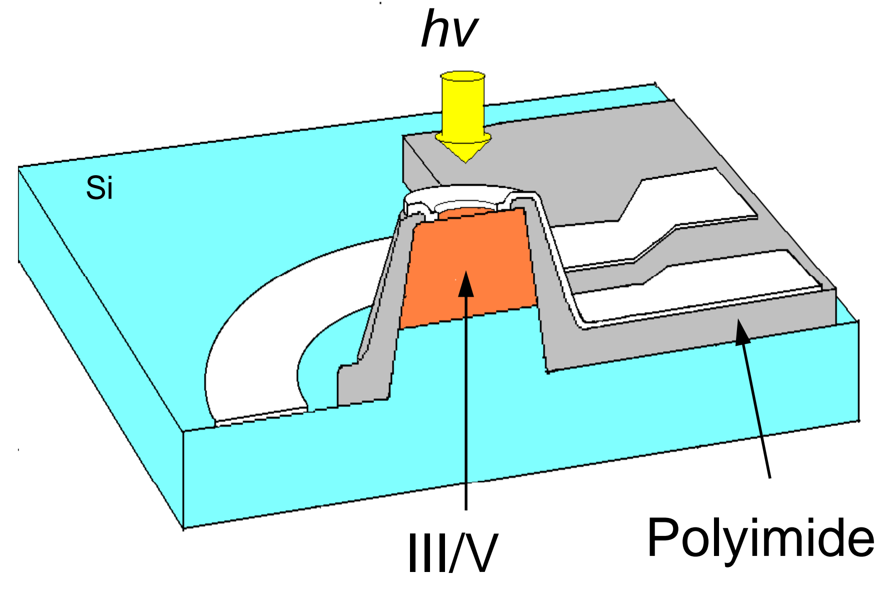
- Ultrasonic bath in *TCE* is a very efficient method to destroy unbonded area.

- **LTS** sample (with low temperature anneal) has high yield.
- High reproducibility.
- Physically robust bonding.

Top View & Cross Section views of Photodiode

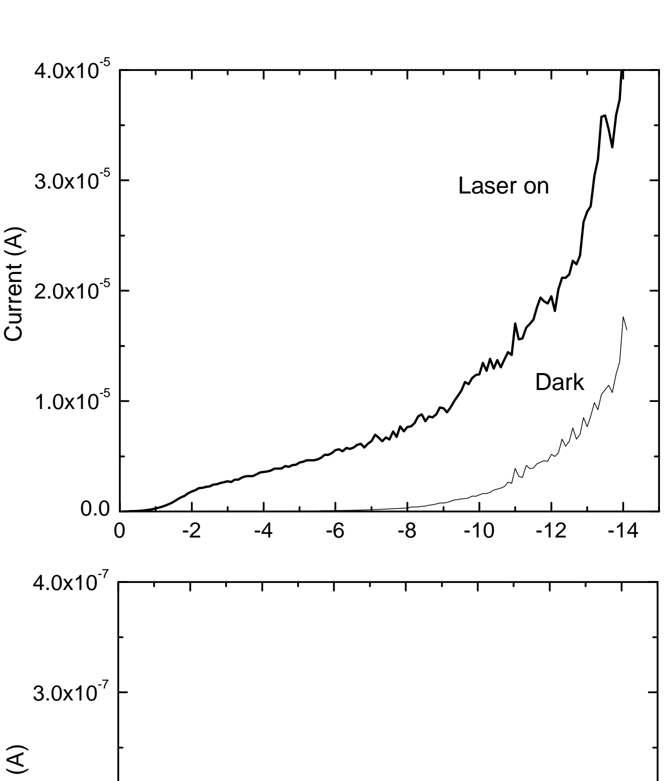


Cross Section along A-A'



- 130μm diameter mesa
- top illumination

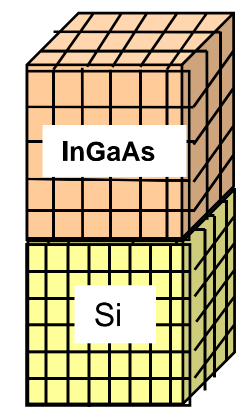
HTS Fused InGaAs/Si p-i-n PD

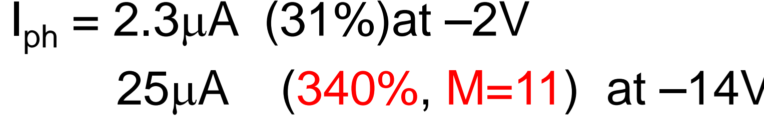


Measurement Conditions:

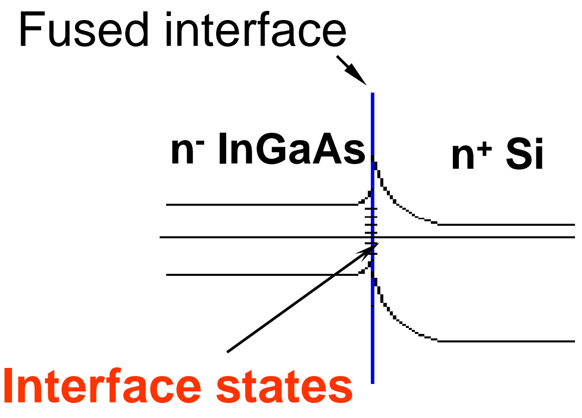
Optical power=7μW

Wavelength=1.32 μm





Fused interface



- Dangling bonds
- Impurities at the interface
- Coulomb potential of charged ions at the interface

Passivation of PIN photodiode

Pre-passivation: $(NH_4)_2S$ solution rinse to prevent

(1) further oxidation after chemical etching of III/V [1]

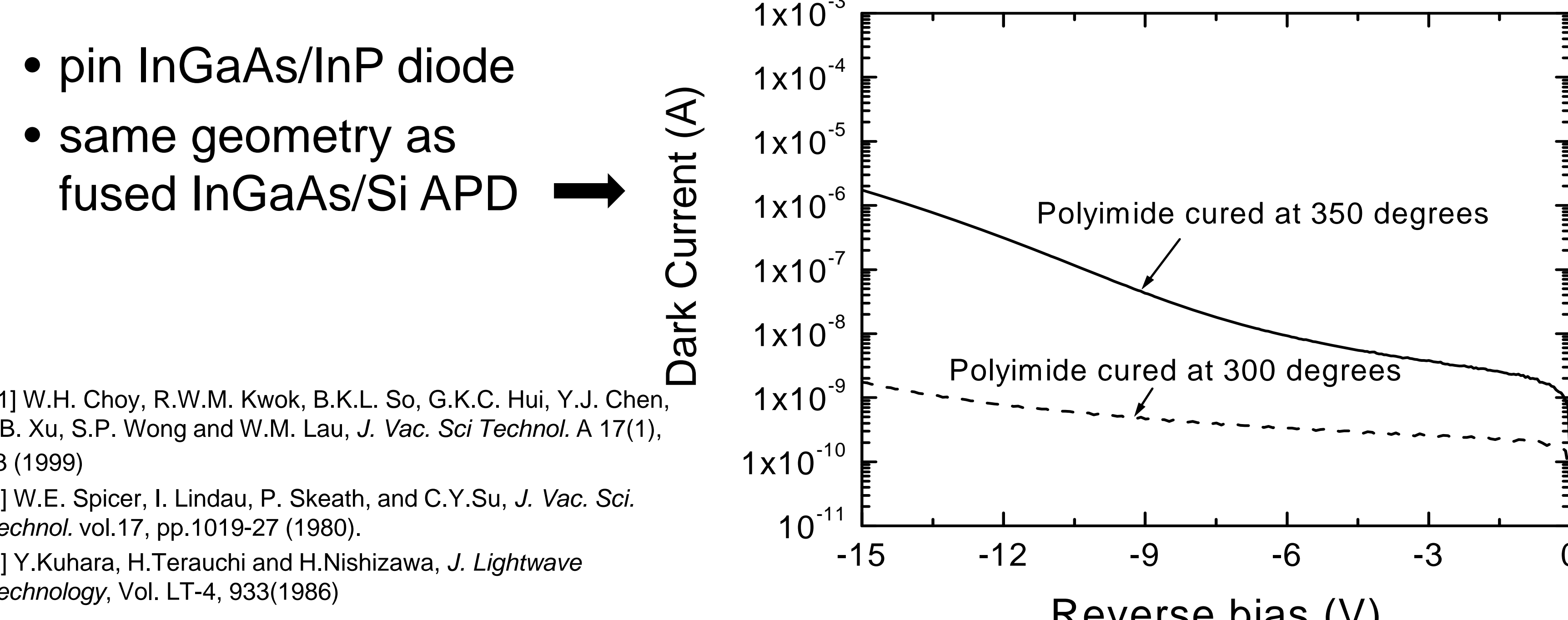
(2) loss of group V during annealing [2].

Passivate the mesa sidewall with low-temperature-cured polyimide [3] to:

(1) isolate mesa sidewall from the ambient

(2) prevent the accumulation and diffusion of mobile ions towards the junction perimeter occurring in a high temperature cure process.

- pin InGaAs/InP diode
- same geometry as fused InGaAs/Si APD ➡



*[1] W.H. Choy, R.W.M. Kwok, B.K.L. So, G.K.C. Hui, Y.J. Chen, J.B. Xu, S.P. Wong and W.M. Lau, *J. Vac. Sci Technol.* A 17(1), 93 (1999)

[2] W.E. Spicer, I. Lindau, P. Skeath, and C.Y.Su, *J. Vac. Sci. Technol.* vol.17, pp.1019-27 (1980).

[3] Y.Kuhara, H.Terauchi and H.Nishizawa, *J. Lightwave Technology*, Vol. LT-4, 933(1986)

LTS Fused InGaAs/Si APD

- Dark Current:

  0.7nA @ M=1

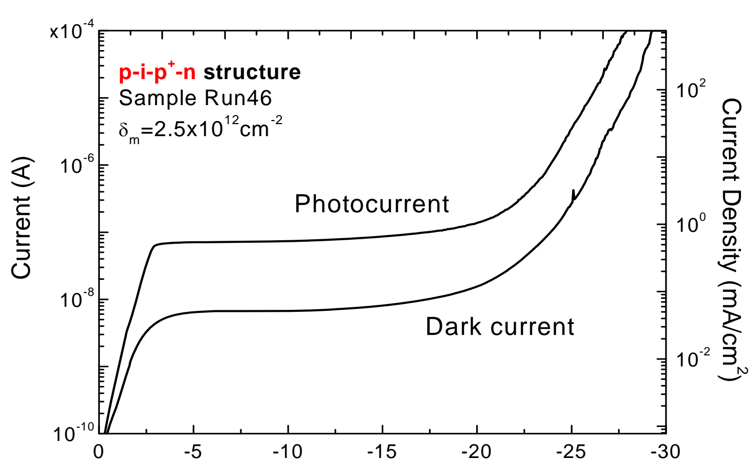
  50nA @ M=10

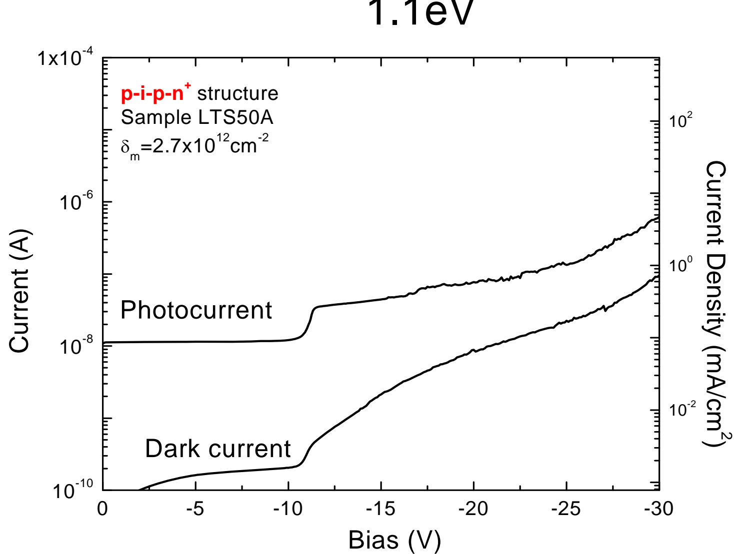
- Photoresponsivity:

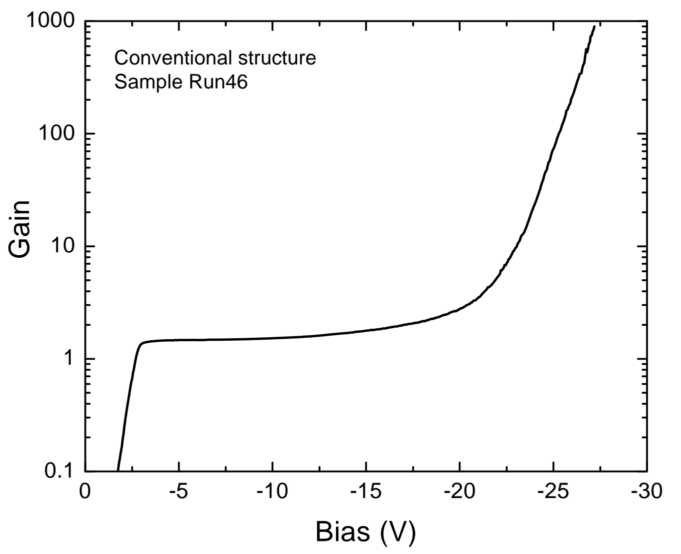
  0.64A/W (60%) @ 1.31 μm

- Forward turn-on voltage:

  1.1eV







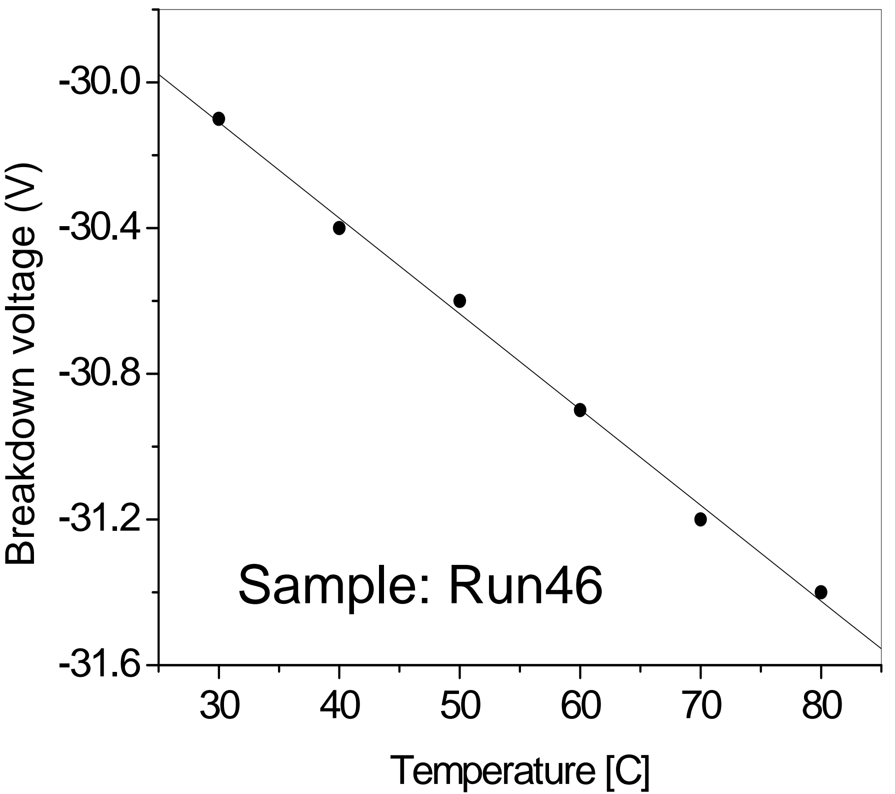
Breakdown Voltage, V_b, vs. Temperature

Thermal coefficient of V_{br}:

$$\delta=(\Delta V_{br}/V_{br})/\Delta T$$

$\delta_{InGaAs/Si} = 0.09\%/°C$

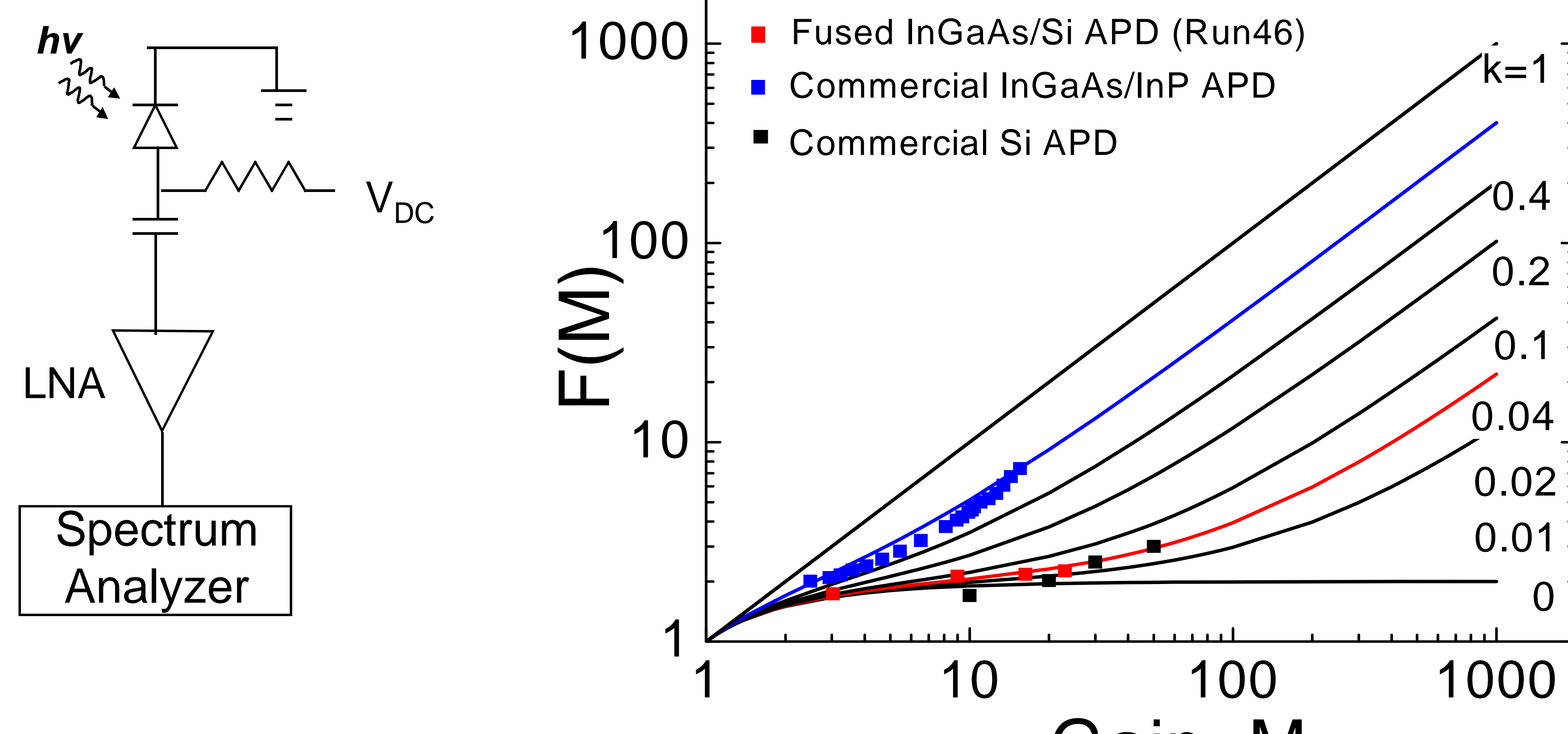
$\sim 0.5\ \delta_{InGaAs/InP}$



Fused InGaAs/Si APDs have better thermal stability than InGaAs/InP APDs.

	Dark Current Density (mA/cm^2)	
	@V_b=-5V	@ Gain, M=10
LTS APD	0.04	0.6
HTS APD	15	2000
COTS APD	-	0.03

LTS Fused InGaAs/Si APD F(M)



Summary

- Direct bonding through wafer fusion has been experimentally studied.
- The InGaAs/Si photodiodes made by HTS have high dark current.
- The LTS fusion is capable of large diameter wafer bonding. With proper sidewall preparation and passivation, it gives rise to low dark current InGaAs/Si APDs.
- The LTS is still very sensitive to the surface roughness and contamination.

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Heterogeneous MMIC

- **How can HMMIC improve upon traditional MMIC designs?**

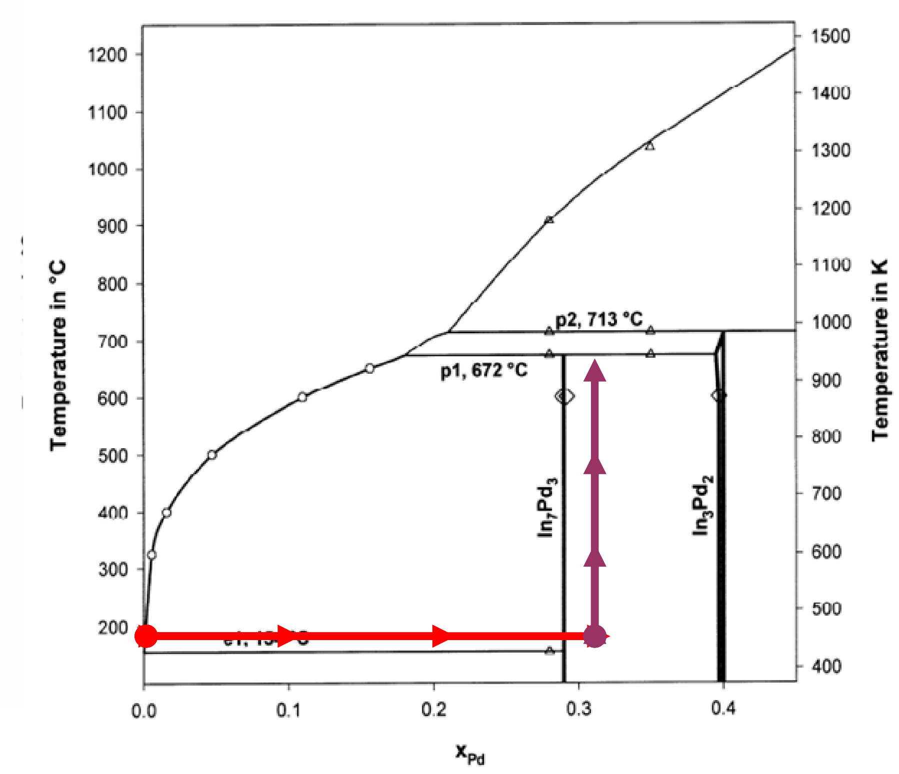
By combining…

- Microwave advantages of compound semiconductors
  - High electron mobility → speed, power
  - Bandgap engineering → heterojunction devices
- Proven CMOS and Bipolar architecture of silicon
  - Provide digital interface and control circuitry → functionality
  - Peripheral components relegated to HR-Si → cost

…to improve mixed RF/digital communications systems

- Functionality
- Speed
- Power
- Size
- Cost

Isothermal Solidification Metalbonding Technique



- **Advantages:**
  - Low bonding temperature reduces thermal stress
  - Transitory liquid state envelopes particles
  - Final solid state allows high temperature processing

- **Disadvantages:**
  - Only works with alloys that have stable peritectic intermetallic compounds
  - Other alloy reactions must not compete

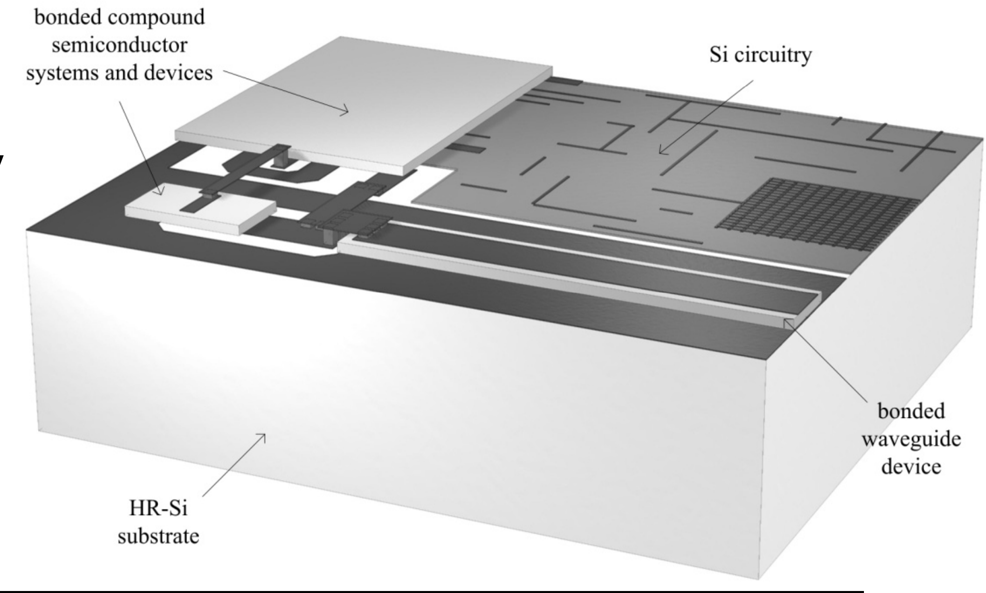
Goals of ITS approach

- Robust Heterogeneous Integration Technique
  - Bottom-up and top-down approaches
  - Case study of GaAs-Si system
    - large thermal mismatch

- Benefits and Capability of HMMIC
  - Benefits of HMMIC
  - Characterize essential bond interface properties
    - Electrical
    - Thermal
    - Microwave

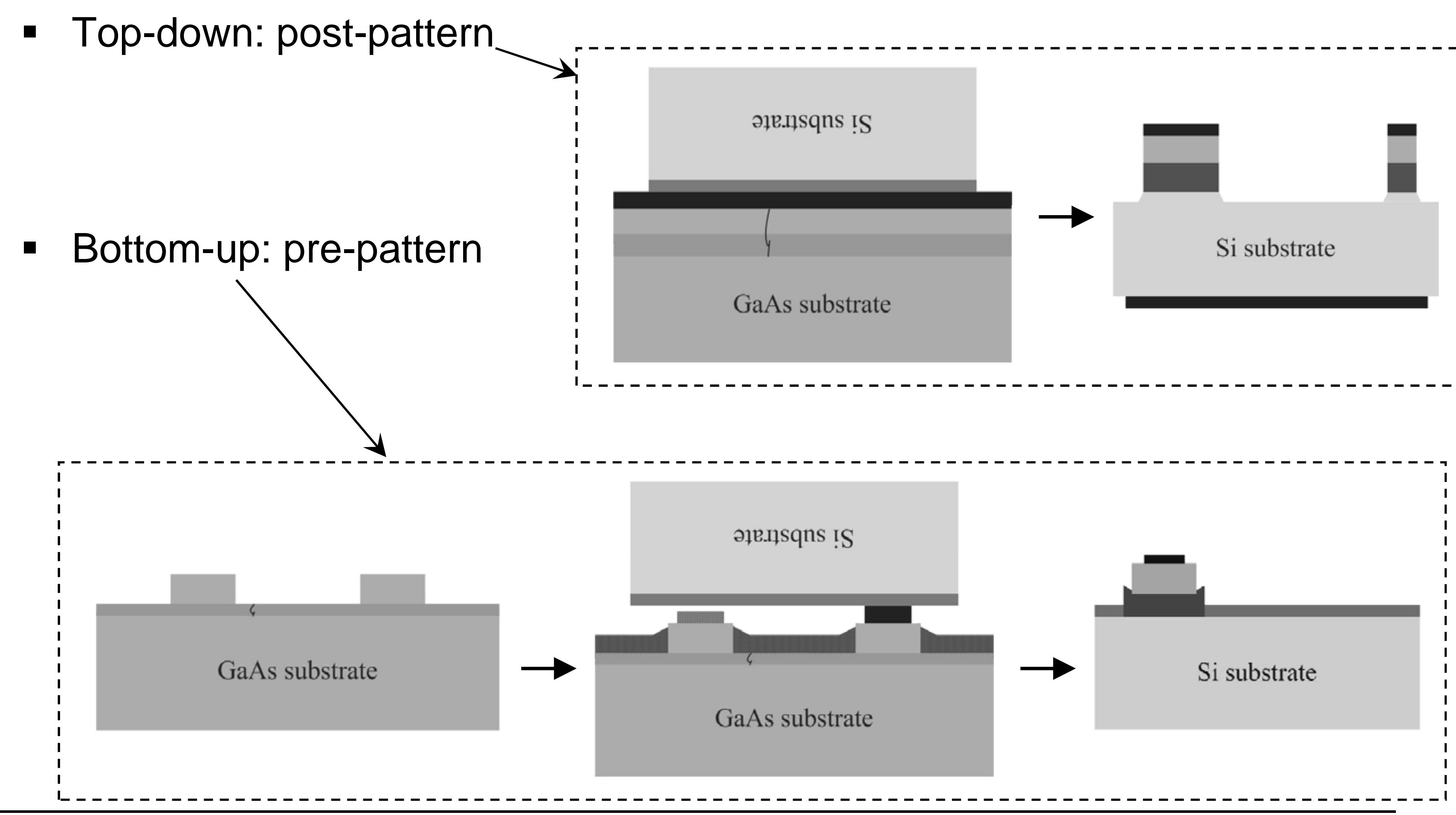
Benefits of Metalbonded HMMIC

- **Separate Substrates**
  - Heterogeneous integration widens functionality
  - Individually engineered for optimal yield or performance
  - Allows testing prior to integration
- **Si Architecture**
  - Si substrate improves device heat dissipation
  - Si provides digital interface
  - Microwave peripherals placed on Si substrate
    - HR-Si for low loss
- **Novel device assembly**
  - Top-side and bond-side connectivity
    - Bonded-microstrip
    - Traveling wave devices
  - Multiple bond-side contacts
    - Single transistors
    - Subsystems



Metalbonding Implementations

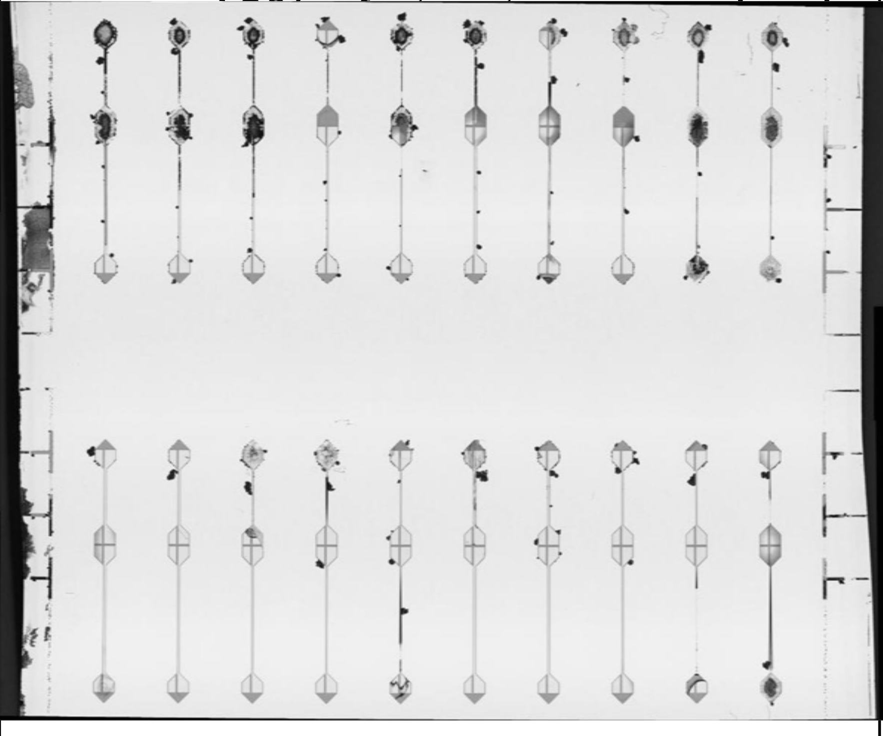
- **Two forms**
  - Top-down: post-pattern
  - Bottom-up: pre-pattern



Metalbonding Results

Post-pattern Method:

Yield



Pre-pattern Method:

Yield

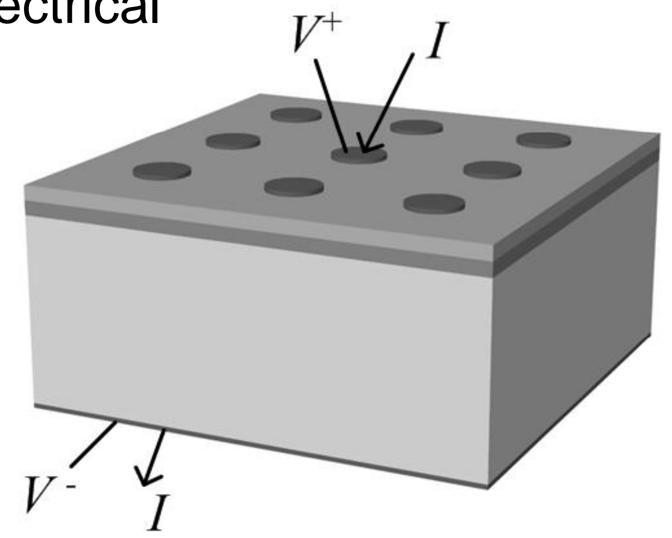
- ~15% of structures survived fully intact, ~60% of survived about 80-90% intact
  - Fewer particles
  - Less vulnerable to etching
  - Higher stress density

Conclusions

- Provide truly intimate integration
  - Selective bonding
  - Back-end process

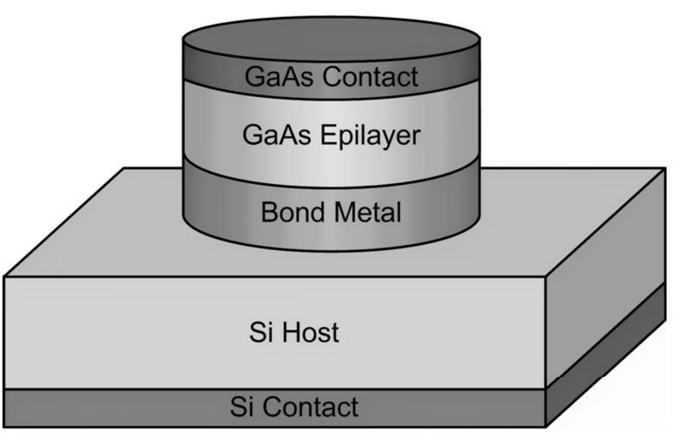
Electrical Interface Measurements

- In-Pd system chosen for GaAs & Si electrical contact properties
- Characterize
  - Electrical behavior
    - Linear (ohmic)
    - Non-linear (not ohmic)
  - Contact resistivity
    - Cox & Strack variation
- Used post-pattern bonding process



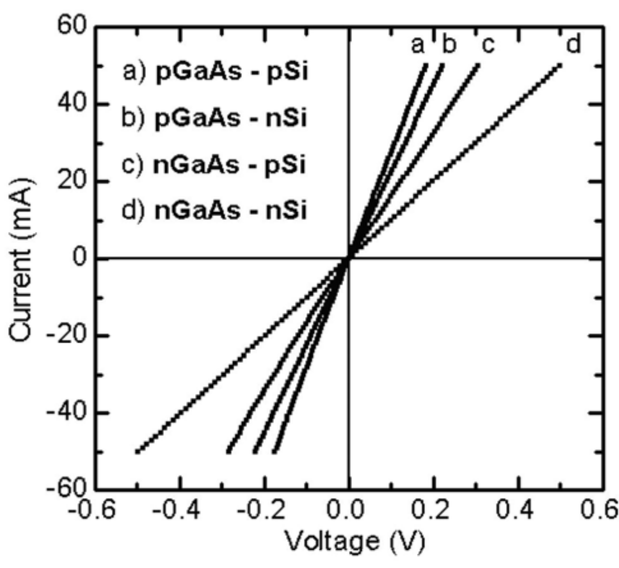
$$R_{total} = R_{ctop} + R_{epi} + R_{cbond} + R_{spread} + R_{cbottom}$$

$$R_{residual} = \frac{\rho_{cbond}}{A} + \text{const}$$

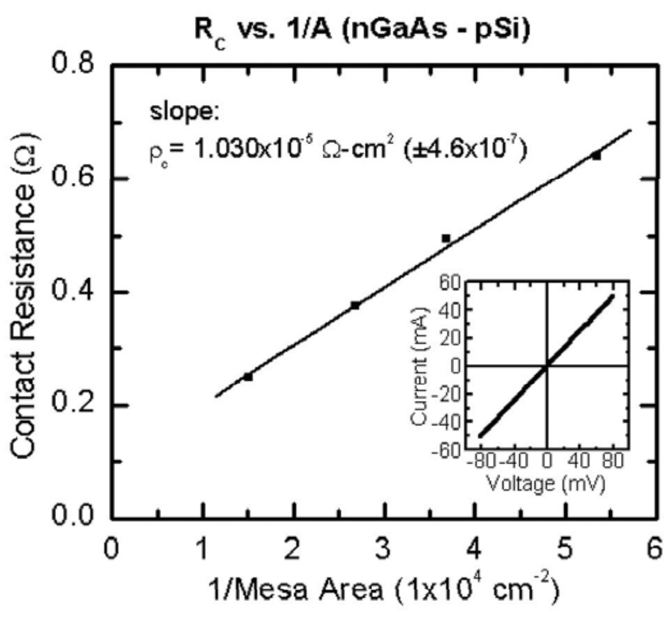


Electrical Characterization Results

Electrical behavior



Contact resistivity



$$R_{residual} = \frac{\rho_{cbond}}{A} + \text{const}$$

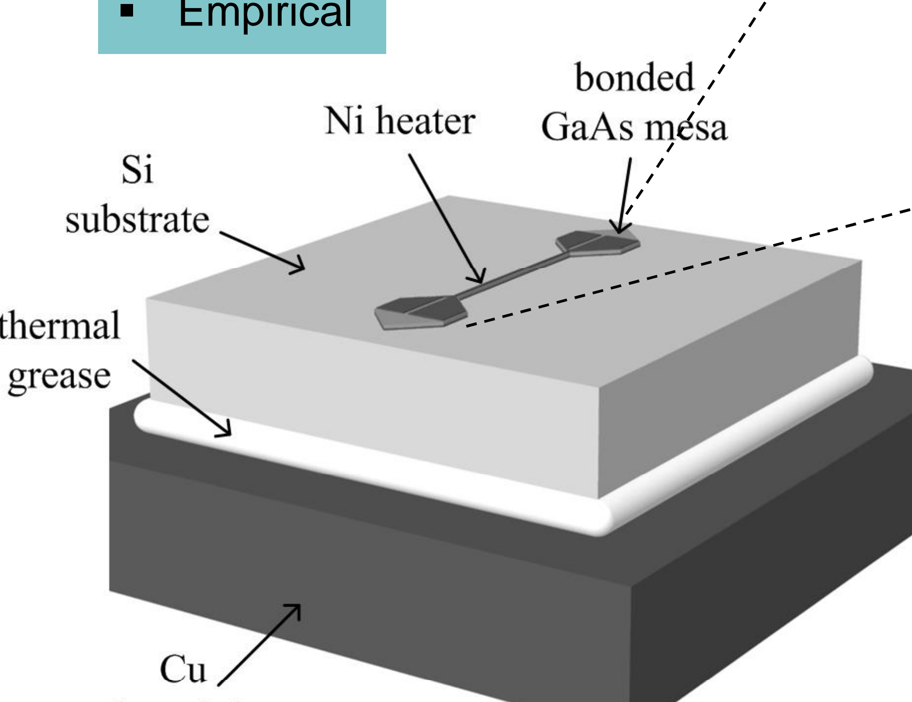
- Universal ohmic behavior between GaAs & Si
- Bond interface resistivity measurement of n-GaAs / p-Si
  - Estimation of remaining combinations
- Further improvement
  - Taylor doping to lower contact resistivity

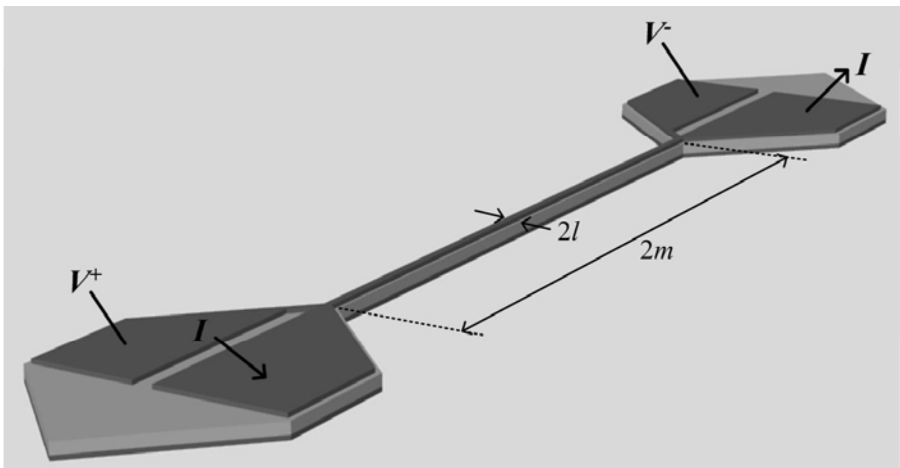
Doping Combination	Contact Resistivity (ohm-cm^2)
p-GaAs / p-Si	(8.49×10^{-6})
p-GaAs / n-Si	(9.08×10^{-6})
n-GaAs / p-Si	1.03×10^{-5}
n-GaAs / n-Si	(1.37×10^{-5})

Thermal Measurement

Steady-state hot-strip method:

- Characterize bondmetal κ
- Used pre-pattern bonding process
- Modeling
  - Theoretical
  - Empirical





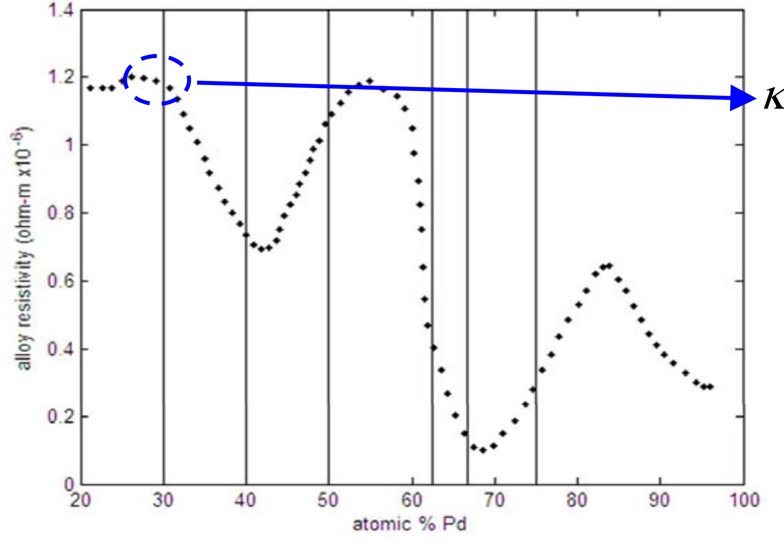
$$R_{total} = R_{mesa} + R_{bond} + R_{spread}$$

$$R_{spread} = a \ln(l) + b$$

Thermal Characterization Results

Bond Material	Thermal Conductivity (W/m-K)	Comparison to In_7Pd_3
polyimide	0.22	11.4x
SiO_2	1.26	2.1x
In_7Pd_3 bondmetal	**2.51**	**1x**
$Pb_{63}Sn_{37}$ solder	55	1/21.9x
Sn	66.6	1/26.5x
Pd	71.8	1/28.6x
In	81.6	1/32.5x

- Lower than initially expected κ_{bond}
  - Too many variables to analytically solve
  - Wiedemann-Franz law estimate
- Better overall heat transfer than un-bonded GaAs
- Further improvement
  - Higher κ substrate material
  - Higher conductivity bond alloy
    - Metallurgy
    - Different alloy
  - Thinner bondmetal



$$\kappa_e = \frac{L}{\sigma T} \rightarrow$$ 6.71 W/m-K

Material	Thermal Conductivity (W/m-K)
Si (CZ)	148
GaAs	48

$$R_{total} = R_{mesa} + R_{bond} + R_{spread}$$

~2x improvement in heat transfer over natural GaAs substrate

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Results Summary

- Pre-pattern ITS metalbonding process sparsely bonded GaAs devices to silicon
  - Selective integration
  - Back-end process
- Universal ohmic behavior with an interface resistivity of 8.49×10^{-6}-1.37×10^{-5} ohm-cm^2
  - Adequately efficient interconnection
- Bondmetal thermal conductivity of 2.51 W/m-K
  - Improvement in heat transfer over natural GaAs substrate
  - Outperformed nearest insulating bond material
  - Fell short of expectation
- Supports microwave propagation
  - Bondmetal alloy resistivity correlated to CPW loss
  - Bonded-microstrip properties

Conclusion

Direct bonding through wafer fusion has the advantage of good thermal contact, however, the lattice mismatch and TCE mismatch necessitate low temperature chemical bonding which is difficult to realize:

•The HTS fusion, due to high stress from both sides, creates a highly defective layer near the interface,

•The LTS fusion, due to its two step process, is becoming more practical.

ITS metal bonding method sparsely integrated GaAs with silicon, is better suited with the bottom-up approach. The electrical, thermal and microwave properties of the Pd/In/Pd bond are encouraging; this low temperature bonding approach can be useful for manufacture of metal bonded HMMIC

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