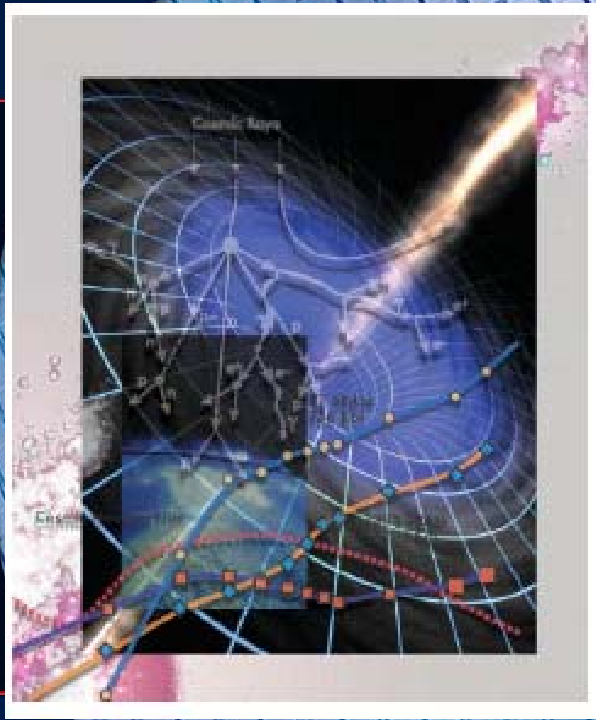
# Soft Errors – No Way To Escape



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**Technology R&D**
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# TOPICS

- DEFINITIONS
- SOURCES OF RADIATION
- MITIGATION TECHNIQUES
  - SEL AND MBU MITIGATION
- MEASUREMENT TECHNIQUES
- MODELING/SIMULATION OF SER
- CYPRESS DATA
- CONCLUSIONS

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- **DEFINITIONS**
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# DEFINITIONS-1

- Soft Error (SE)

  A change of state or transient in a device induced by an energetic particle such as a cosmic ray or alpha particle. These are "soft" errors in that a reset or rewriting of the device causes normal device behavior thereafter**.**

- Single Event Upset (SEU), Single Bit Upset (SBU)

  Event caused by a single particle. The error is “soft” because the circuit itself is not permanently damaged and behaves normally after the data state has been restored. If only one memory cell is affected, this is a SBU (Single Bit Upset)

- Multiple Bit Upset (MBU)

  An event induced by a single energetic particle that causes multiple upsets or transients during its path through a device or system. A logical MBU is an event that causes two or more bits in the same logical word to fail (thus not correctable with single-bit ECC).

- Soft Error Rate (SER)

  The rate that soft errors are occurring, usually quoted in FIT/Mb.

- Accelerated Soft Error Rate (ASER)

  SER obtained under accelerated conditions, using high activity radioactive sources or high energy particle accelerators.

- System Soft Error Rate (SSER)

  SER obtained under normal operating conditions. Typically hundreds of devices are operated for hundreds of hours, monitoring the data for errors.

# DEFINITIONS-2

- Failure In Time (1 FIT = 1 error in $10^9$ device-hours), Examples:
  - Cell Phone with **4Mb** of SRAM with **1,000FIT/Mb**
    SER = 4,000 errors per $10^9$ power-on hours
    You must reset your phone every … **28 years**
  - Laptop with **512MB** of DRAM with **4,000FIT/Mb** (traveling at 35,000 feet)
    SER = 1 error every **62 hours**
    To be safe, save your data every … 5 hours
  - Internet router with **100Gb** of SRAM with **100FIT/Mb**
    SER = 1 error every … **4 days**
    Unacceptable; must use ECC to detect and correct errors
- Single Event Latchup (SEL)

  A condition which causes loss of device functionality due to a single event induced high current state. An SEL may or may not cause permanent device damage, but requires power strobing of the device to resume normal device operations.
- Single Event Effects (SEE)

  Any measurable effect to a circuit due to a particle strike. This includes (but is not limited to) SEUs, SEL, MBUs, SEFI, SET etc.

# FAILURE RATE EXAMPLES

Single SRAM

| MTBF (days) | FIT/Mbit 100 | 150 | 200 | 250 | 288 | 300 | 500 | 1000 |
|---|---|---|---|---|---|---|---|---|
| 4M | 104,167 | 69,444 | 52,083 | 41,667 | 36,169 | 34,722 | 20,833 | 10,417 |
| 9M | 46,296 | 30,864 | 23,148 | 18,519 | 16,075 | 15,432 | 9,259 | 4,630 |
| 18M | 23,148 | 15,432 | 11,574 | 9,259 | 8,038 | 7,716 | 4,630 | 2,315 |
| 36M | 11,574 | 7,716 | 5,787 | 4,630 | 4,019 | 3,858 | 2,315 | 1,157 |
| 72M | 5,787 | 3,858 | 2,894 | 2,315 | 2,009 | 1,929 | 1,157 | 579 |

| MTBF (weeks) | FIT/Mbit 100 | 150 | 200 | 250 | 288 | 300 | 500 | 1000 |
|---|---|---|---|---|---|---|---|---|
| 4M | 14,881 | 9,921 | 7,440 | 5,952 | 5,167 | 4,960 | 2,976 | 1,488 |
| 9M | 6,614 | 4,409 | 3,307 | 2,646 | 2,296 | 2,205 | 1,323 | 661 |
| 18M | 3,307 | 2,205 | 1,653 | 1,323 | 1,148 | 1,102 | 661 | 331 |
| 36M | 1,653 | 1,102 | 827 | 661 | 574 | 551 | 331 | 165 |
| 72M | 827 | 551 | 413 | 331 | 287 | 276 | 165 | 83 |

System with 6 SRAMs

| MTBF (weeks) | FIT/Mbit 100 | 150 | 200 | 250 | 288 | 300 | 500 | 1000 |
|---|---|---|---|---|---|---|---|---|
| 4M | 2,480 | 1,653 | 1,240 | 992 | 861 | 827 | 496 | 248 |
| 9M | 1,102 | 735 | 551 | 441 | 383 | 367 | 220 | 110 |
| 18M | 551 | 367 | 276 | 220 | 191 | 184 | 110 | 55 |
| 36M | 276 | 184 | 138 | 110 | 96 | 92 | 55 | 28 |
| 72M | 138 | 92 | 69 | 55 | 48 | 46 | 28 | 14 |

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# SOURCES OF RADIATION

- Alpha Particles ($\alpha$, $He^{++}$)

  Alpha particles (Helium nuclei) are generated by radioactive decay of naturally occurring contaminants, such as $^{232}Th$ and $^{238}U$, found in mold compounds and other semiconductor processing and assembly materials. E $\approx$ 2MeV to 9MeV.

- High-Energy Neutrons (n)

  Generated by galactic cosmic rays interacting with the Earth's atmosphere, and producing a shower of neutrons and other particles. E $\approx$ 10MeV to 1GeV.

  (Cosmic rays generate a cascade of other particles – muons, protons, etc.; however at near-terrestrial altitudes over 90% are neutrons.)

- Thermal Neutrons ($n_{TH}$)

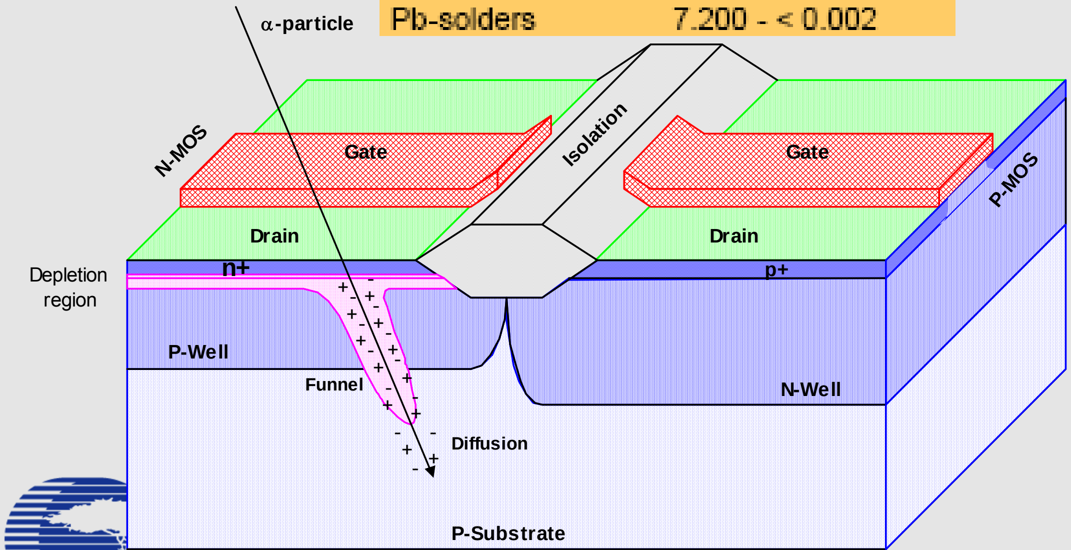
  Neutrons which have reached thermal equilibrium with the atmosphere. Of cosmic or terrestrial crust origins. E $\approx$ 25meV (kT).

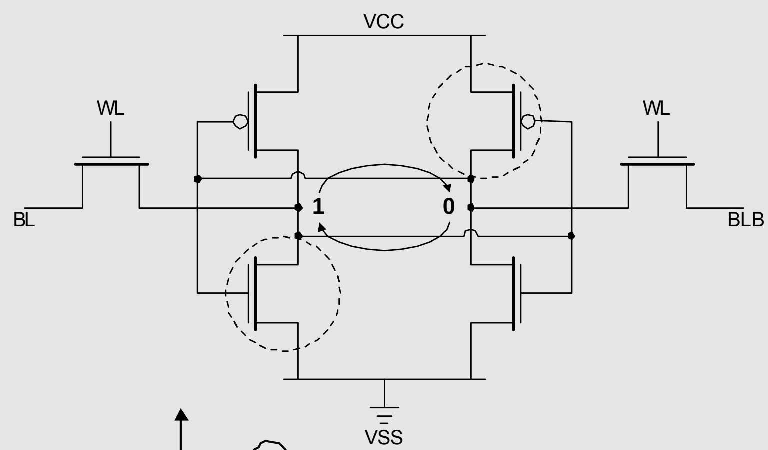
  An isotope of Boron ($^{10}B$, 20% natural abundance) has a high rate of interaction with thermal neutrons, decaying into Lithium and Helium nuclei.

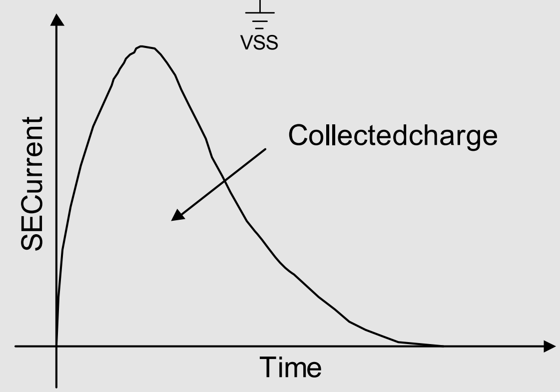
# ALPHA PARTICLES

- As the $\alpha$ traverses the semiconductor, it generates e-h pairs in its wake, on the order of $10^6$ pairs, or about 100fC of charge.
- The electric field in the depletion region causes charge drift, creating a current disturb.
- If the charge displacement overcomes the “critical charge,” Qcrit, stored in the memory cell, the stored data may flip, causing an error when it is next read. No permanent damage is caused – the cell may be re-written.

| | |
|---|---|
| Processed Wafers | 0.0009 $\alpha/cm^2$-hr |
| Cu Metal (thick) | 0.0019 |
| Al Metal (thick) | 0.0014 |
| Mold Comp. | 0.024 - < 0.002 |
| Underfill | 0.002 - 0.0009 |
| Pb-solders | 7.200 - < 0.002 |

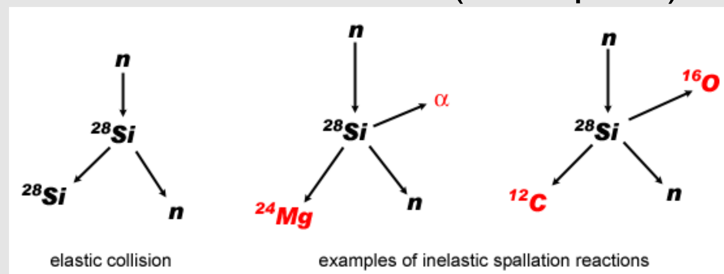


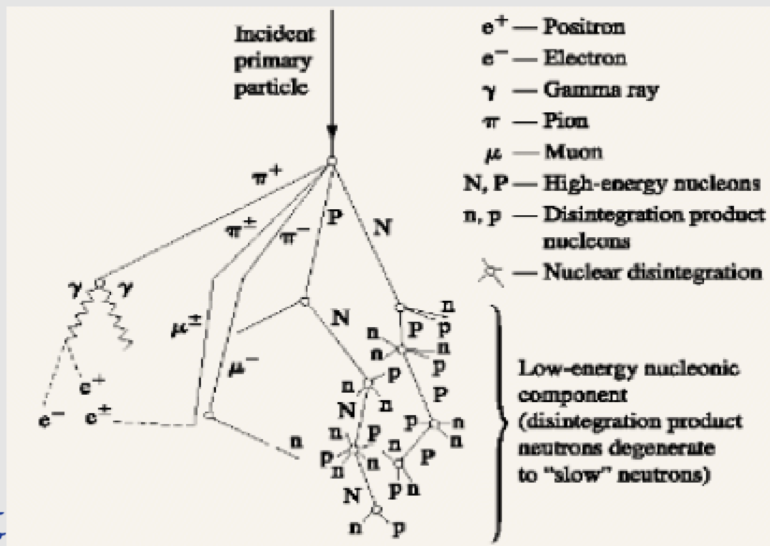



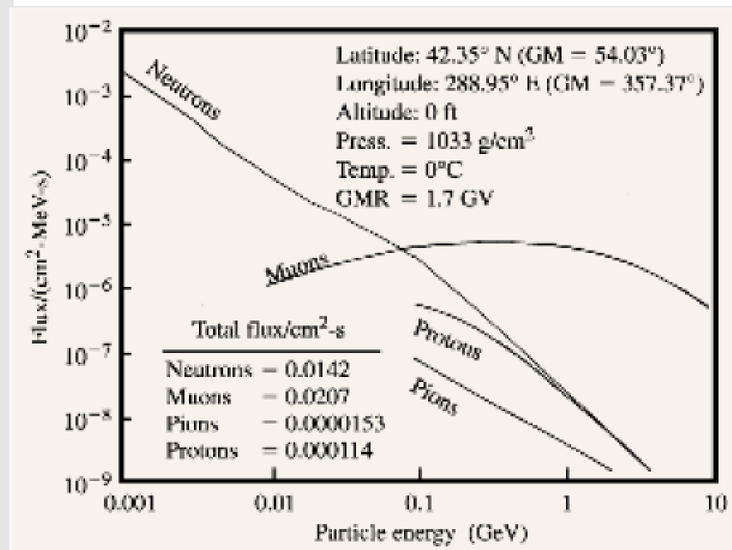



# HIGH ENERGY NEUTRONS

- Galactic cosmic rays (relativistic heavy nuclei like Fe) interact with the atmosphere starting at about 50km altitude and generate a shower of particles. After a few generations of collisions, mostly high energy and thermal neutrons reach the earth.
- No Coulombic interactions – 70% will go through 1 foot of concrete. Attenuation is about 1.4*n* where *n* is the number of feet of concrete.
- High-energy neutron-Si collision ➔ charged particles ➔ ionization tracks (like alphas).
- Neutron flux varies with:
  - Altitude (peaks at about 15km)
  - Position (worst at Poles)
  - 11-yr Solar Cycle (30% p-to-p)



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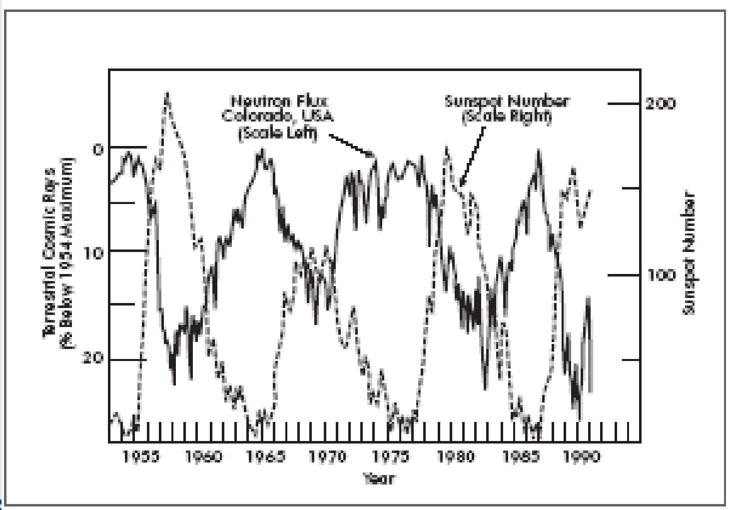
# NEUTRON FLUX RATIOS

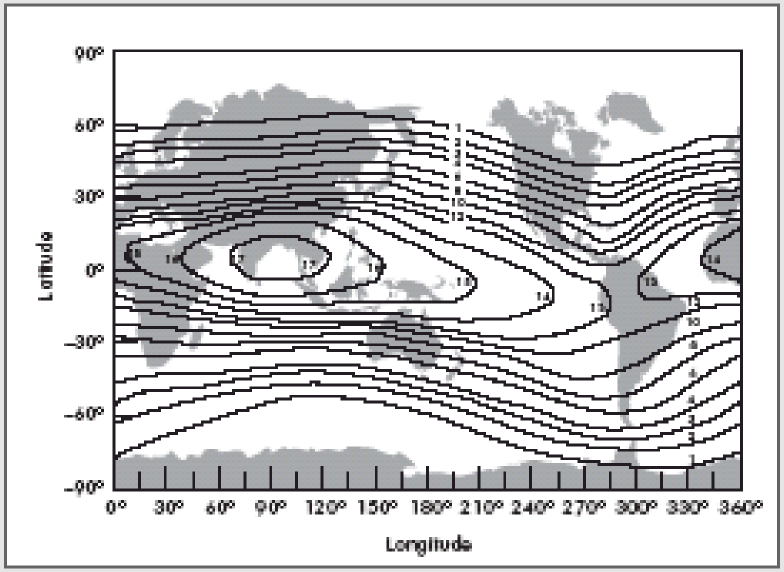
| | | |
|---|---|---|
| New York City | 1 | Sea level |
| Tokyo | 0.64 | 14m |
| CML | 0.60 | Cypress Manila (1st test site) |
| CODC | 4.39 | Cypress Colorado (2nd test site) |
| Mauna Kea | 9.22 | 4176m (new Cypress SSER site) |

All ratios quoted in “50% solar activity” conditions (average)

Solar Activity:

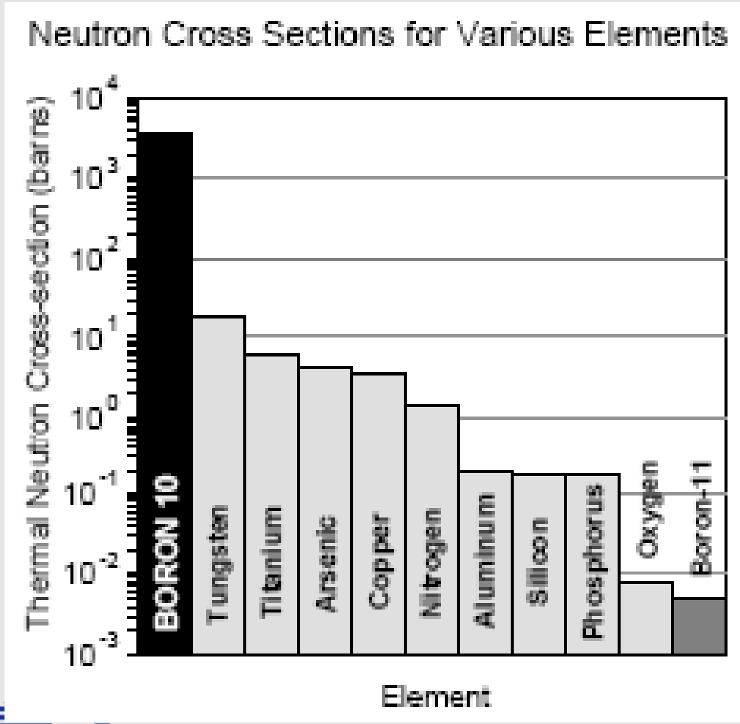


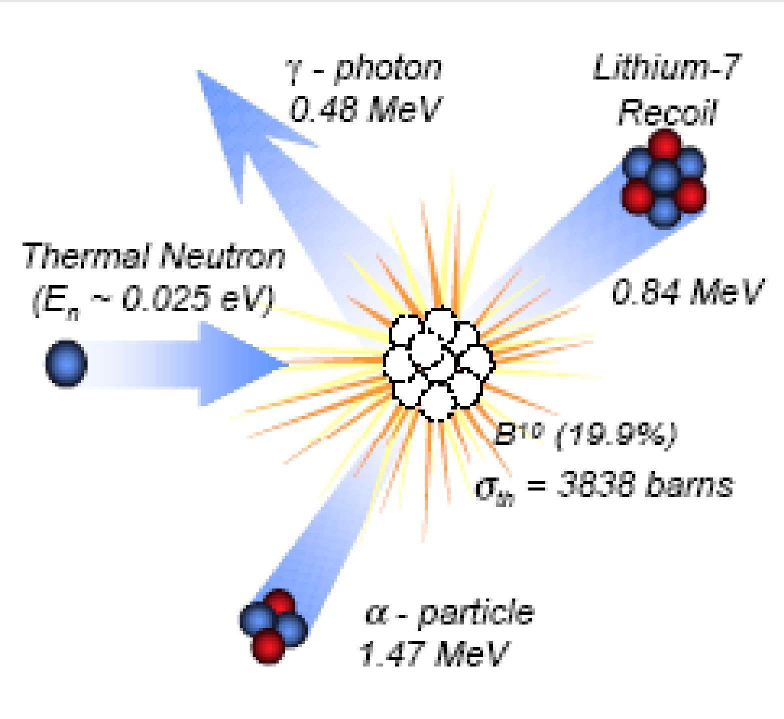

Magnetic Rigidity:



# THERMAL NEUTRONS

- Interact with $^{10}B$, an isotope of Boron, found in BPSG oxide films.
- $^{10}B \rightarrow Li^{+++} + He^{++}$, which in turn generate charge tracks in the semiconductor.
- Believed to dominate SER for devices which contain BPSG (CY uses PSG <180nm node).
- Can be stopped by polyethelene or Boron shields.



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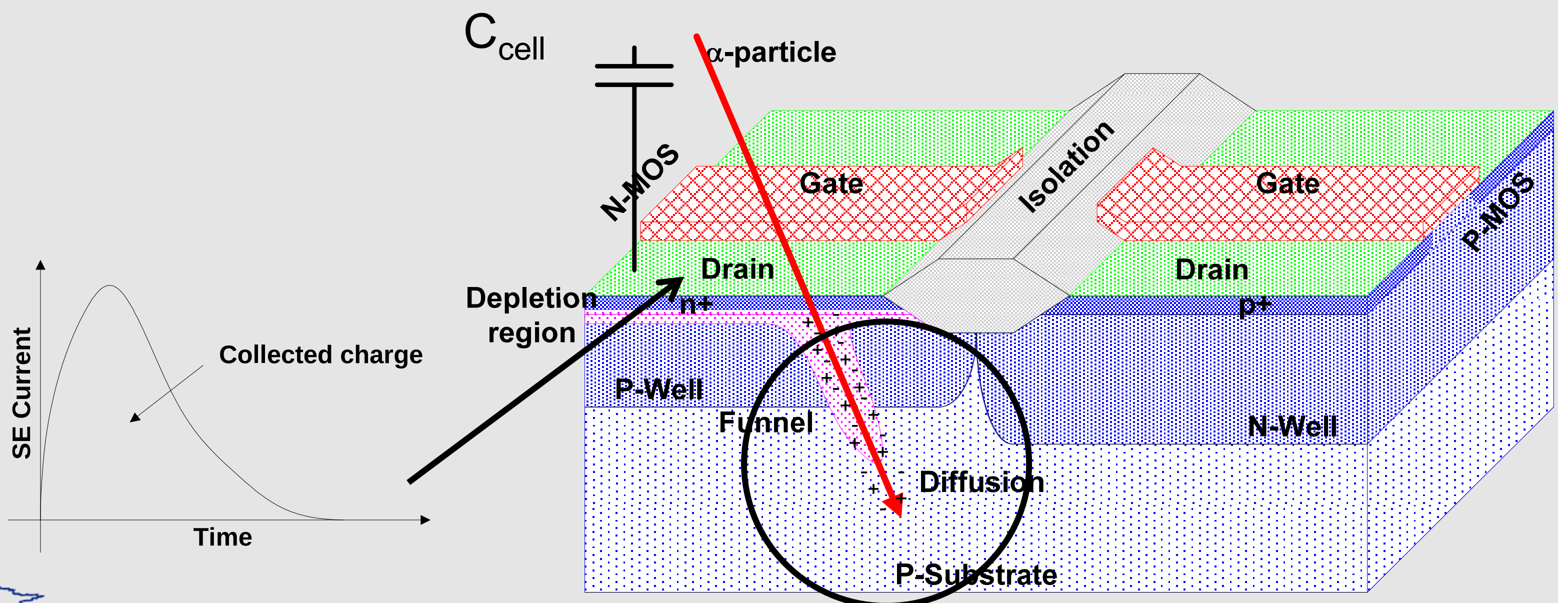
# SOFT ERROR MITIGATION TECHNIQUES

Mitigation techniques for SEU

- System Architecture (user)
- Chip Design and Architecture
- Process Technology and Cell Layout
  - Reduction of the particle generated charge in the IC substrate
  - Increase of the storage node capacitance $C_{cell}$.

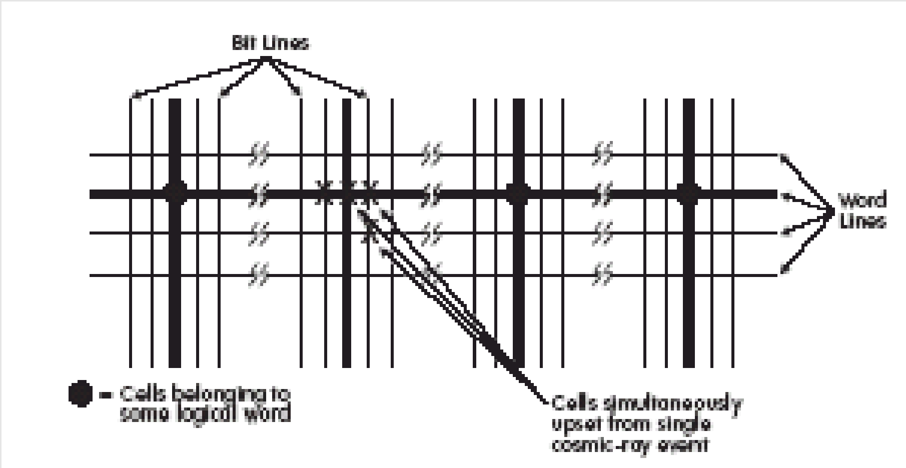


# SYSTEM MITIGATION TECHNIQUES

- System Architecture
  - Design system so that soft error does not appear to user outside the system (TCAM false hit => request data again)
  - External (system-level) Error Correction (ECC)
- Parity Protection
  - Re-fetching of data from clean storage (NVM) if parity error detected
- Multi-Store Protection
  - If less than ½ memory is used replicate the data in different memory location and use both data sets to correct errors
  - Can be retrofitted if ECC is not available
- Voter Scheme
  - Multiple instances of critical data and voter scheme to harden data

# DESIGN MITIGATION TECHNIQUES

- Error Correction Code (ECC)
  - Additional bits are added to the data word to detect and correct bit upsets (72/64 configuration)
  - Die size increase (6% for 128bit data word)
- Bit interleaving
  - Avoid multi bit upsets by spreading out the data word
  - Implemented on all Cypress products
- Memory Scrubbing
  - Used to avoid an additional upset to already corrupted data by periodic update of memory information
  - Implemented on nvSRAM products through software command



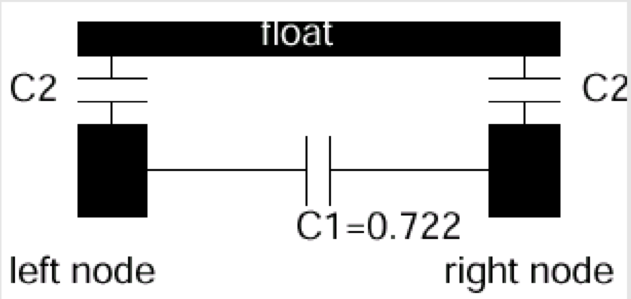
# PROCESS MITIGATION TECHNIQUES

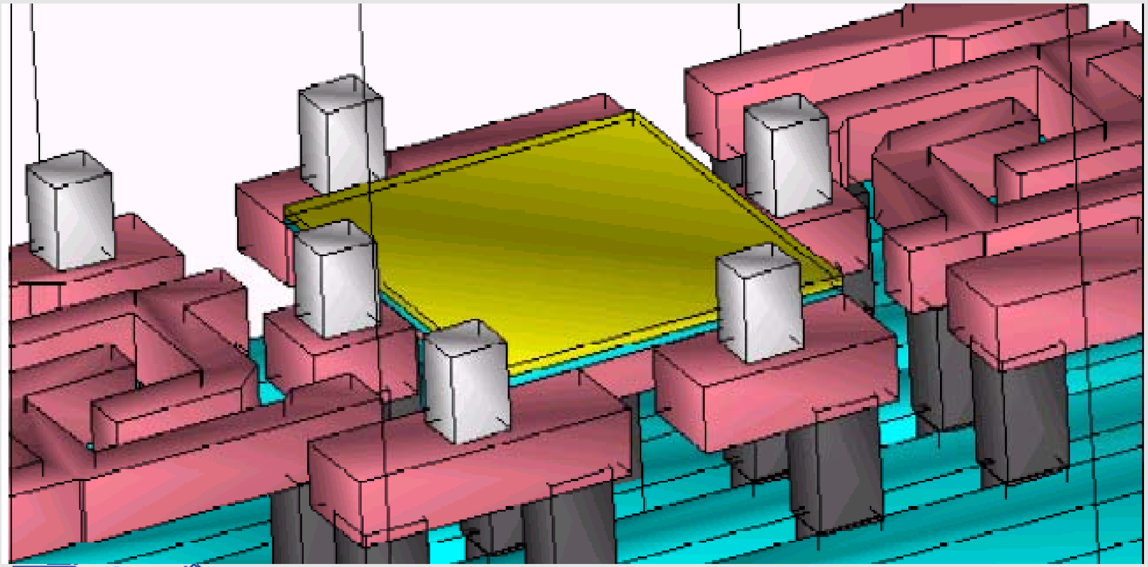
- Node Capacitance Techniques
  - Increase of Node Coupling Capacitance between Storage Nodes:
    - Backend Metal-in-Metal (MIM) capacitor
    - DRAM capacitor on top of memory cell
    - Size up the diffusion node (larger die size)
    - Increase sidewall coupling capacitance (Self Aligned Contacts)
    - Increase junction capacitance (at expense of junction breakdown)

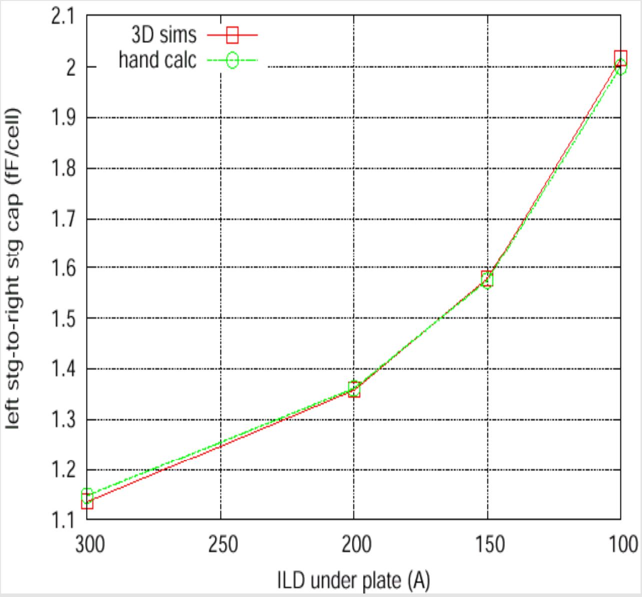
- Substrate Engineering Techniques
  - Epitaxial Substrate:
    - Lightly doped epi-layer on a heavily doped substrate.
    - Short funnel length and less generated charge in EPI layer.
  - Triple Well:
    - Deep n-well is built underneath both n-well and p-well tubs in p-type substrate.
    - Collects electrons before they can upset the by surface memory cell => not so simple!! Parasitic Bipolars

# NODE SER CAPACITOR

- Manufactured in local interconnect or Metal layers
- Metal plate increases storage node capacitance
- Up to 70% improvement possible for alpha SER (20% for neutrons)





# EPITAXIAL SUBSTRATE

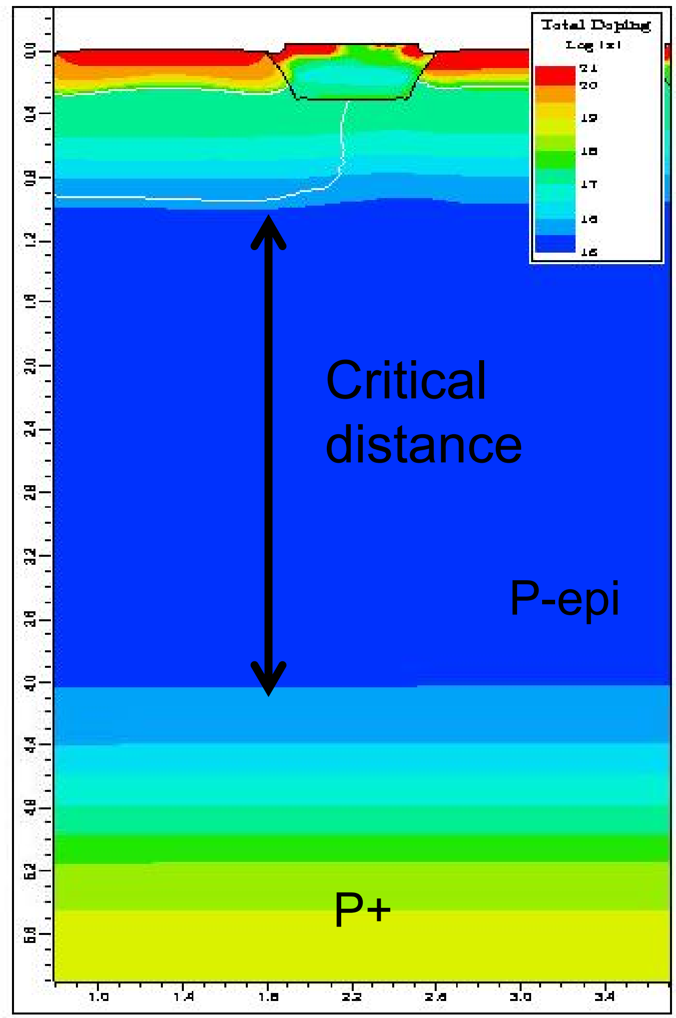
- Efficiency depends on critical distance between surface junctions and high doped substrate
- No improvement observed for 90nm node besides cost penalty for EPI substrate

| VDD | Vcore | *Single Bit Upset Failure Rate (FIT/Mbit)* | | | |
|---|---|---|---|---|---|
| | | *Epi 1.5um* | *Epi 2.0um* | *Epi 2.5um* | *Standard* |
| 2 | 0.85 | 365.09 | 309.89 | 289.08 | 373.80 |
| 2.36 | 1.00 | 287.99 | 219.40 | 287.07 | 287.88 |
| 2.65 | 1.12 | 209.78 | 220.77 | 216.66 | |
| 3.06 | 1.30 | 193.28 | 232.00 | 209.69 | 155.94 |
| 3.8 | 1.61 | 130.57 | 87.06 | 164.82 | 209.80 |

Table #1 – Summary of SBU results (FIT/Mbit) calculated for NYC

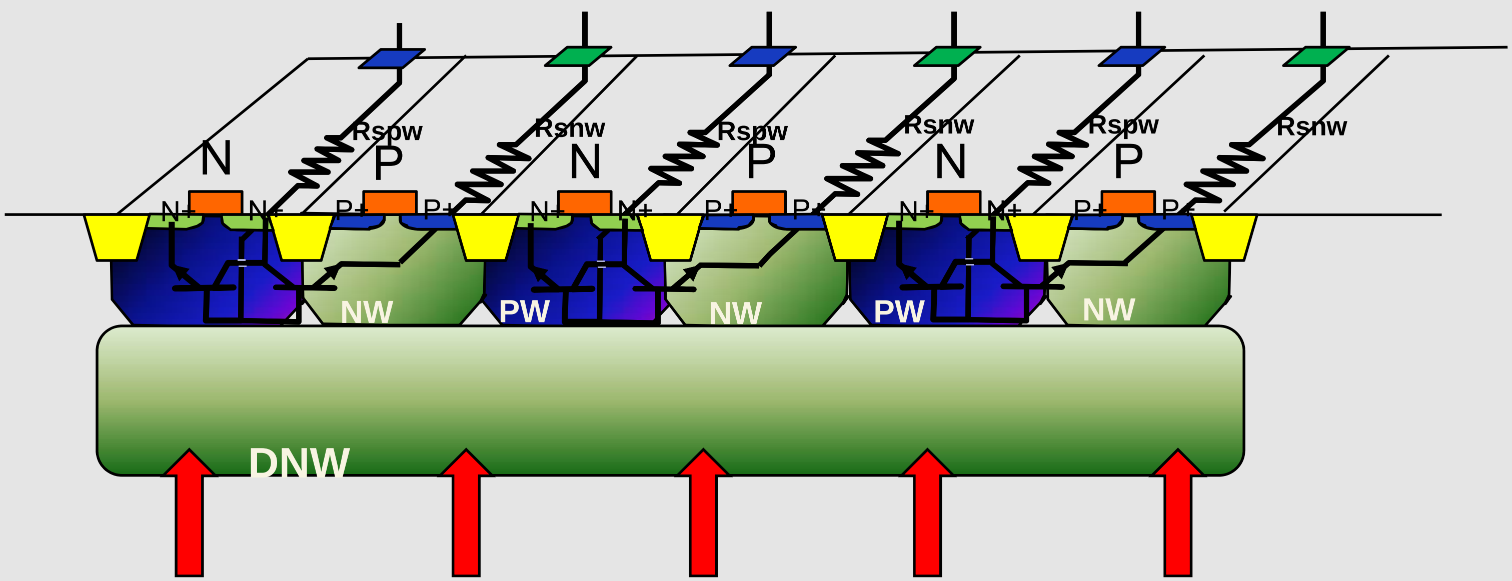
| VDD | Vcore | *Multiple Bit Upset Failure Rate (FIT/Mbit)* | | | |
|---|---|---|---|---|---|
| | | *Epi 1.5um* | *Epi 2.0um* | *Epi 2.5um* | *Standard* |
| 2 | 0.85 | 68.19 | 51.12 | 158.72 | 27.97 |
| 2.36 | 1.00 | 53.58 | 51.74 | 53.69 | 25.47 |
| 2.65 | 1.12 | 38.50 | 55.65 | 82.76 | |
| 3.06 | 1.30 | 37.57 | 46.36 | 13.23 | 20.15 |
| 3.8 | 1.61 | 0.00 | 3.46 | 3.46 | 65.57 |

Table #2 – Summary of MBU results (FIT/Mbit) calculated for NYC



# TRIPLE WELL SCHEME

- Deep Nwells (DNW) widely used for ABB (active body biasing)
- DNW is built underneath both n-well and p-well tubs and connected to Vcc and isolates the p-well region
- Parasitic bipolars are easier to turn on and increase MBU FIT rate
  - N+ Drain – Pwell – Nwell: <180nm technologies experienced
  - N+ Drain – Pwell – N+ Source:  severe for 90/65nm technologies (5-10x higher)




Neutron Event e- Injection

# TRIPLE WELL NEUTRON ASER DATA

| Part | SBU | Phys.MBU | Total SEU | SEL | %MBU | Comment |
|---|---|---|---|---|---|---|
| R9 36M QDR | 175 | 25 | 225 | 0 | 11 | TSL |
| R9 18M QDR | 175 | 25 | 225 | 0 | 11 | TSL |
| R9 72M TW L122 | 174 | 165 | 504 | 0 | 32 | TSL |
| R9 72M TW A | 175 | 99 | 373 | 0 | 27 | TSL |
| R9 72M TW C | 159 | 106 | 371 | 0 | 29 | TSL |
| R9 72M TW G | 140 | 85 | 310 | 0 | 27 | TSL |
| R9 72M TW H | 163 | 86 | 335 | 0 | 25 | TSL |

- Comparable SBU rate but dramatic increase in MBU rate
- Data have been confirmed on 65nm Technology

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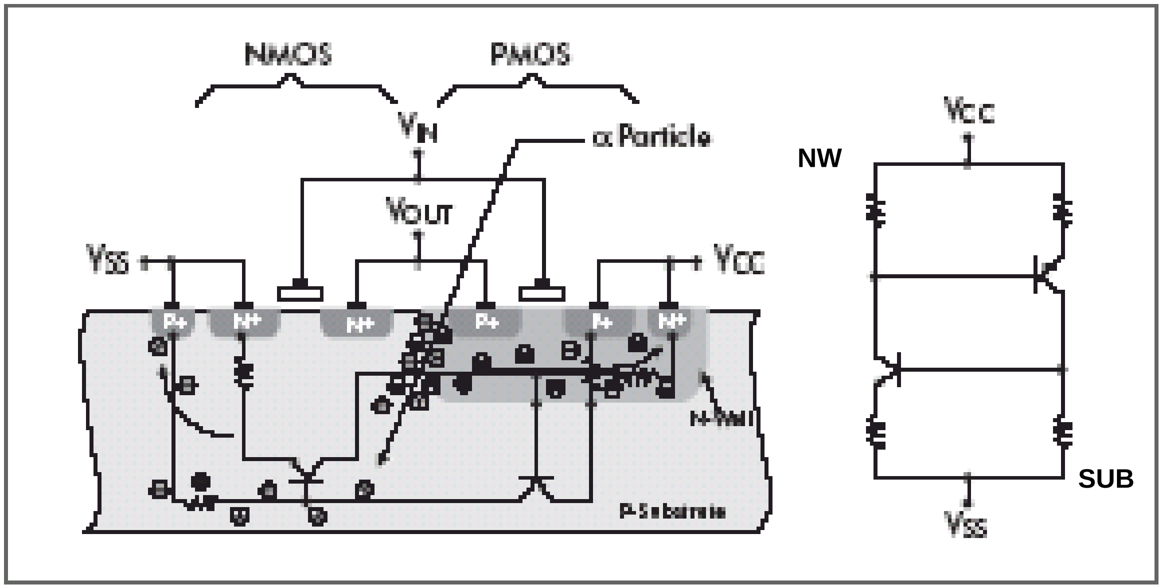
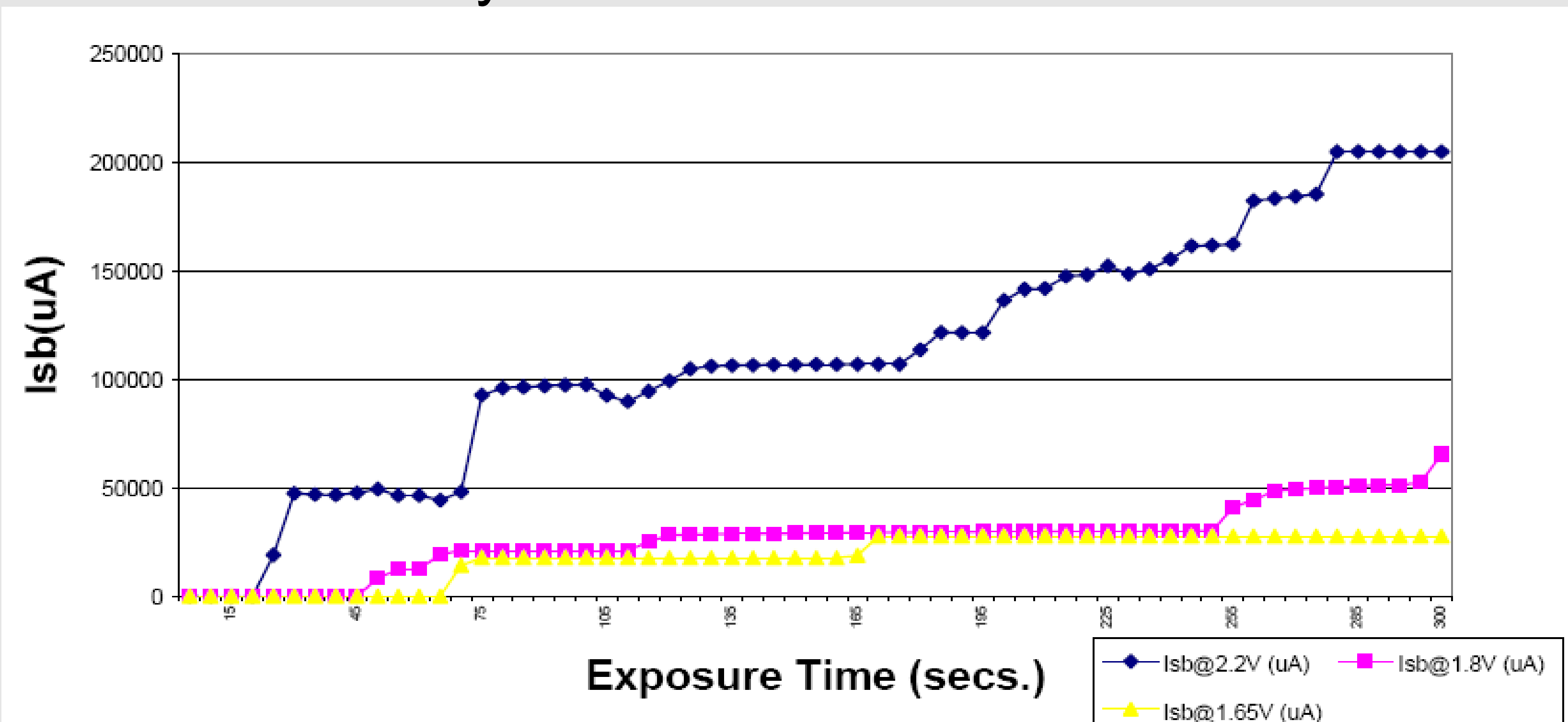
# SINGLE EVENT LATCH-UP

- Non-catastrophic condition
- Whole memory block latching up
- Recovers fully during power down/up cycle
- Mitigated by same techniques as standard latch-up (well engineering, substrate tapping)




# DETECTION OF SEL

- Place Memory under $Th^{232}$ foil:



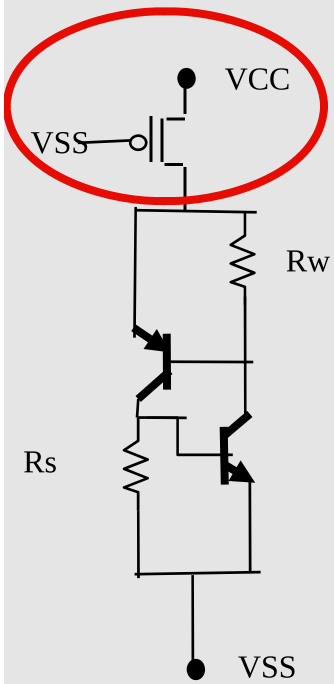

- Non-recoverable blockfailures => power down
- Conventional mitigation of SEL through technology process options (EPI, Triple well)

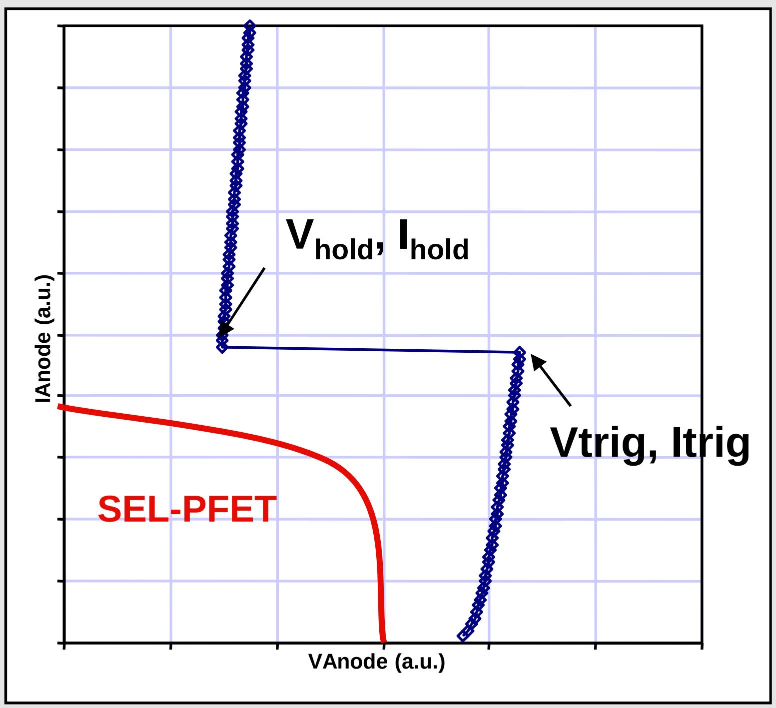
# CY SEL MITIGATION STRATEGY

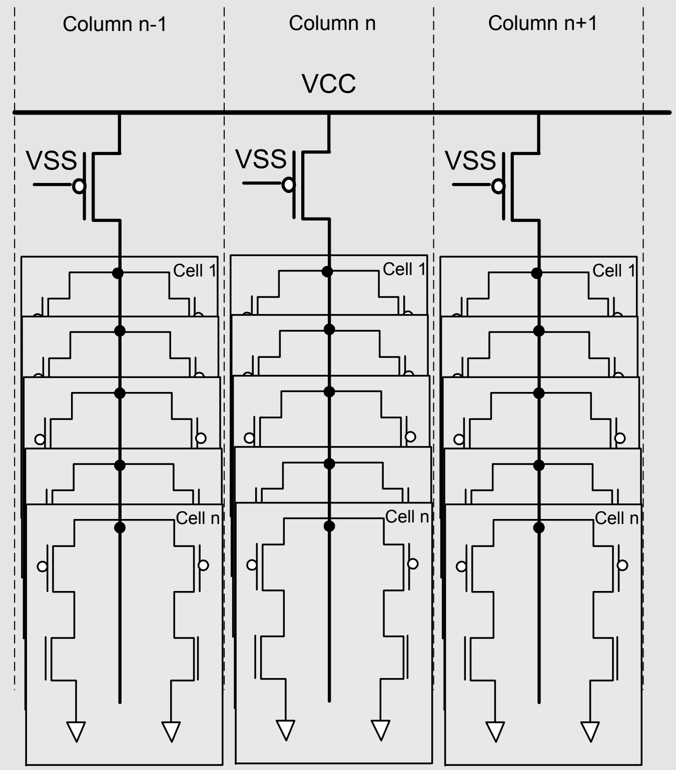
- Design Solution Implemented:

  Current Limiting Device (SEL-PFET):

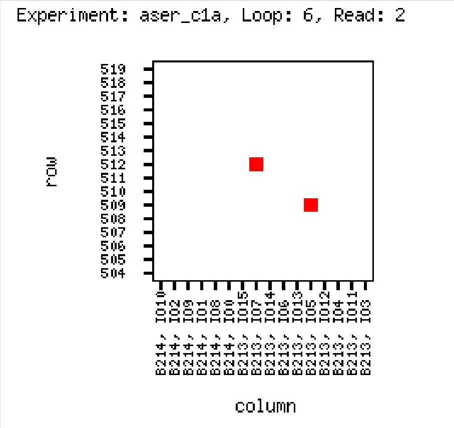
  - Use A PMOS Current Limiting Device In Every Column Pair
  - Works By Quenching Current Thus Preventing Latchup
  - No Impact To Normal Operation Of Memory Write And Read



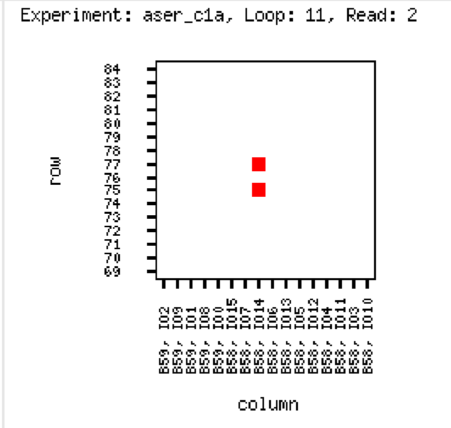



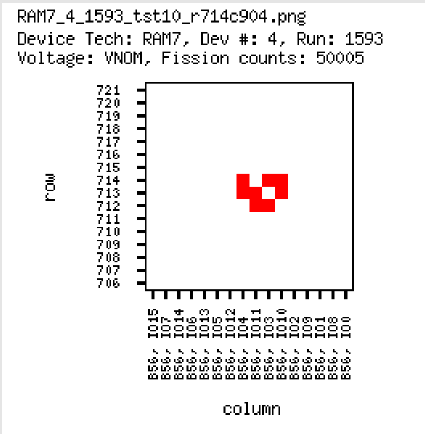
# MULTI-BIT UPSETS AND LATCHUP

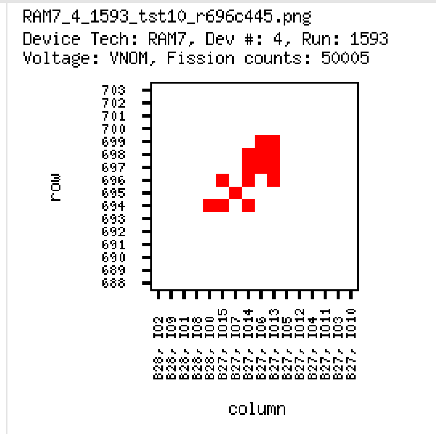



Two SEUs

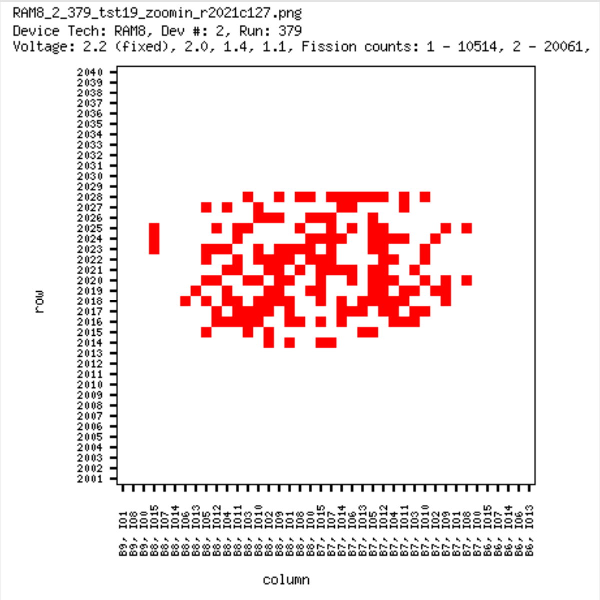



One MBU

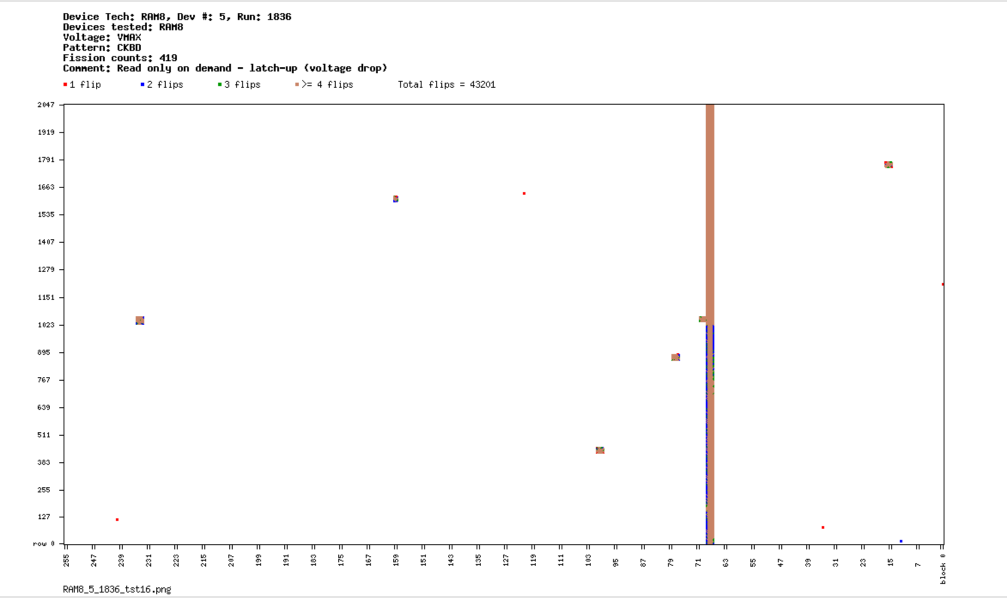



Neutron MBU examples




SEL






CYPRESS

IEEE-SV CHAPTER MEETING, OCT. 14 2008, SUNNYVALE, CA

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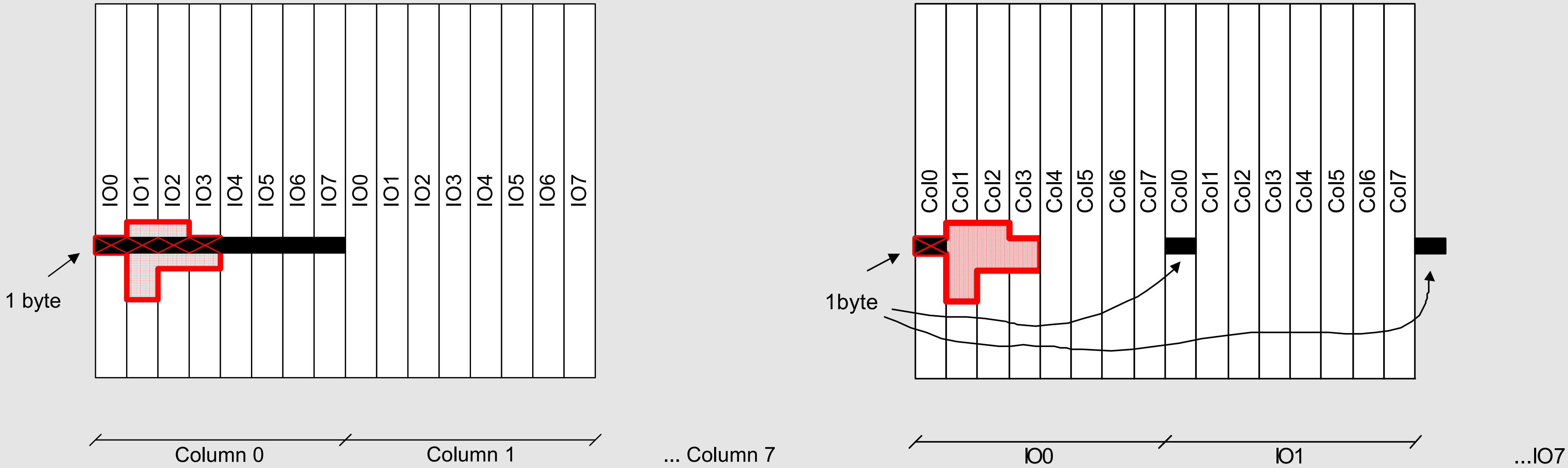
# EFFECT OF ARCHITECTURE

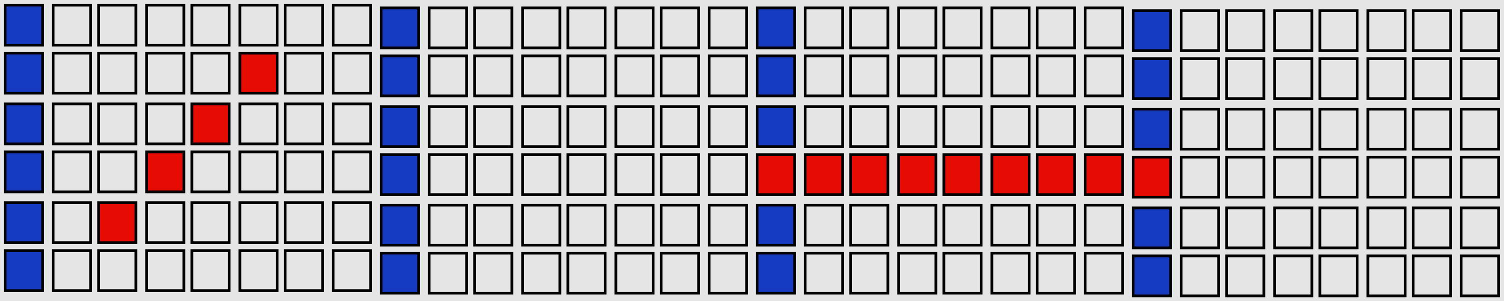
- Multiple Bit Events can lead to Single or Multiple Errors within a Byte.



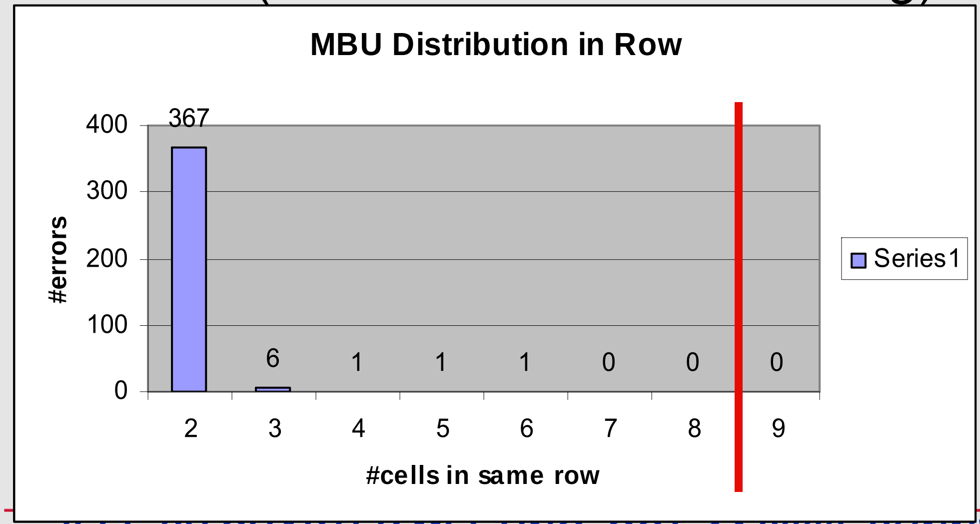

- ECC (Error Correction Circuit):
  Very effective in correcting Single-bit errors, but at expense of larger chip area. Can effectively be implemented at the system level.
- Voting:
  Redundant circuitry is designed in the system together with a “judge” passing the data from the majority of the “voters.”

# SBU vs. MBU

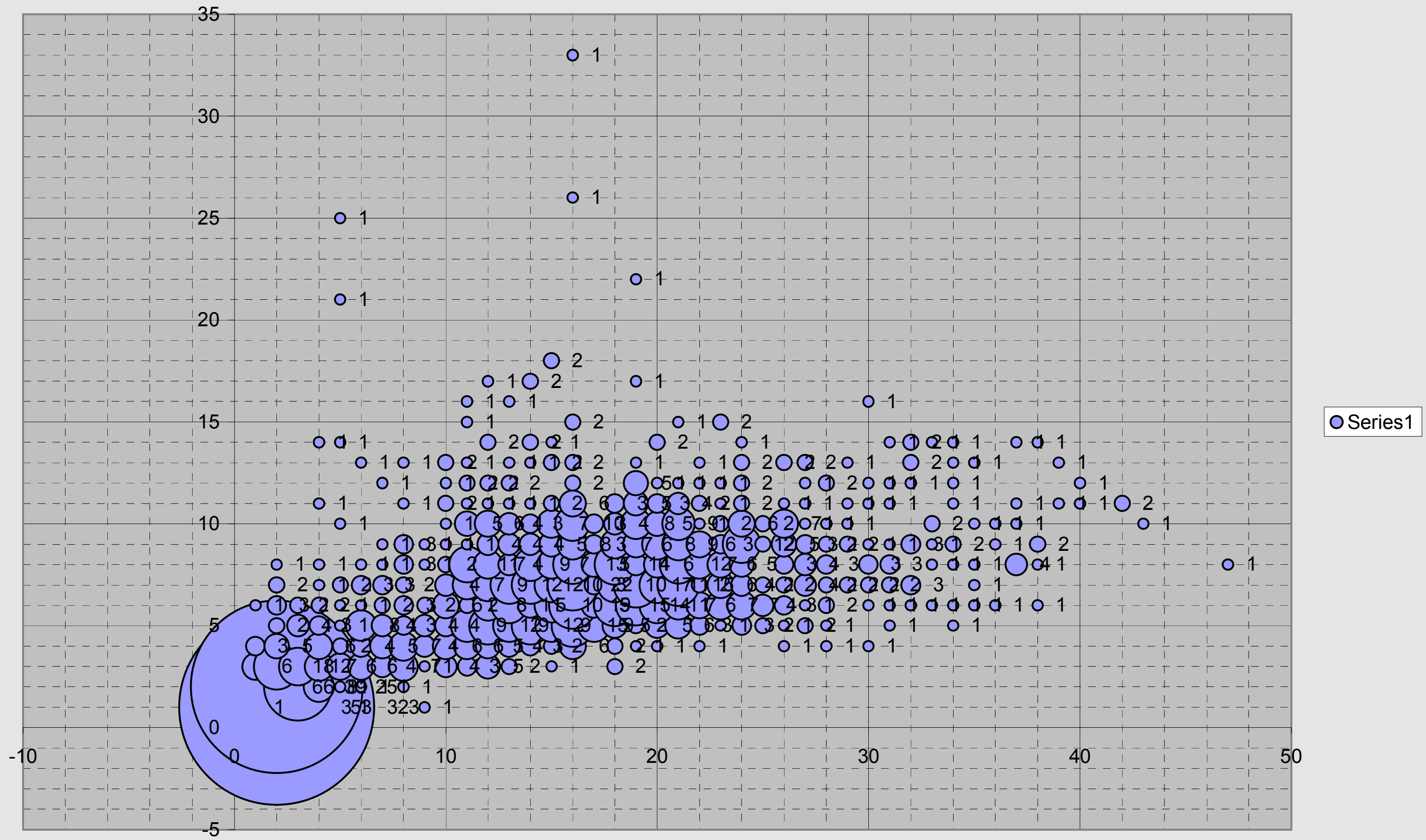
- MBU Characteristics: (e.g. 8bit interleaving)



- Only MBU's in the same row can cause a logical MBU
- Interleaving needs to be wider than MB distribution
- R9 72M QDR Data: (**16bit** burst of 4 interleaving)

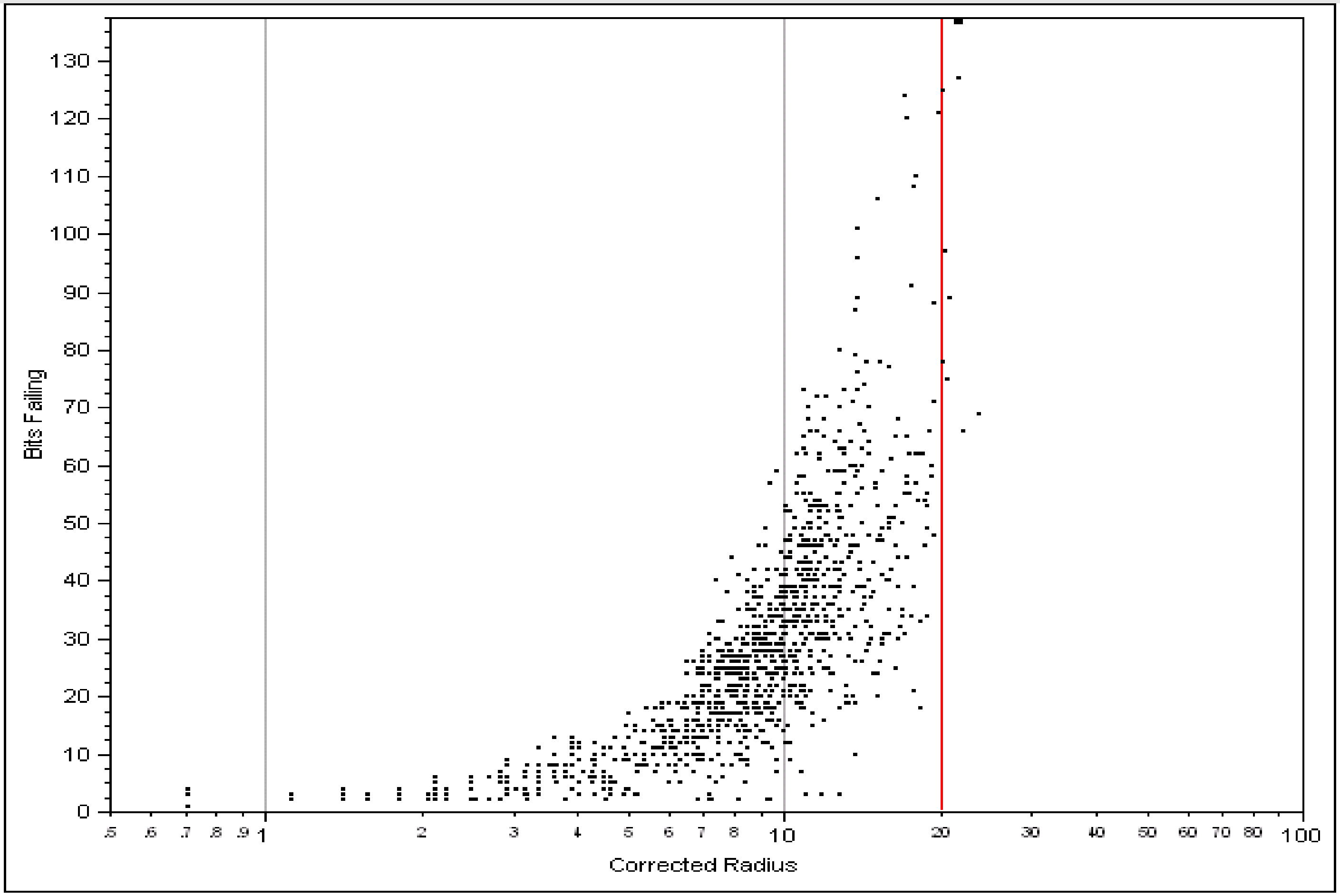


# SBU/MBU ANALYSIS



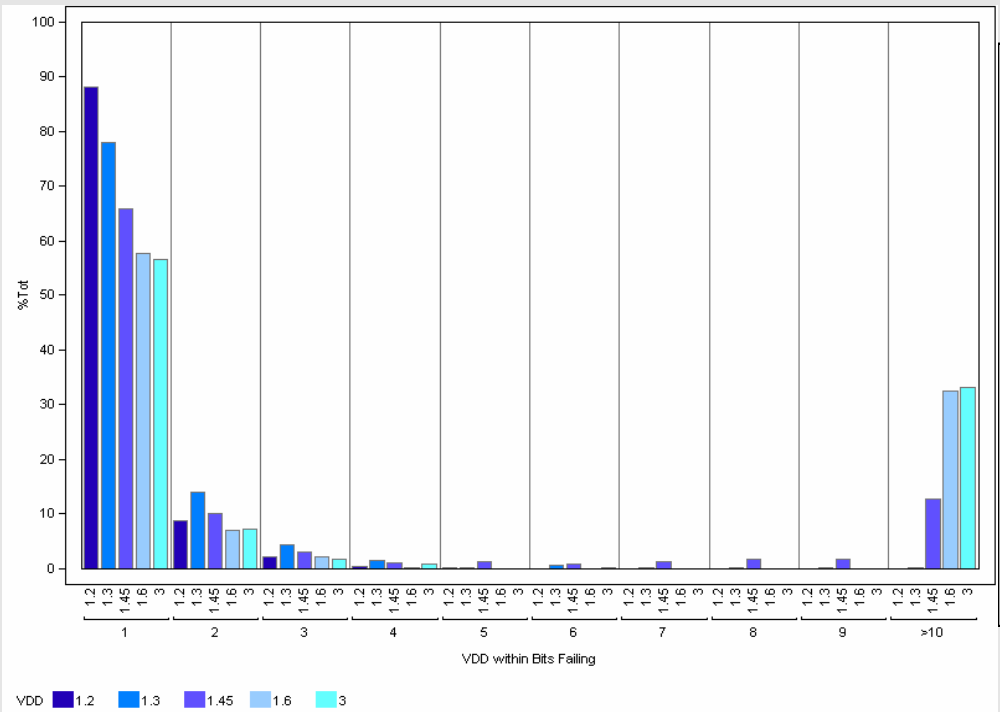

- Investigation of all MBU's and occurance

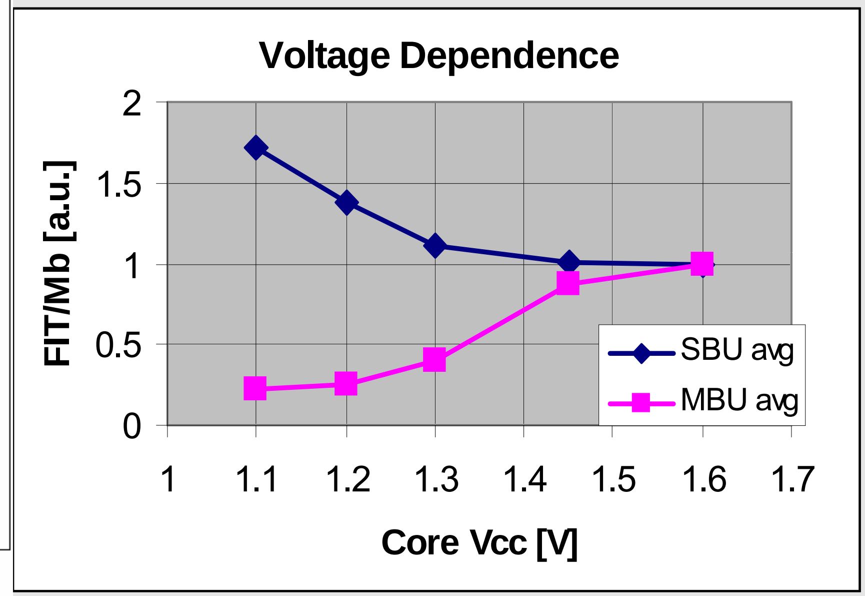
# MBU RADIUS




- Bits spread more than 20 cells are consider independent events

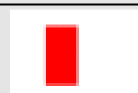
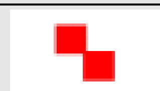
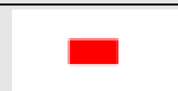
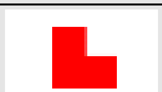
# VCC DEPENDENCE SBU/MBU



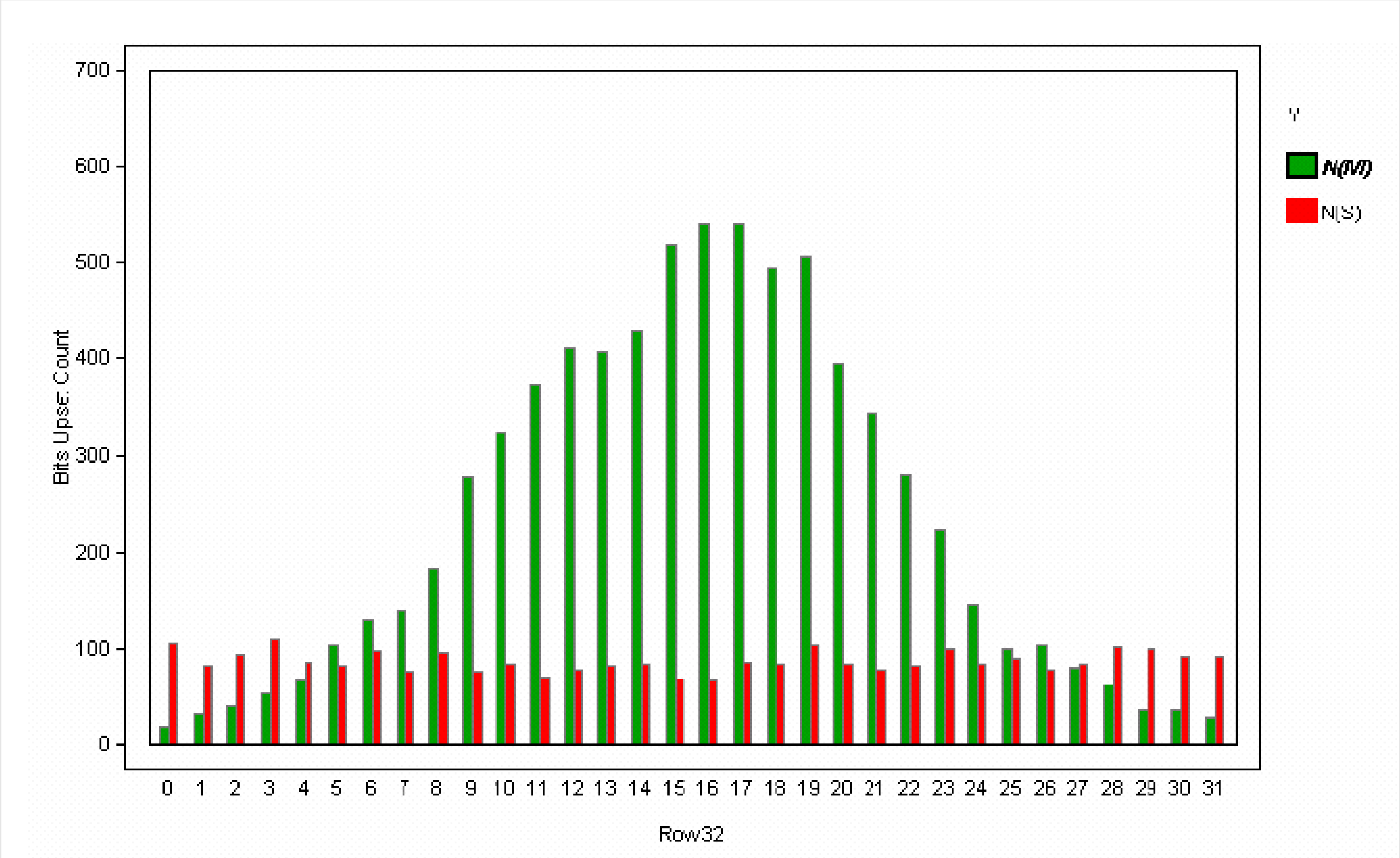

- SBU increase with lower Vcc
- MBU decrease with lower Vcc (LU dominated or parasitic bipolars weaker)

# SHAPE DEPENDENCE SBU/MBU

| VDD | MBU Shape | | | | | | |
|---|---|---|---|---|---|---|---|
| | 2-bit Other |  |  |  | 3-bit Other |  | n-bit |
| 1.2 | 10 (7.51%) | 7 (5.26%) | 29 (21.80%) | 52 (39.09%) | 12 (9.02%) | 14 (10.52%) | 9 (6.76%) |
| 1.3 | 28 (12.28%) | 18 (7.89%) | 37 (16.22%) | 64 (28.07%) | 22 (9.64%) | 24 (10.52%) | 35 (15.35%) |
| 1.45 | 11 (2.51%) | 16 (3.62%) | 18 (4.10%) | 64 (14.61%) | 14 (3.19%) | 18 (4.10%) | 297 (67.80%) |
| 1.6 | 8 (1.63%) | 7 (1.43%) | 19 (3.89%) | 46 (9.42%) | 9 (1.84%) | 15 (3.07%) | 384 (78.68%) |

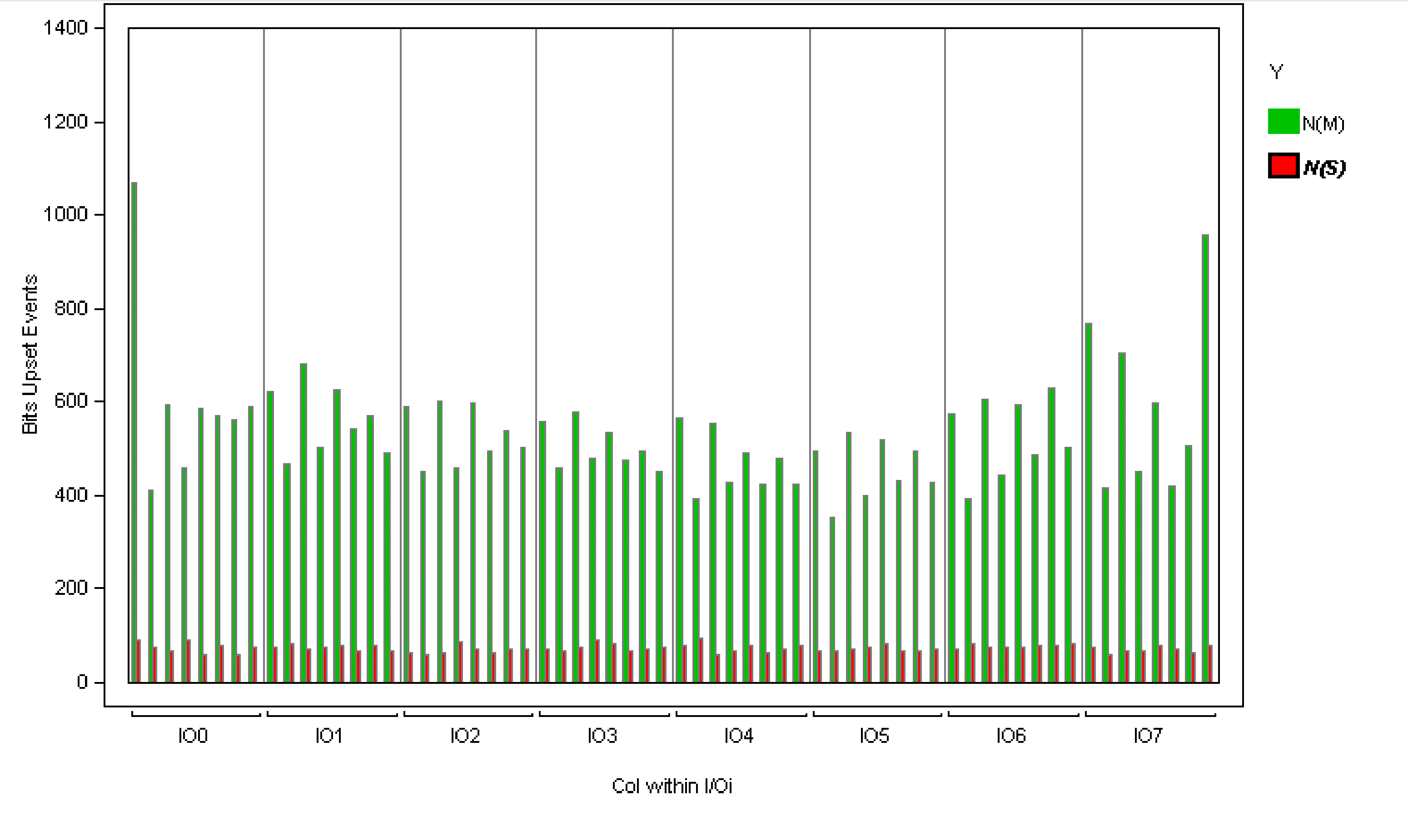
- Strong well dependence of MBU's – MBU spread in direction of the Nwell or Pwell
- Significant amount of "n-bit" events
- Double bit events dominating due to mirrored memory cell core architecture

# ROW DEPENDENCE SBU/MBU




- Strong row dependence of MBU’s

# COL DEPENDENCE SBU/MBU



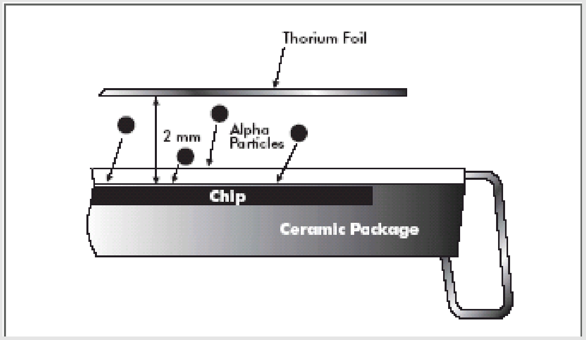

- Weak col dependence of MBU’s

# TOPICS

- DEFINITIONS
- SOURCES OF RADIATION
- MITIGATION TECHNIQUES
  - SEL AND MBU MITIGATION
- **MEASUREMENT TECHNIQUES**
- MODELING/SIMULATION OF SER
- CYPRESS DATA
- CONCLUSIONS

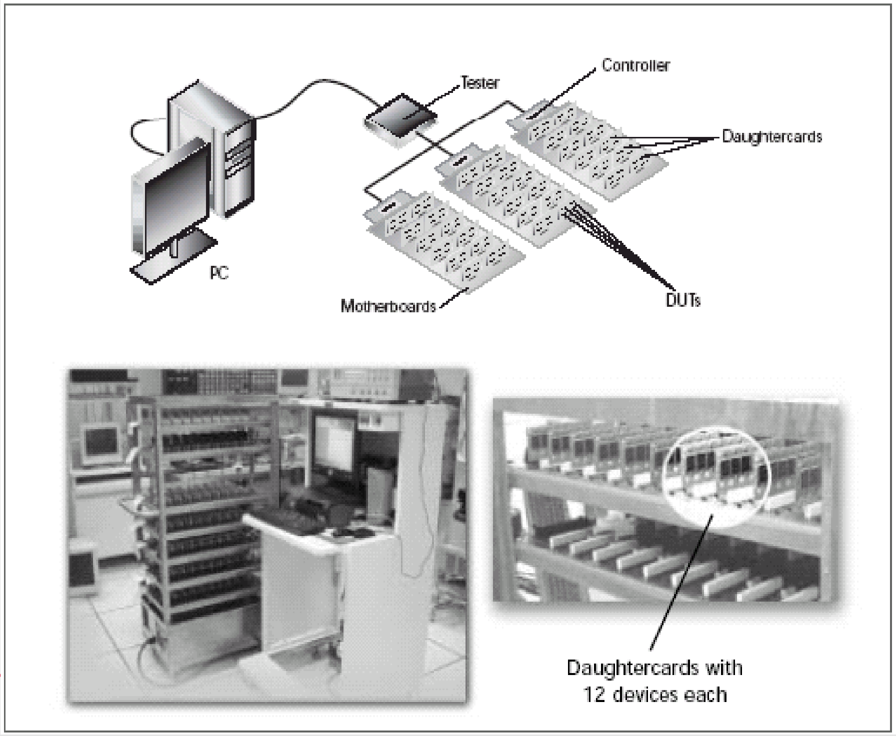
# SE MEASUREMENT TECHNIQUES

- Alpha Particles:
- Accelerated alpha measurements with $Th^{232}$ foil
- Neutron Particles:
- Accelerated neutrons measurements at LANL, IRoC
- Accelerated proton measurements at Harvard
- Thermal Neutrons:
- Measurements taken by USNA using nuclear reactor



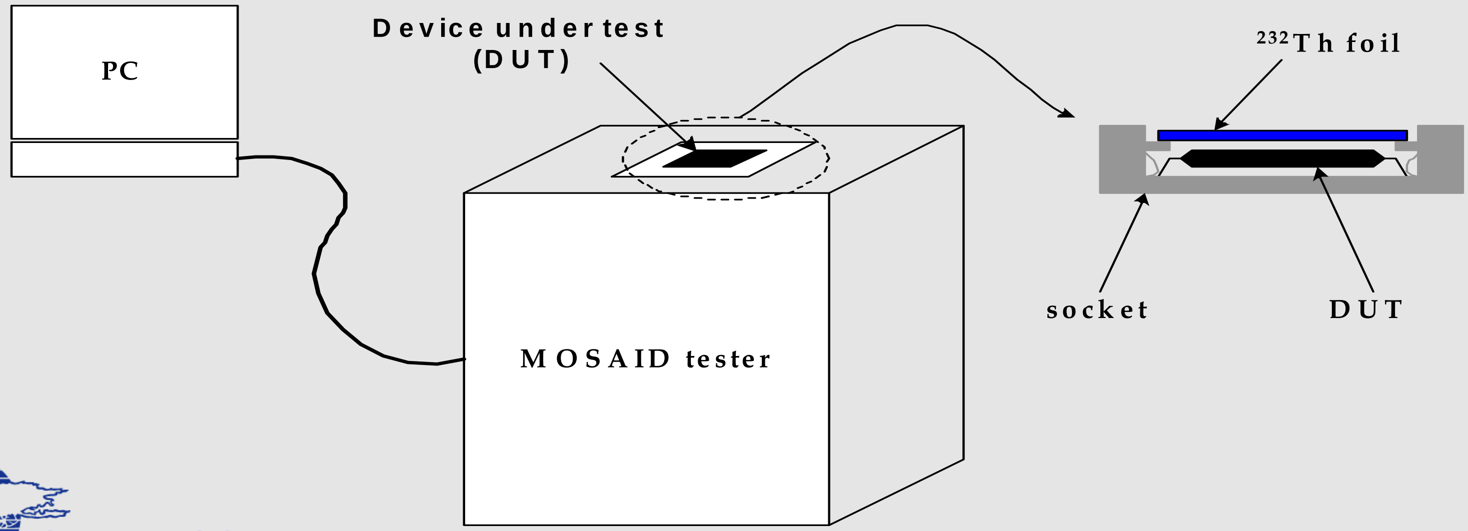

**Life Testing:**

- **Measuring "real" soft error rate in large electronic systems (alpha +cosmic)**
- **Mauna Kea, Colorado and Philippines Cypress test sites**
- **Developed own tester**



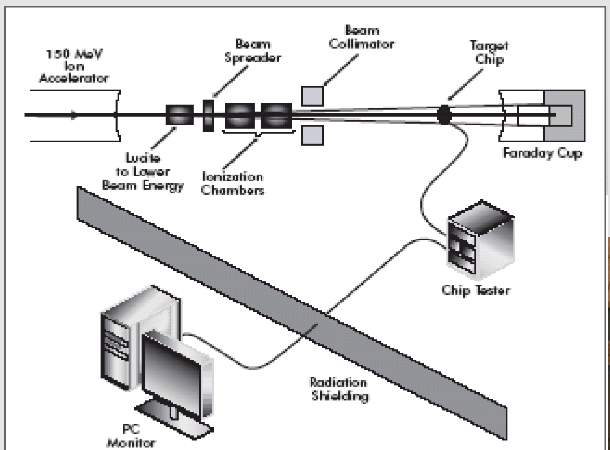
# ALPHA MEASUREMENT SETUP

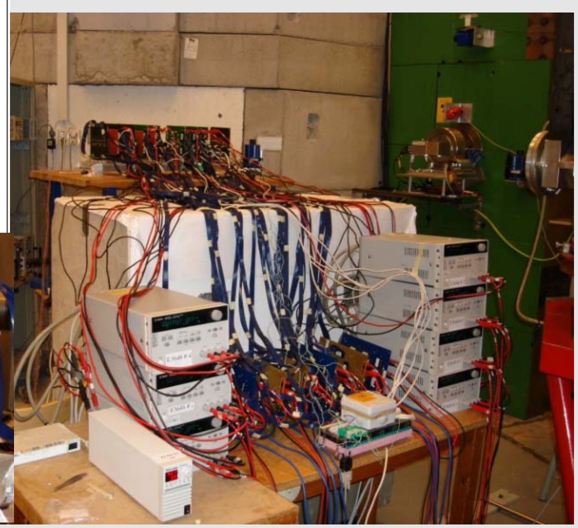
- Tester with the open top DUT and $^{232}Th$ foil positioned at a predefined distance from the die surface.
- The alpha particle source $^{232}Th$ is calibrated and its flux ($\alpha/cm^2/min$) is known at a specific distance.
- Test flow:
  - Write/Verify of a known data pattern (checkerboard, 0 only, 1 only)
  - Wait period with the alpha source in position
  - Read to monitor and log all the "bit-flip" occurred.
  - Monitor current for SEL events

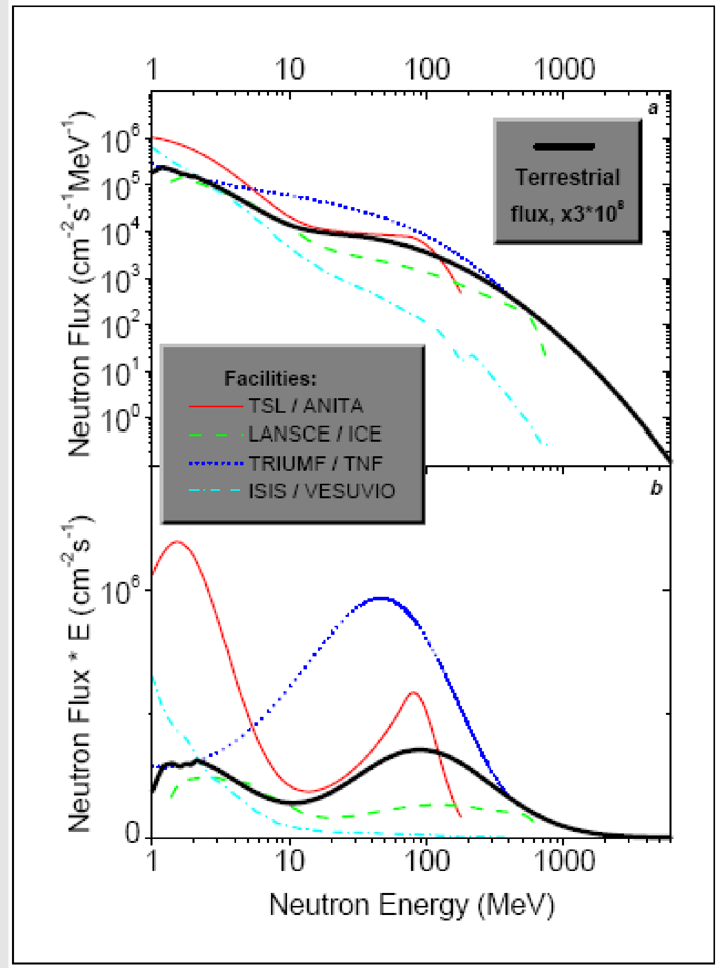


# ACCELERATED PARTICLE TESTING

- Neutrons, Protons, and heavy particles
- About 20 sites worldwide which are frequently used (JEDEC)
- Beams can be mono-energetic or spectral
- Accelerated beam flux is calibrated to natural cosmic flux at sea level (13 neutrons/cm2.hr)

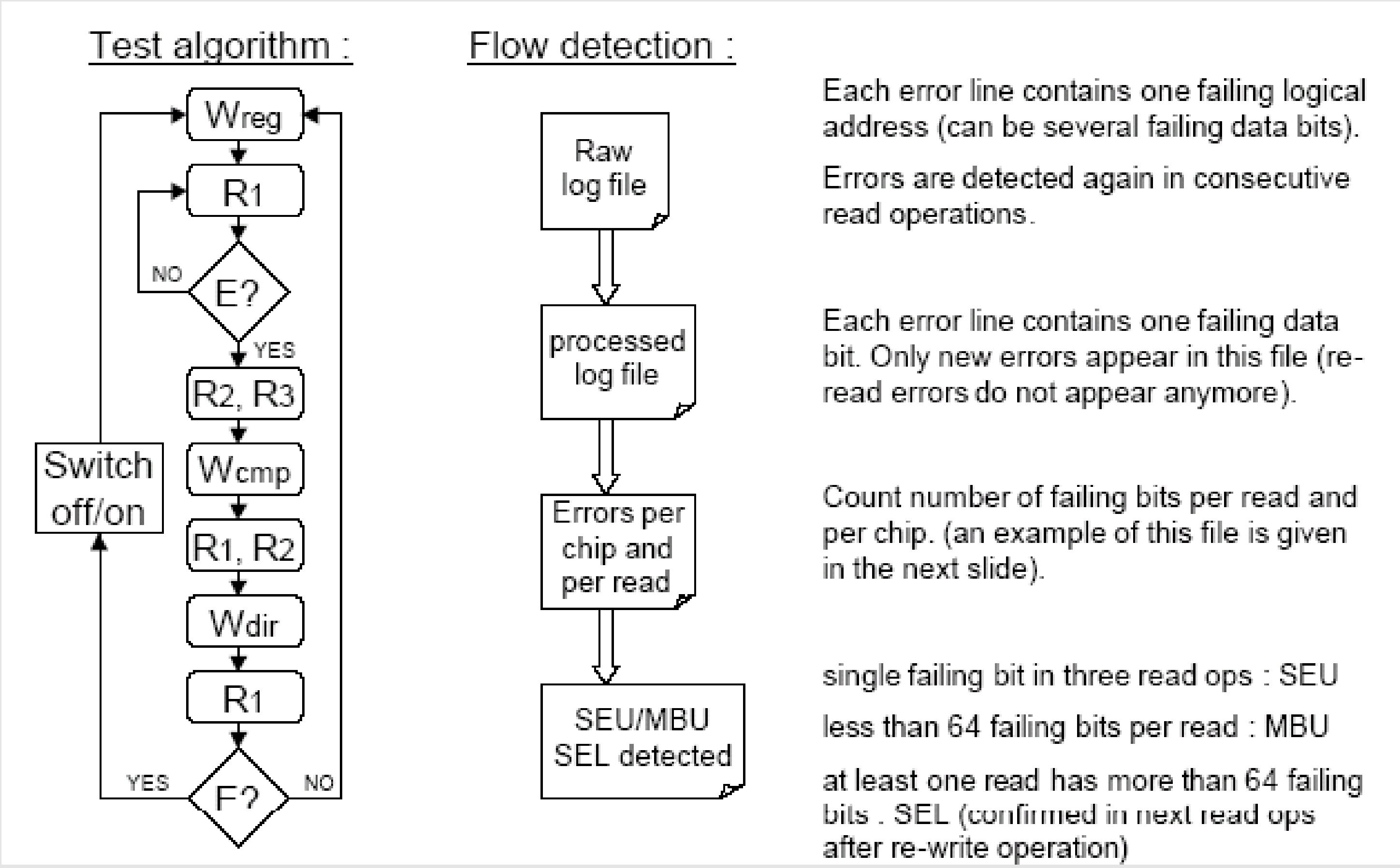




# NEUTRON/PROTON TEST FLOW

- State-of-the-art test flow to catch MBU,SEL (IRoC)
- Eliminate tester hardware differences



# SYSTEM SER – LIFE TESTING

- Build large memory banks
- Test natural SER without acceleration
- Test time from 3wks (CO) to months (Philippines) depending on particle flux
- Two altitudes allow extraction of Alpha and Cosmic contributions
- Cave testing allows elimination of Neutron particles

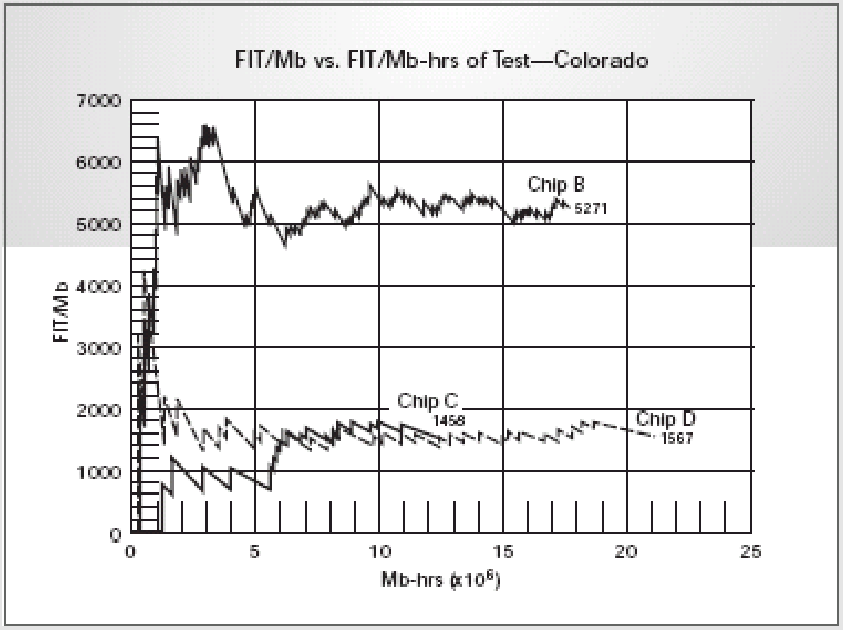



*Table 7.6. Accelerated SER vs. Life-Testing (Colorado and Philippines experiments before solar flare incident). Cosmic SER Data is Scaled to NYC.*

| | SER Accelerated Testing (FIT/Mb) | | | SER Life Testing (FIT/Mb) | | |
|---|---|---|---|---|---|---|
| | α-SER | Cosmic SER | Total SER | α-SER | Cosmic SER | Total SER |
| Chip B | | 1896 | | | | |
| Chip C | 153 | 734 | 887 | 0 | 285 | 285 |
| Chip D | 22 | | | 36 | 354 | 390 |

# TOPICS

- DEFINITIONS
- SOURCES OF RADIATION
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  - SEL AND MBU MITIGATION
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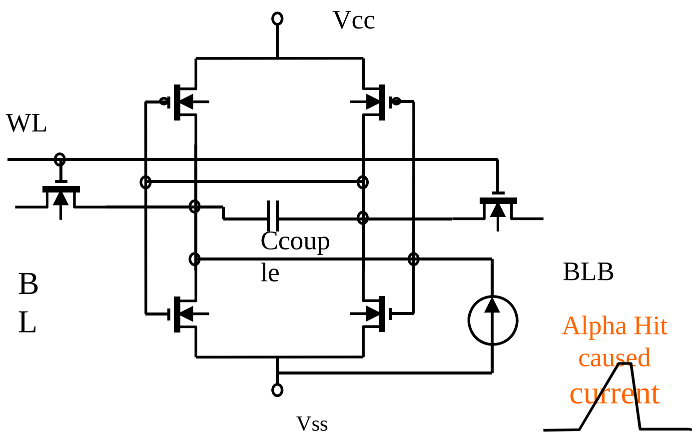
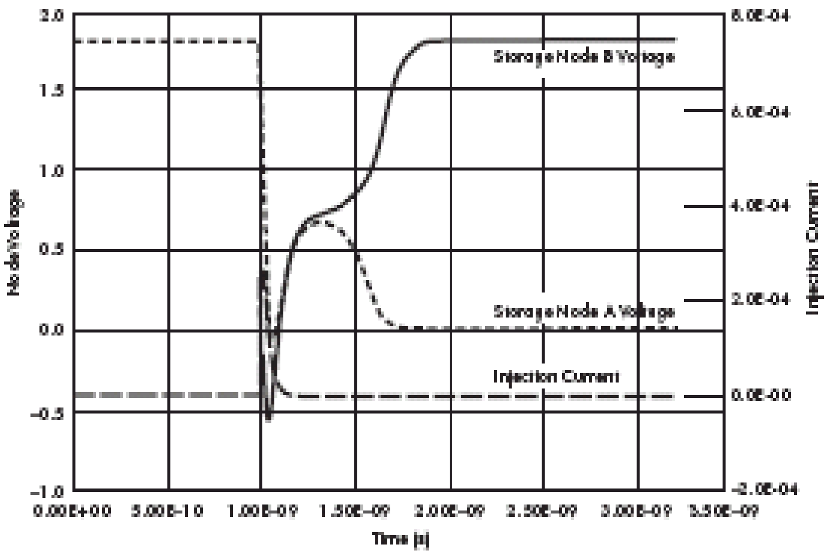
- **MODELING/SIMULATION OF SER**
- CYPRESS DATA
- CONCLUSIONS

# MODELING TECHNIQUES

- Compact Modeling
- Particle generated carrier are modeled as current pulse during circuit simulation
- Accurate R-C netlist of memory cell needed
- “Critical Charge” extracted by varying injected pulse amplitude and raise time until cell status flips

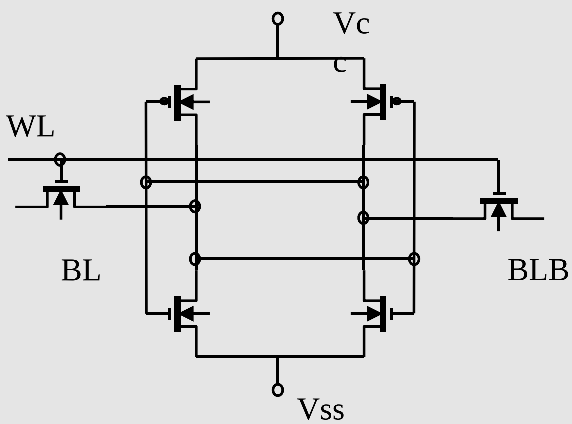


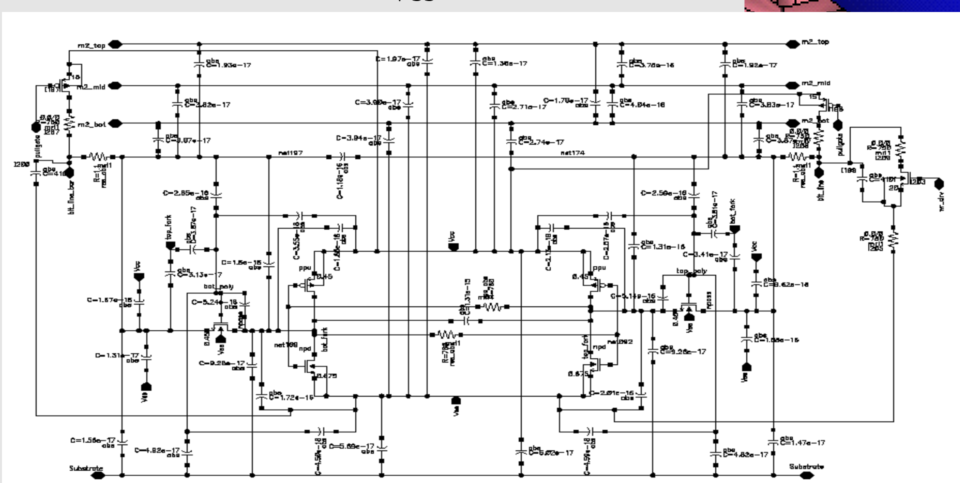

**Schematic set up of the 6T SRAM cell with an alpha particle hit**

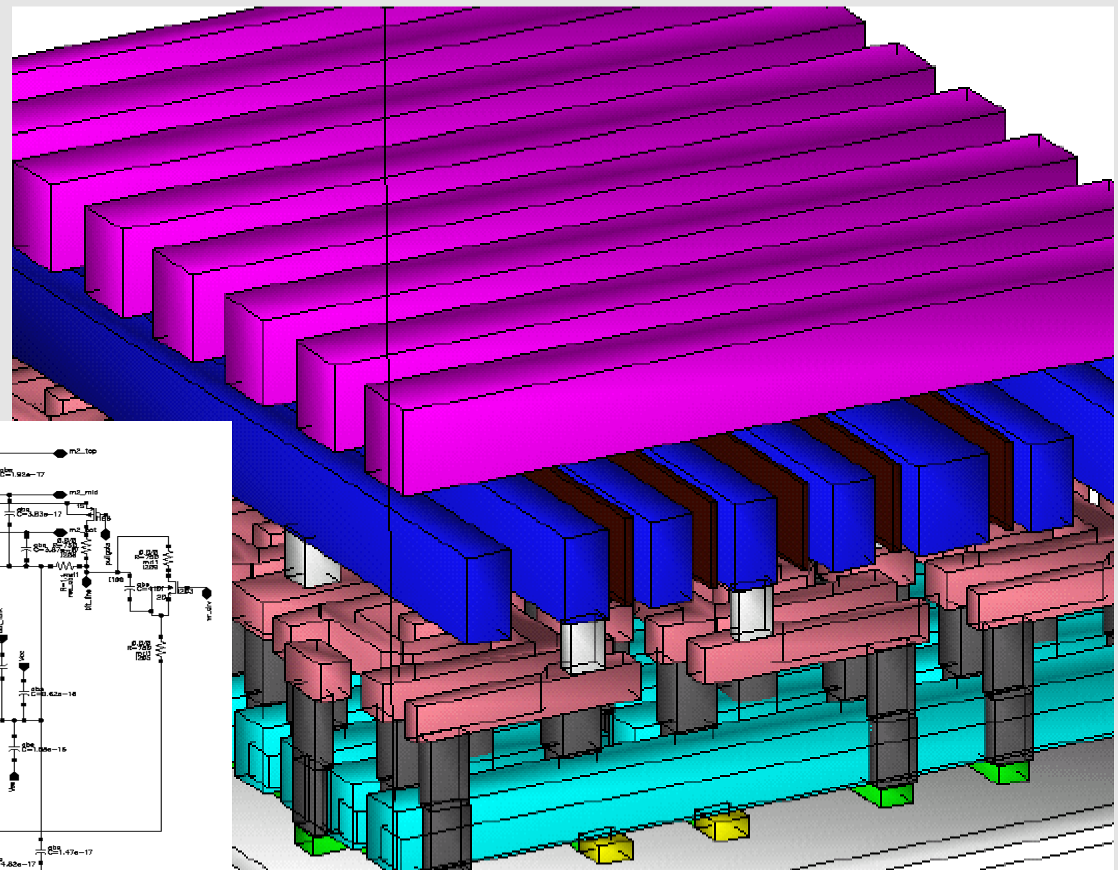


# CELL NETLIST

- Using 3D field solver to extract cell capacitances
- Manually assemble netlist including contact resistances



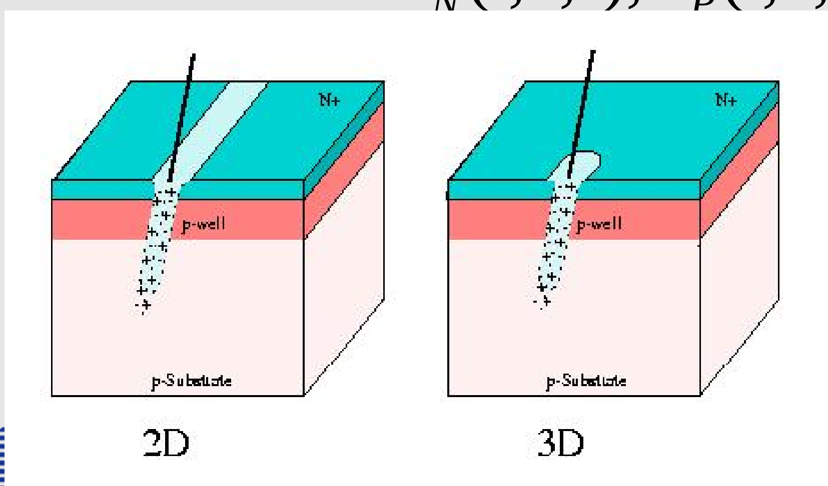





# TECHNOLOGY CAD MODELING

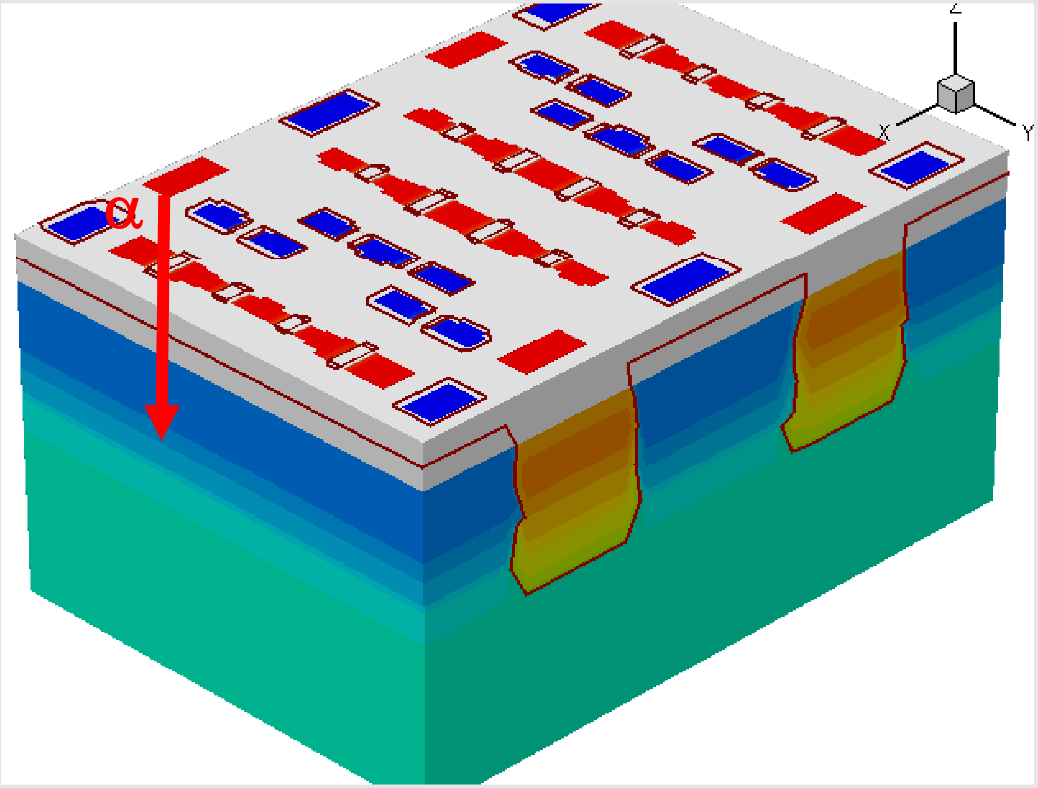
- Process and Device Simulation
- Simulate manufacturing process and electrical behavior using PDE’s and numerical integration scheme’s
- 2D and 3D possible depending on application
- Particle generated charge is modeled using photo-generation model

$$G_N(l,r,t), G_P(l,r,t) = C_1 \times e^{-(\frac{r}{r_0})^2} \times \frac{2e^{-(\frac{t-t_0}{t_c})^2}}{t_c\sqrt{\pi} \times erfc(-\frac{t_0}{t_c})}$$



# Full 3D SRAM Cell

- TCAD tools allow full 3D simulation of upset event

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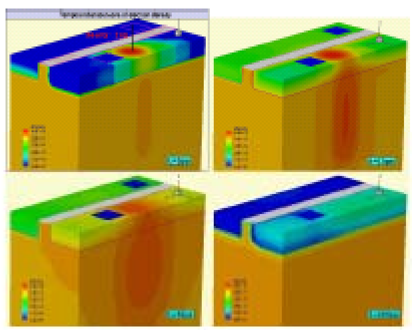
- RADSAFE – MC + TCAD + SPICE (Vanderbuilt)

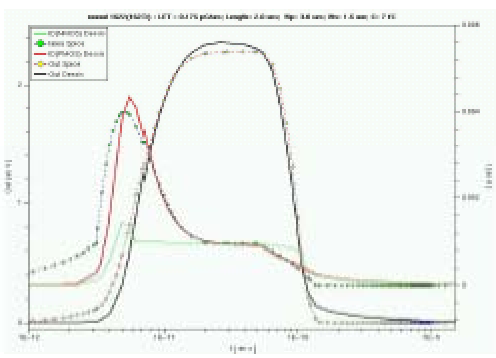
# FULLY INTEGRATED SER SOLUTION

**EVALUATION OF IRoC FULLY INTEGRATED SOLUTION – SoCFIT**

- CALIBRATION OF CELLS (SRAM, FF, LOGIC) THROUGH EITHER TCAD OR EXPERIMENTAL DATA
- PREDICTS MBU RATION AND SHAPE
- ALLOWS FOR SER FULL CHIP BUDGETING

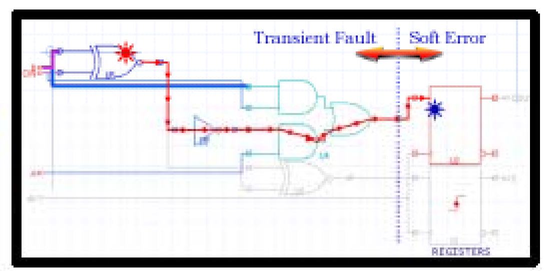


*T-CAD Simulations Model Generation*



*Spice simulations including SE*

*FIT calculation*




*SOC/System Analysis*

*Risk Reduction*

# TOPICS

- DEFINITIONS
- SOURCES OF RADIATION
- MITIGATION TECHNIQUES
  - SEL AND MBU MITIGATION
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- CONCLUSIONS

# CYPRESS SER TEST METHODOLOGY

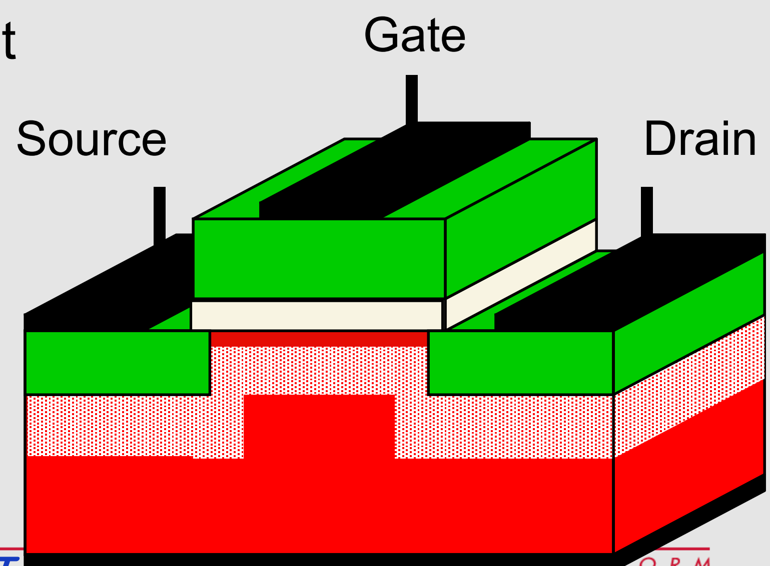
- Memory
  - Accelerated Alpha:
    - Th232 foil at 2mm open package, R/W checkerboard, different Vcc
    - SB and MB detection and analysis
    - SEL detection
  - Accelerated Neutron/Proton:
    - Utilizing Harvard Univ, TSL, TRIUMF, and LANL
    - Broad spectrum and mono-energetic beams
    - Correlation to NYC FIT rate base on Goldhagen group neutron distribution
    - SB and MB detection and analysis
    - SEL detection
  - System SER:
    - Mauna Kea, Colorado , and Manila
  - Thermal Neutron, X-Ray:
    - At request by DoD, Navy experiments

# SER TEST METHODOLOGY

- Logic + Memory: NSE
  - Accelerated Neutron/Proton
  - Accelerated Alpha not possible (Flipchip package)
  - SSER not possible (test to complicated, tester power consumption)
  - Logic test methodology customer dependent
- Logic SER:
  - Under development in community
  - Participate in JEDEC spec update
  - Not an issue until 45nm Technologies

# TECHNOLOGY SCALING TRENDS

- CMOS Technologies continue to shrink
- Impact on soft errors:
- Storage Node:
  - Supply voltage scaling: stopped at 65nm but degrades SER
  - Junction Capacitance: increases with shrinking technologies
  - Gate Capacitance: thickness decreasing (higher capacitance) however area scaling faster => overall reduction
  - Cell area shrink: lower X-section of hit




**SER vs. Technology:**

**=> Depends on combination of above factors**

# SER vs. TECHNOLOGY SCALING

- Cypress developed scaling model:
  - Vcc
  - SRAM cell capacitance
  - Critical N+ diffusion area (SENSITIVE VOLUME)

| Technology | Vcc V | kVcc | N+diff Area um2 | kndiff | Cell Size um2 | Node Capactitance fF | kcnode | SER Rate FIT/Mb |
|---|---|---|---|---|---|---|---|---|
| R7 | 2.25 | 0.67 | 0.09 | 1.25 | 2.94 | 2.25 | 0.79 | 1.17 |
| R9 | 1.50 | 1.00 | 0.07 | 1.00 | 1.22 | 1.77 | 1.00 | 1.00 |
| C9 | 1.45 | 1.03 | 0.04 | 0.65 | 0.95 | 1.76 | 1.00 | 0.83 |
| C10 | 1.26 | 1.19 | 0.03 | 0.42 | -- | 1.95 | 0.94 | 0.49 |

  - Continuous reduction in SRAM cell SER due to aggressive area shrink
  - Vcc scaling slowed down for 65nm Tech

# 90nm TECH SER BENCHMARK

| Technology (Vcc) | Splits | Alpha SER | Cosmic N SER | System SER | N-SEL |
|---|---|---|---|---|---|
| R5 62146 0.25um 4M | Standard | NA | 375 (LANL) | NA | 0 |
| Samsung 0.18u 18M | | 104 | 780 | 401 | <10 |
| R7 18M 1372C (2.5V) | Standard | 246 | 734 | 255 | <10 |
| TSMC 0.09u | Standard | NA | 300 | NA | NA |
| R9 9M 1356C (2.5V) | Standard, Latchup pFET | 190 | 210 | 241 | 0 |
| Samsung 0.13u QDR | Standard | NA | 220 | NA | NA |
| R9 72M 1472A (2.5V) | Standard | 250 | 394(LANL) | 241 | 0 |
| R9 72M 1513A (1.8V) | Standard, Latchup pFET | 144 | 200 | 241 | 0 |
| C9 1M 1021D (1.32V) | Standard, Latchup pFET | NA | 222 (LANL)<br>195 (TSL) | NA | 0 |
| R9 72M 1513A (1.8V) | Standard, Latchup pFET | 144 | 200 | 133* | 0 |

**N-SEL: Tested @ >150MeV Neutron/Proton Labs**
**Unit – FIT/Mbit scaled to NYC**

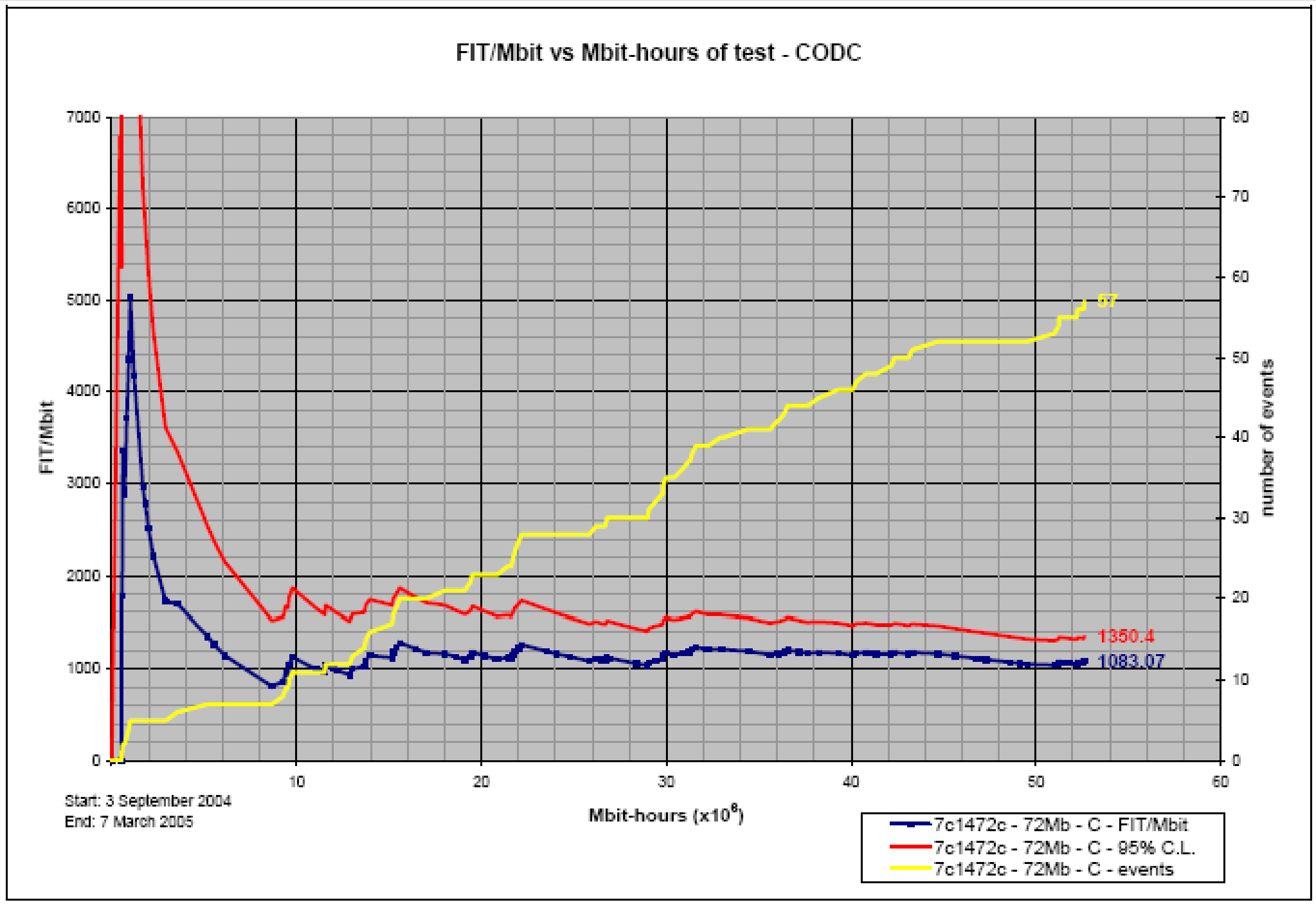
- Best in Class SER Neutron FIT rate 195FITs +- 10%

# SRAM SYSTEM SER TESTING

- Hundreds of devices are mounted on a system and accessed serially.
- Typically each device is accessed every 4 hours.
- Currently the systems are installed at Cypress Colorado Design Center and Mauna Kea, Hawaii.

# R9 SSER QUALIFICATION DATA

- Tested in Cypress Colorado from 3-Sep-04 to 7-Mar-05
- 214pcs of 72M R9; 730,941 device-hours collected
- Failure rate in Colorado is 1083 FIT/Mb
- Avg. Failure rate in NYC is 246 FIT/Mb




Picture #1 – SSER (FIT/Mbit) versus test hours, and number of errors versus test hours.



PERFORM

# ALPHAS vs. NEUTRONS

160nm SRAM SSER data collected at CML and CODC

SSER= nSER + αSER + ~~$n_{TH}$SER~~ ← zero (no BPSG)

Conclusion: significant (231/576) contribution from Alphas

**2. Conclusions**

The failure rate (FIT/Mbit) measured at CML is reported below:

| | Test time | | SEU | | | SEL | | |
|---|---|---|---|---|---|---|---|---|
| Device | Mbit-hours | Device-hours | Events | FIT/Mbit | | Events | FIT/Mbit | |
| | | | | Average | 95% C.L. | | Average | 95% C.L. |
| CY7C1372B | 18,588,583 | 1,032,699 | 24 | 1,291 | 1,816 | 1 | 54 | 255 |
| CY7C1372C | 21,188,643 | 1,177,147 | 9 | 425 | 741 | 0 | 0 | 141 |

Table #1 – Summary data for the SSER at CML (Jun 18-Nov 24 2003)

The failure rate (FIT/Mbit) measured at CODC is reported below:

| | Test time | | SEU | | | SEL | | |
|---|---|---|---|---|---|---|---|---|
| Device | Mbit-hours | Device-hours | Events | FIT/Mbit | | Events | FIT/Mbit | |
| | | | | Average | 95% C.L. | | Average | 95% C.L. |
| CY7C1372B | 26,720,255 | 1,484,459 | 138 | 5,165 | 5,948 | 1 | 37 | 178 |
| CY7C1372C | 34,474,913 | 1,915,273 | 57 | 1,653 | 2,061 | 0 | 0 | 87 |

Table #2 – Summary data for the SSER at CODC (Jan 14-June 27 2004)

| Device | α Average | n @ CODC Average | n @ CML Average | n @ NYC Average | SSER @ NYC Average |
|---|---|---|---|---|---|
| CY7C1372B | N/A | N/A | N/A | N/A | N/A |
| CY7C1372C | 231 | 1,422 | 193 | 324 | 555 |

CYPRESS PERFORM

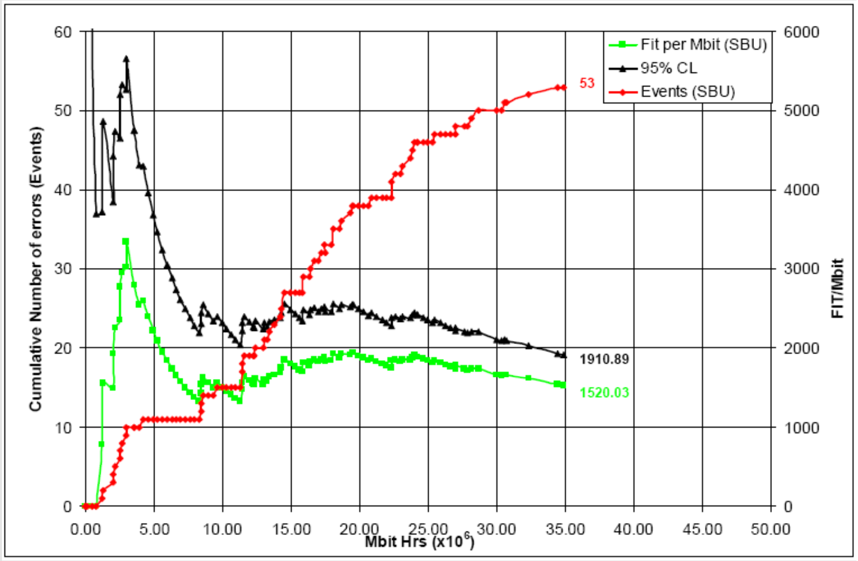
# SYSTEM SER HIGH ELEVATION

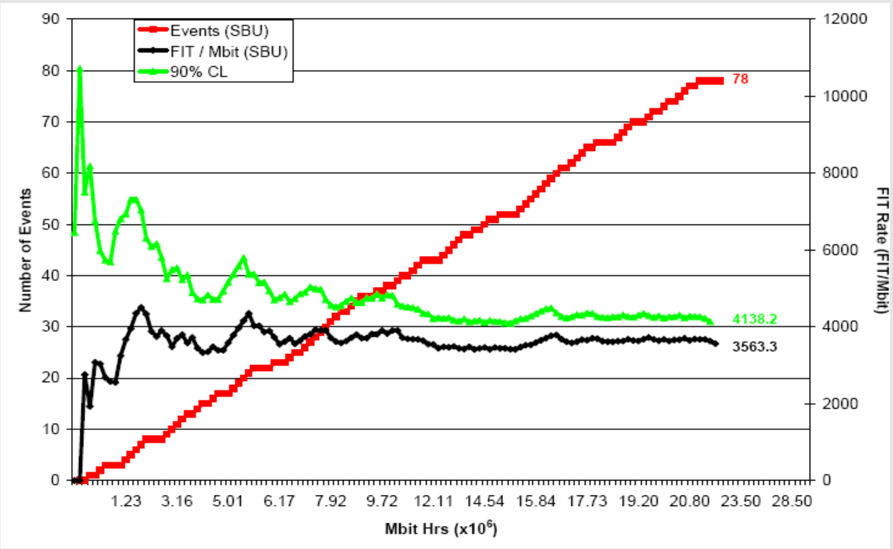
## Colorado: 386x 36M SYNC

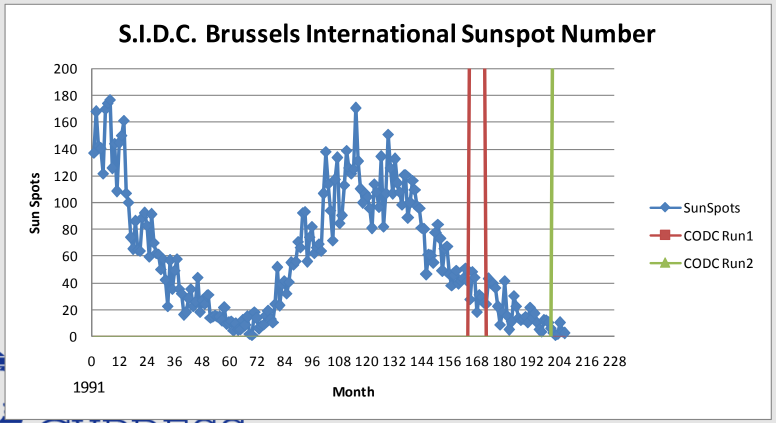
- 4.3x Acceleration over NYC
- Test Time: Sept07-Mar08
- 5.1 Gb.yrs/1.24M device hrs completed
- Current FIT rate: 326 FIT/Mb
- Elevated FIT rates due to Solar Cycle (close to 0% activity)

## Mauna Kea: 1100x 16M MoBI

- 9.22x Acceleration over NYC (13.7kft)
- Test Time: Dec07-May08
- 1.72 Gb.yrs/944k device hrs completed
- Current FIT rate: 373 FIT/Mb



# NEUTRON FLUX 2004-2008

90nm SRAM SSER 72M was measured 09/04-03/05 in CODC

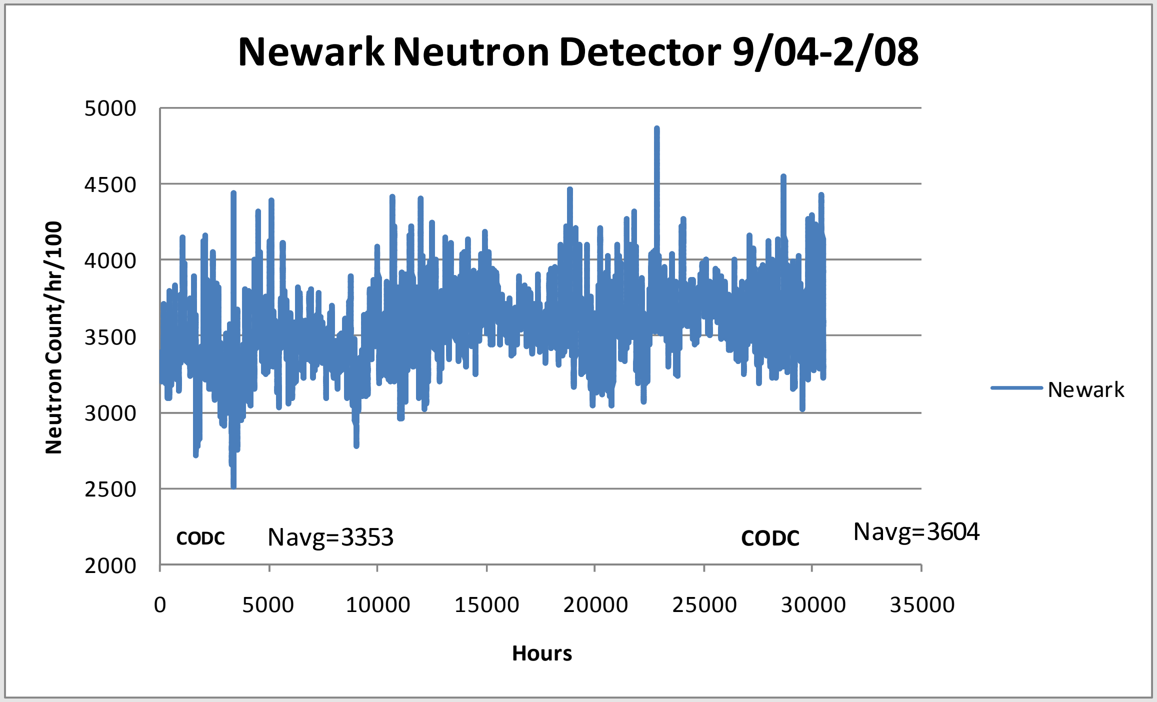
90nm SRAM SSER 36M was measured 09/07-03/08 in CODC

- Cosmic ray flux depends on:
  - Solar Activity
  - Barometric Pressure

Average Neutron Rate during the measurement periods:

- 09/04-03/05: 3353
- 09/07-02/08: 3604

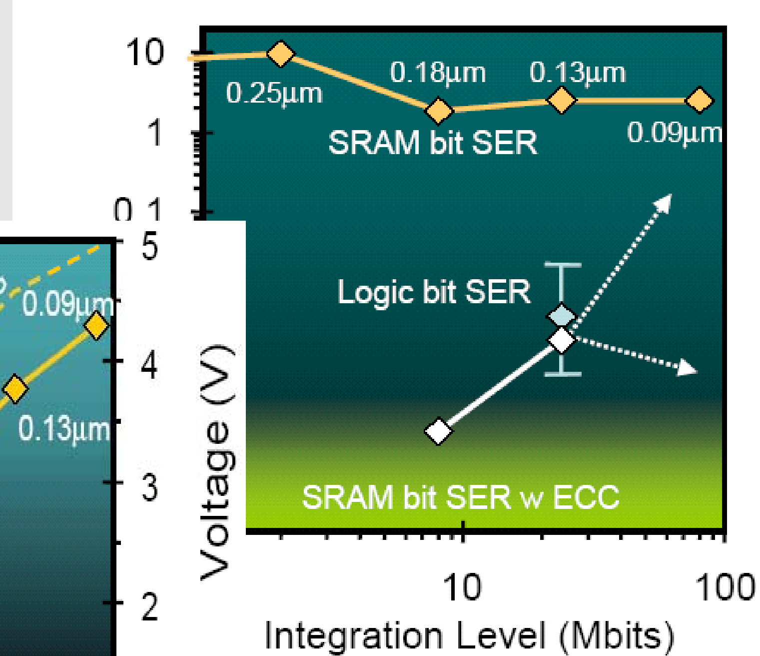
SSER NYC failure rate needs to be corrected for the solar activity



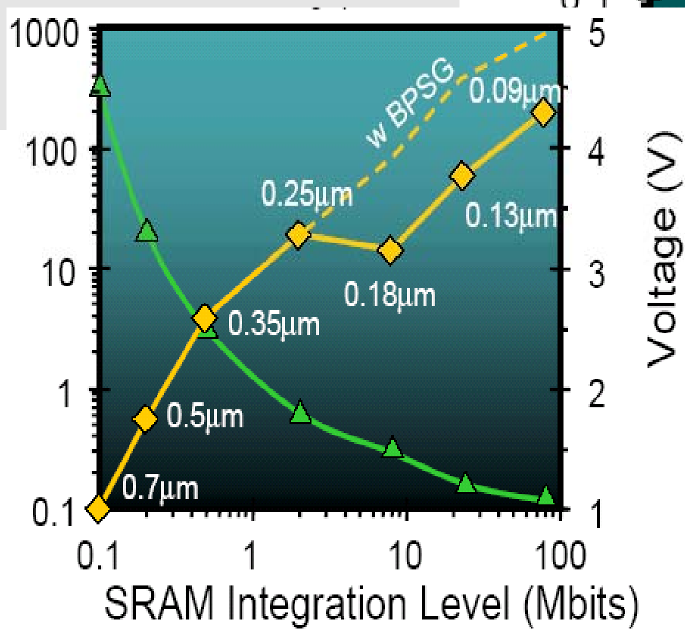
# SER TRENDS

- •System SER is increasing
- •Logic SER is catching up

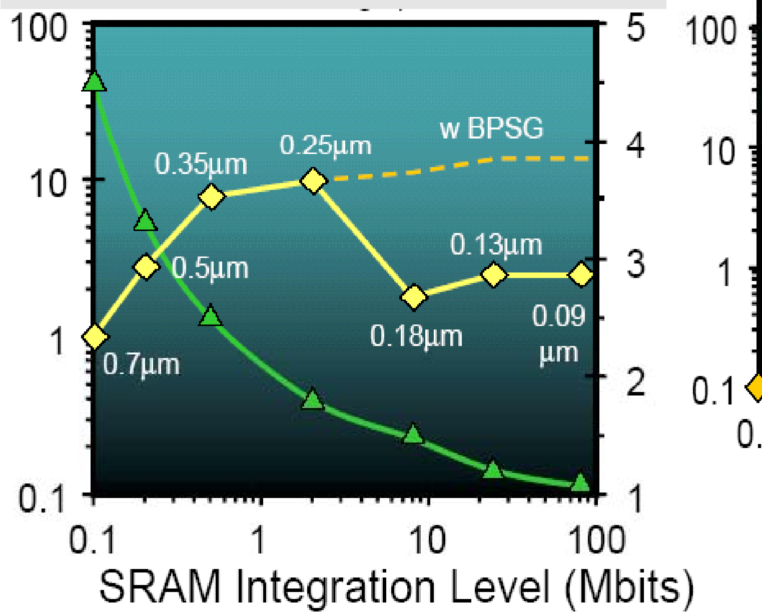
Logic SER




System SER




SRAM




R.Baumann, TI

# CONCLUSIONS

- Presented overview of Soft Error:
  - Definitions
  - Upset mechanisms
  - Mitigation Techniques
  - Measurement Techniques
  - Modeling Techniques
  - Benchmark Data and System Data
  - Outlook

**Any questions: serquestions@cypress.com**

# SER-History, Trends and Challenges

- Ch1 – *Historical Perspective* - The chapter reviews the last 30 years of how soft-fails have impacted the semiconductor industry.
- Ch2 – *Evaluating Chip SER* - The chapter summarizes the various methods to evaluate the soft- error rate (SER) of chips.
- Ch3 – *Soft Errors from Alpha Particles* – Detailed evaluation of alpha particle effects on chips and methods to mitigate these effects.
- Ch4 – *Terrestrial Cosmic Rays* – A scientific review of cosmic radiation at sea level and terrestrial sites, and the expected variations.
- Ch5 – *Soft Errors from Thermal Neutrons* – A review of the specialized soft fails which can occur from thermal neutrons.
- Ch6 – *Process Techniques to Minimize Chip SER* – Methods of enhancing chip resistance to soft fails from process changes in manufacturing.
- Ch7 – *Evaluating SER using Life Testing* – Review of extensive Cypress experience in evaluating chips SER in the natural environment.
- Ch8 – *Modeling Chip SER from Alpha Particles* - The chapter shows how to model chip sensitivity to alpha particles from fundamental principles.
- Ch9 – *SER from the OEM Perspective* – Complex computer products must be designed to operate reliably even with possible errors so they do not impact system performance.
- Ch10 – *High Reliability Systems: Implantable Medical Electronics* – A review of the critical application of implantable chips (in people), in which soft errors can have the most serious consequences.