

2008 ITRS Update Highlights

IEEE Santa Clara Chapter
Tuesday, 02/10/09

Rev 2.1 (added ITRS logo and source note)



2007-08 - 10th Anniversary of ITRS!

<http://www.itrs.net> [*incl. Public Presentations]

1991
Micro Tech 2000
Workshop Report

1992NTRS

1994NTRS

1997NTRS

Europe

Japan

Korea

Taiwan

USA

1998ITRS
Update

1999ITRS

2000ITRS
Update

2001ITRS

2002ITRS
Update

2003ITRS

2004ITRS
Update

2005ITRS

2006ITRS
Update

*2007ITRS

2008ITRS
Update



Agenda

- Pre-Summary
- Moore's Law and More
- Technology Pacing Trends Update
 - Physical and Printed GL Focus in 2008 Update
- Some TWG Highlights
- Summary

- Backup
 - Design On-Chip Frequency
 - SICAS Technology, Wafer Generation Demand Update
 - “More Moore” and “More than Moore” Definitions Update



2008 ITRS Update Highlights Pre-Summary

- 2007-08 ITRS 10th Anniversary!
- Technology Trends Revised – Major adjustment to Printed and Physical Gate Length plus TWG survey warnings of more to come in 2009 (DRAM 4F2, MPU SRAM)?
- “Equivalent scaling” technology substituting for classic dimensional gate length and oxide thickness scaling
 - Copper interconnect, strained silicon, Hi-K, Metal Gate technologies, etc. providing potential solution options for historical dimensional scaling of gate length and equivalent oxide thickness (EOT)
 - Availability of more process technology options has allowed the advancement of transistor performance, but also met requirements for lower power
- “Moore’s Law” is still on track
 - Lithographic capabilities have enabled the scaling of half-pitch ($\sim 0.7x$ /generation) on ITRS trends
 - Multi-Level-Cell (MLC) Memory storage (Flash) “Equivalent scaling” also contributed to memory density, including 4 bits/cell MLC added in 2007
- 2009 Roadmap work needed for PIDS and FEP and Design cross-TWG to correlate device properties to actual product performance (which was historically keyed off of dimensional gate length and EOT)



2008 ITRS Update Highlights Pre-Summary (cont.)

- Design and System Driver Providing More Roadmap Detail and Framework for Application Needs and cross-TWIG “equiv. scaling” Potential Solutions
- PIDS tables adapted to new Gate Length trends, plus Transistor “equivalent scaling” Modeling Required in 2009 for Performance and Power Options
- Litho Technology Potential Solution options updated/narrowed
- Interconnect Low-k targets renegotiated to match delayed solutions
- A&P tables adjusted to adapt to accelerated 3-D SIP and 3D Interconnect implementations
- Metrology – Ongoing CD and Overlay Variability and Measurement Challenges
- FI - Guidance for 300mm and 450mm Next Generation Factory Performance and Productivity Needs are Addressed
- ESH - Key Focus on Management of Resources
- ERD/ERM complete workshops to prioritize “Beyond CMOS” “information processing” potential solutions, and included new Definitions in the Glossary
- Additional Details Available in Online Roadmaps and Public Presentations at www.itrs.net ; http://www.itrs.net/Links/2008ITRS/Update/2008_Update.pdf
- Future Fab 2008 ITRS special edition articles also online and linked at: www.itrs.net to <http://www.future-fab.com/welcome.asp>



2007 ITRS Executive Summary Fig 5

[2008 –

Moore's Law & More

Update Definitions]

Traditional
ORTC Models

Functional Diversification (More than Moore)

Facilitator:
Europe IRC

Analog/RF HV Power Passives Sensors Actuators Biochips

Scaling (More Moore)

[Geometrical & Equivalent scaling]
Baseline CMOS: CPU, Memory, Logic

130nm
90nm
65nm
45nm
32nm
22nm
...
V

Information Processing

Digital content
System-on-chip (SoC)

Interacting with people
and environment

Non-digital content
System-in-package (SiP)

Continuing SoC and SiP: Higher Value Systems

Facilitator:
USA IRC

Beyond CMOS

Facilitator:
ERD/ERM ITWG

SIP "White Paper"
A&P ITWG
[www.itrs.net/
papers.html](http://www.itrs.net/papers.html)



2007/08 ITRS “Moore’s Law and More” Alternative Definition Graphic

**Baseline
CMOS**

Memory

RF

**HV
Power**

Passives

**Sensors,
Actuators**

**Bio-chips,
Fluidics**

“More Moore”

“More than Moore”

Computing &
Data Storage

Sense, interact,
Empower

Heterogeneous Integration

System on Chip (SOC) and System In Package (SIP)



Source: ITRS, European Nanoelectronics Initiative Advisory Council (ENIAC)

New 2008 ITRS “Beyond CMOS” Definition Graphic

Baseline CMOS *Ultimately Scaled CMOS* *Functionally Enhanced CMOS*

Nanowire Electronics *Ferromagnetic Logic Devices* *Spin Logic Devices*

32nm

22nm

16nm

11nm

8nm

Multiple gate MOSFETs

Channel Replacement Materials

Low Dimensional Materials Channels

“More Moore”

New State Variable

New Devices

New Data Representation

New Data Processing
Algorithms

“Beyond CMOS”

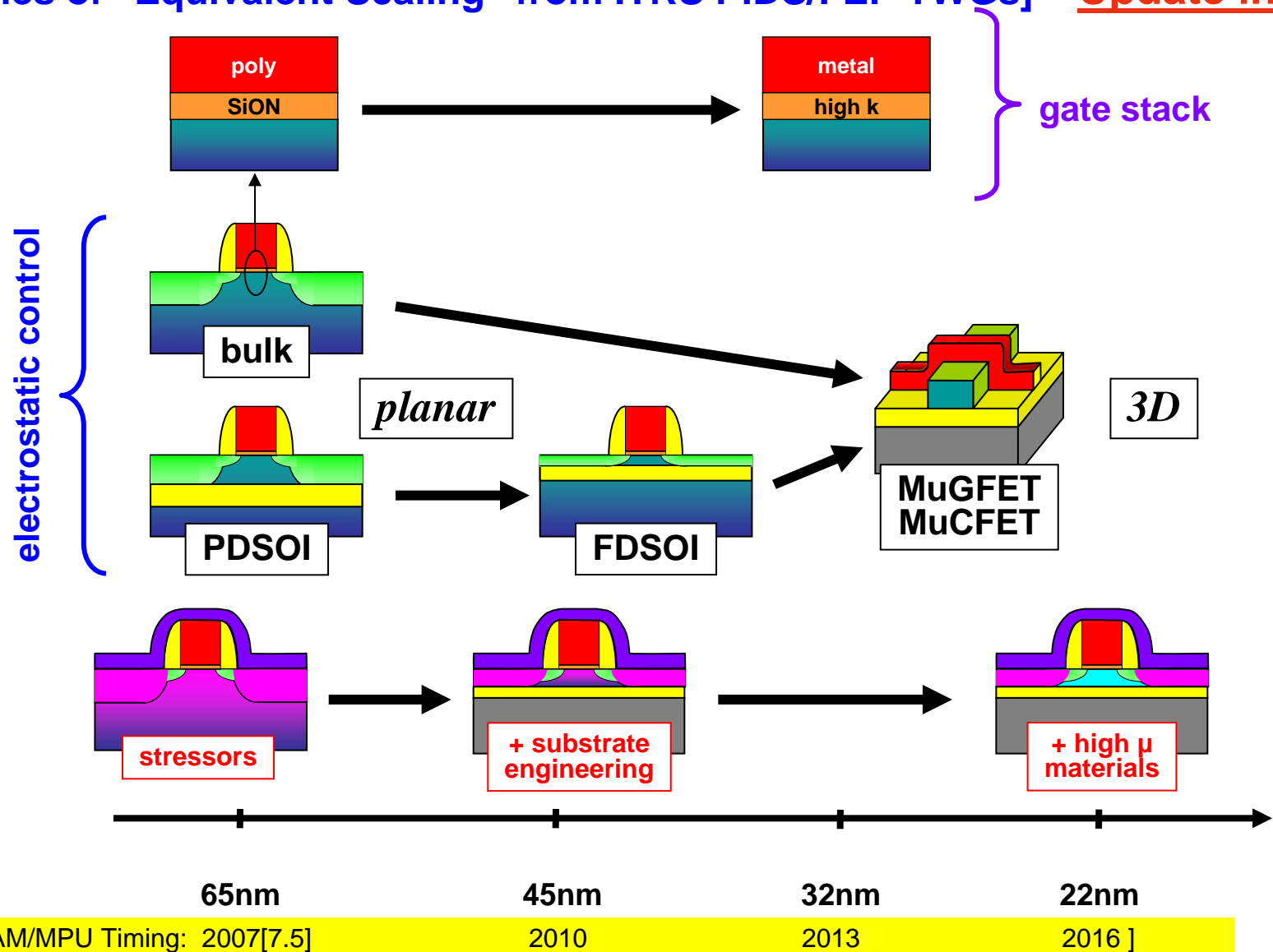
Computing and Data Storage Beyond CMOS

Source: Emerging Research Device Working Group



2007/08 - PIDS/FEP - Simplified Transistor Roadmap

[Examples of "Equivalent Scaling" from ITRS PIDS/FEP TWGs] – Update in 2009



[ITRS DRAM/MPU Timing: 2007[7.5]

2010

2013

2016]

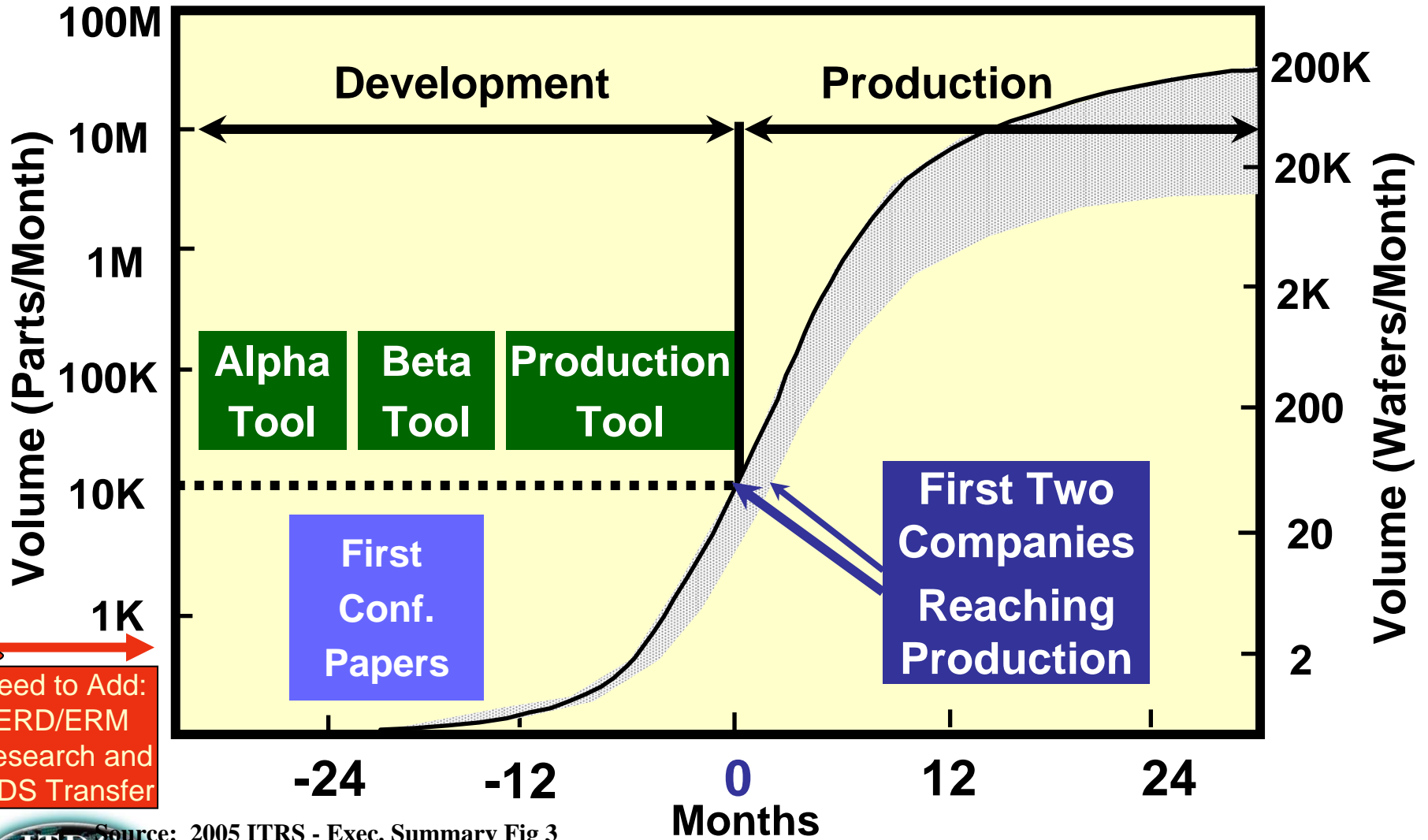


Source: ITRS, European Nanoelectronics Initiative Advisory Council (ENIAC)

Fig 3

2008 - Unchanged

Production Ramp-up Model and Technology **Cycle Timing**



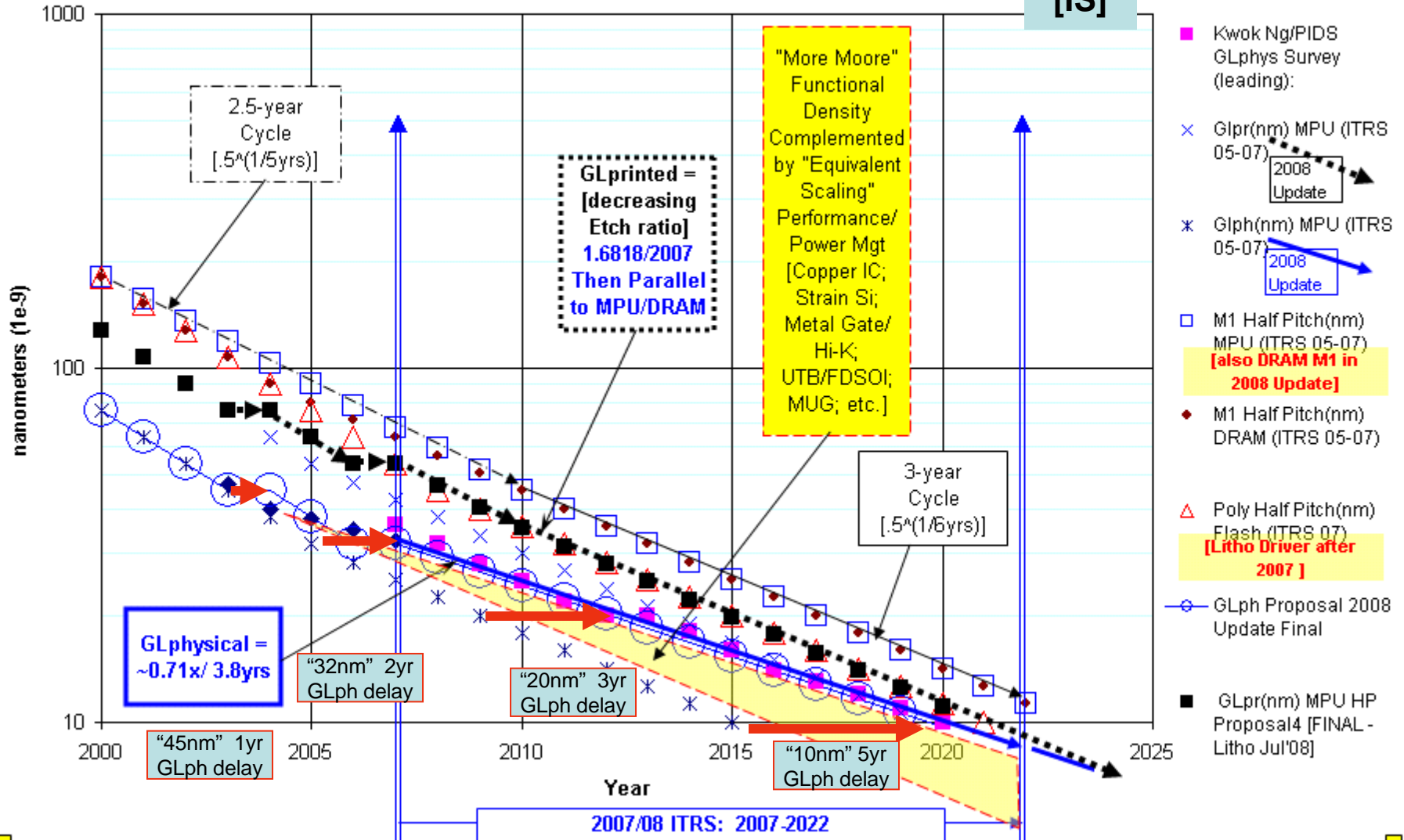
Need to Add:
ERD/ERM
Research and
PIDS Transfer



Source: 2005 ITRS - Exec. Summary Fig 3

2008 ITRS Update - Technology Trends vs Actuals and Survey [including Final Litho Printed Gate Length Proposal]

[IS]



- GLphysical 2008 Update IS: 3.8yr cycle after 2007; enabled by "Equiv. Scaling"
- FEP and PIDS have proposed shifted/interpolated tables; full model redo in '09
- GLprinted parallel to MPU/DRAM M1 Half-Pitch; shrinking etch ratio to GLphy



Performance and Power Management Enabled by "Equivalent Scaling"

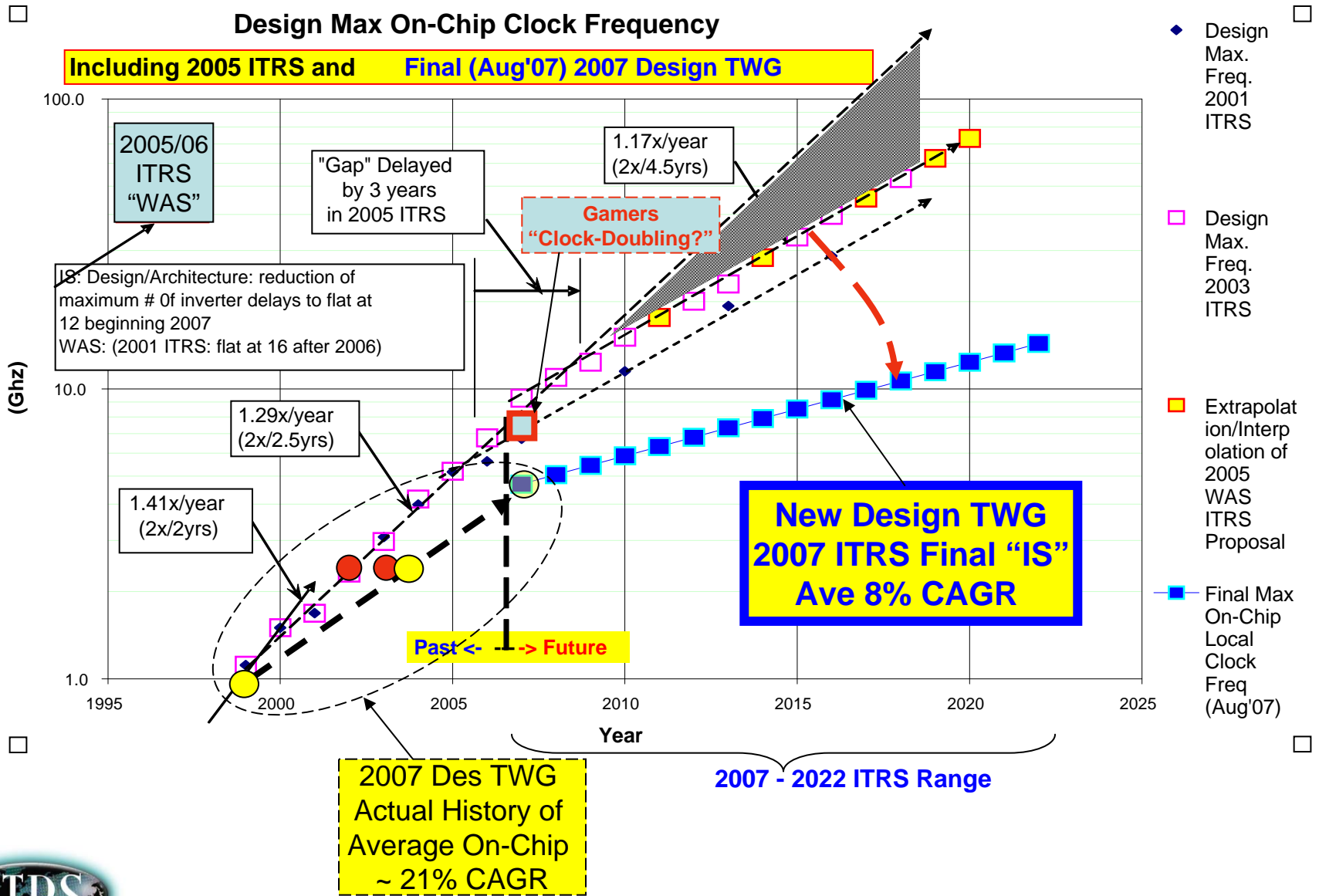


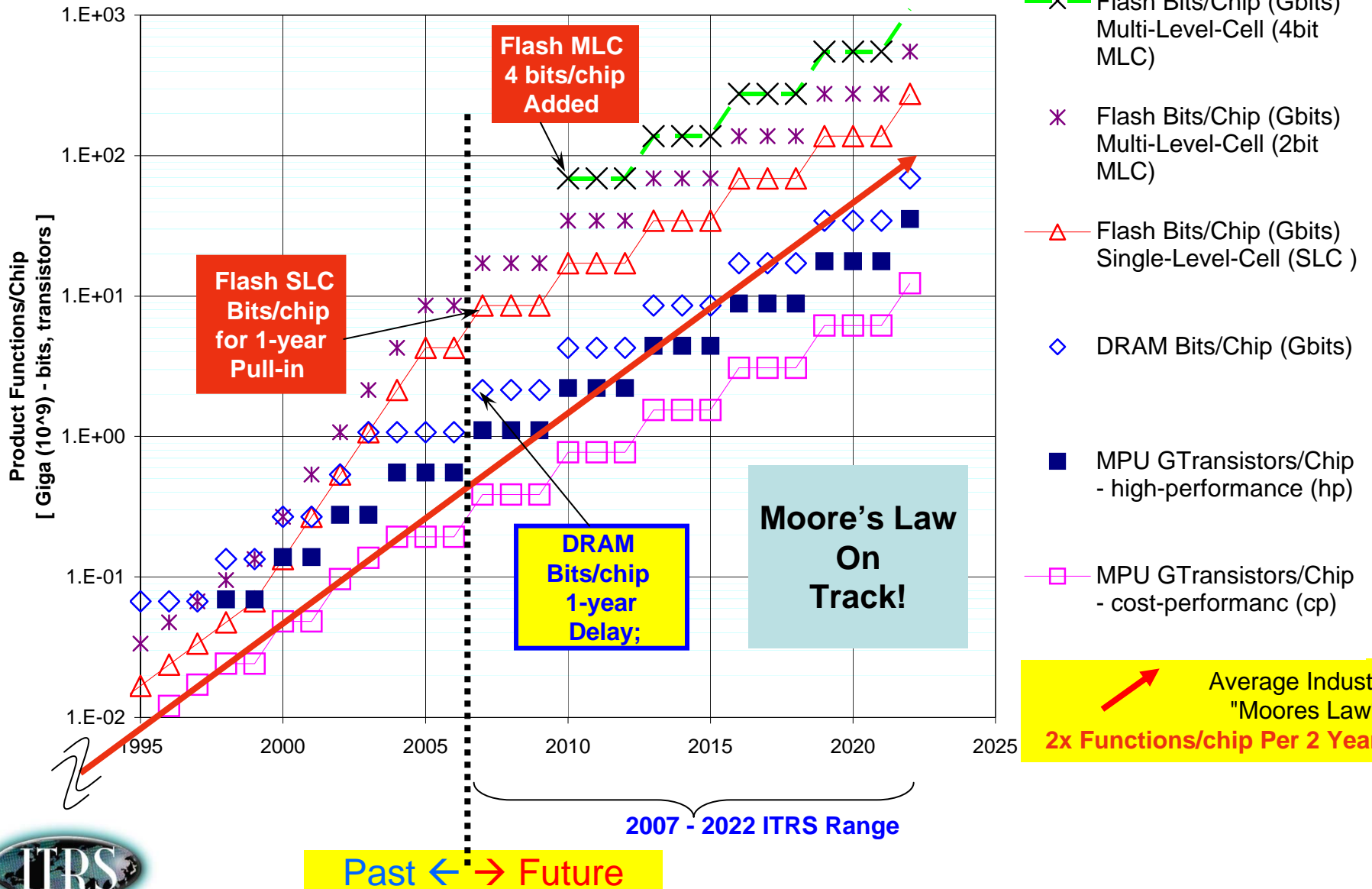
Figure 10 ITRS Product Functions per Chip

[MIT "Moore's Law" Article:

<http://www.technologyreview.com/computing/21901/?a=f>]

[Unchanged for 2008]

Functions per Chip



ORTC Summary – 2008 Update Status

✓ Flash Model un-contacted poly half-pitch trend

- **Unchanged** 2-year cycle* through 2008/45nm, then 3-year cycle* (2014/22.5; 2020/11.25); ;
- **Unchanged:** Cell Design Factor; Array Efficiency; Bits/Chip
- PIDS Flash Survey Team to report status of survey data update and proposals in July meetings.

✓ DRAM Model stagger-contacted **M1 half-pitch updated to the MPU 2.5-year cycle* through 2010/45nm [affects 2007, 2008, 2009], then**

- **Unchanged** 3-year cycle* beginning 2010/45nm (2016/22.5; 2022/11.25);
- **Unchanged:** Cell Design Factor; Array Efficiency; Bits/Chip

✓ DRAM function size, function density, and chip size models have been updated to latest Product 2.5-year cycle scaling rate;

- **Only 2007-2009 years affected** in 2008 Table Update.
- **Unchanged 2010-2022**

✓ MPU Model M1 stagger-contact half-pitch **unchanged** from 2007

- 2.5-year cycle* through 2010/45nm, then 3-year cycle* (2016/22.5; 2022/11.25).

• MPU/ASIC Printed Gate Length Updated

- 1.6818 Etch Ratio in 2007;
- Then variable Gpr/Gphy Etch Ratio (parallel to DRAM/MPU M1 Contacted Half Pitch) '07-'22).

• MPU/ASIC High-Performance Physical Gate Length

- 3.8-year cycle* beginning 2007; Performance and Power needs managed by mixing “equivalent scaling” process technology insertions with traditional dimensional scaling
- FEP and Litho TWGs have agreed on new annual variable GLprinted/GLphysical ratio targets
- Slower On-Chip Frequency trend (**8% trend**) was set by Design TWG in 2007 ITRS ORTC) - **need updated transistor and design model alignment by PIDS, FEP, and Design – 2009 Renewal.**
- **New drivers will be Ion/Width, CV/I – possibly add to ORTC - 2009 Renewal ORTC line items.**

* ITRS Cycle definition = time to .5x linear scaling every two cycle periods]



ORTC Summary – 2008 Update Status (cont.)

- **MPU/ASIC Low Operating Power Printed Gate Length**
 - Delay paced from new 2008 MPU High Performance Printed Gate Length
 - **MPU/ASIC Low Standby Power Physical Gate Length [add to ORTC 1a,b]**
 - No Change in years 2007, 2008; two-year delay 2009-2011 from High Performance; one-year delay in 2012; and no delay 2013-2022.
 - **New Linked Excel Table Format for ORTC and TWG Tables in the 2008 Update**
-
- **New 2008 “Moore’s Law and More” Working Groups and Definitions Work (see backup slides – Glossary updates) :**
 - **“More Moore”** (“Moore’s Law;” typically digital computing) Functional and Performance scaling is enabled by both “Geometrical” and also “Equivalent” scaling technologies; **Design “Equivalent Scaling” added in 2008**
 - **More than Moore “Functional diversification” text will be impacted** (typically non-digital sensing, interacting) system board-level migration/miniaturization is enabled by system-in-package and system-on-chip (also note: A&P SIP white paper at www.itrs.net/papers.html)
 - **“Beyond CMOS” definition will be added, focused on the Computing and Storage Logic Switch transition and consensus options at “Ultimately Scaled CMOS”**
 - The average of the industry product **“Moore’s Law”** (2x functions/chip per 2 years) **rate forecast to continue** throughout the latest 2007-2022 ITRS timeframe
 - The **Semiconductor Industry Capacity Analysis Statistics (SICAS 2Q08 – www.sia-online.org)** **“<80nm” Capacity** and **300mm Capacity Demand** have both ramped to **over 40%** of Total MOS
 - Industry **<80nm Technology and 300mm Capacity Demand capacity (as of 2Q08 status) is 95% utilized (see backup slides – SICAS Updates)**



Some TWG Highlights

- Design and System Drivers
- PIDS
- Lithography
- Interconnect
- A&P
- Metrology
- Factory Integration
- ESH
- ERD/ERM



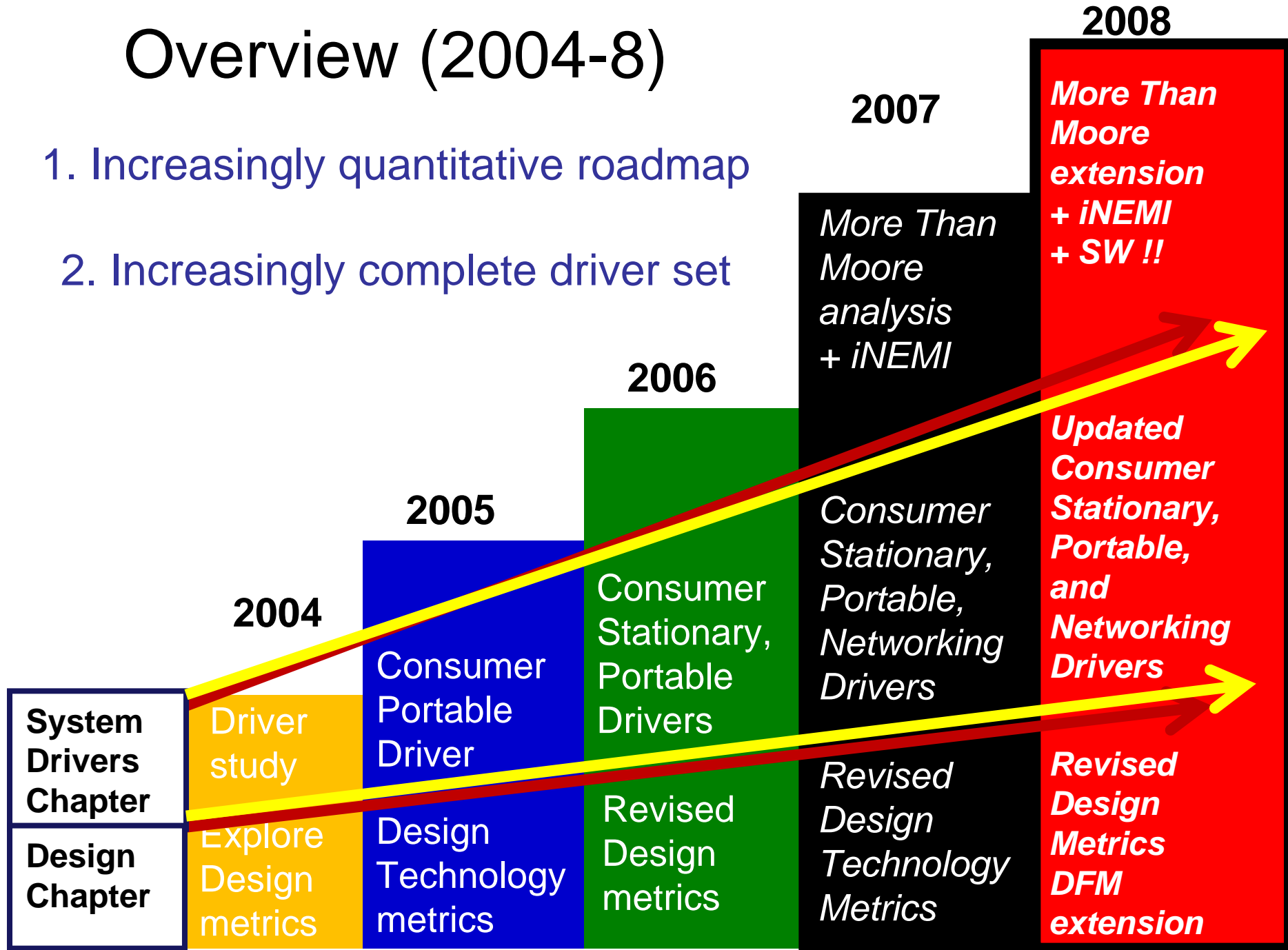
2008 TWG Highlights – Design and System Drivers

- Confirmed software as an integral part of semiconductor products, and software design productivity as a key driver of overall design productivity.
 - Included additional rows in the tables for system-level design;
 - Highlighted how productivity growth can only be ensured with heavy use of special purpose multi-core architectures.
- Started analyzing what specific design technologies enable viable manufacturing technology control requirements (ie CD control), and in what amount,
 - Impact analysis to be complete next year.



Overview (2004-8)

1. Increasingly quantitative roadmap
2. Increasingly complete driver set



2008 TWG Highlights – Process Integration, Devices and Structures (PIDS) TWG

- Incorporate the new physical gate length (L_g) scaling models adopted by the ORTC
 - In response to recent PIDS survey results and the reverse-engineering findings. These new scaling models slow down the L_g scaling compared to those in the 2007 ITRS.
- Because of this, the speed scaling of 17% per year in the HP Technology CV// is relaxed. Accordingly, the introduction of UTB FD and DG structures are also assumed to delay.
- Ultra-thin-body (UTB) Fully Depleted (FD) structures start in 2013;
- Double Gate structures start in 2015, for all High Performance (HP), Low Operating Power (LOP), and Low Standby Power (LSTP) technologies.
- Shifted the starting of high-k/metal gate from 2008 to 2009 to reflect delay of 2nd company (ITRS timing guideline).



PIDS 2008 Update (cont.)

- Japan PIDS team provided survey on L_g (physical gate lengths) for HP, LSTP, and LOP logic devices, along with reverse-engineering data from FEP, helped to establish new slowed-down scaling model.
- 2008 update adopts new L_g rules proposed by ORTC.



PIDS 2008 Update (cont.)

- HP and LOP devices using new L_g rules. LSTP devices remain same.
- Data entries are based on “interpolation” of 2007 data.
First 3 years are re-calculated by MASTAR.
- Some “bumps” in first ~3 years, due to merging of 2005 & 2007 tables.
- UTB-FD and DG follow delay of L_g rules.



PIDS 2008 Update - 2009 Work outlook

- MASTAR calculation on $CV//$ to replace values obtained from interpolation in 2008 tables.
- Consider new speed metric using ring oscillator or inverter.
- Consider equations to derive new speed metric above, in addition to MASTAR.
- Incorporate new speed scaling factor smaller than 17%/year.



2008 TWG Highlights – Lithography TWG

- All of the Lithography requirements have been updated to reflect the new product based half pitch requirements and the new time physical gate length for MPU products.
 - Drivers all of the values that are based on Half Pitch and Gate Length have been changed based on the previously established equations.
 - New product based spit is shown in the Lithography Technology Requirements table.
 - Other tables are driven off of the hardest specifications associated with the lithography requirements. (In most cases this means the MPU gate CD requirements.)
- Color changes reflect the relaxing of the MPU gate CD and the improvement that have been achieved in the industry.

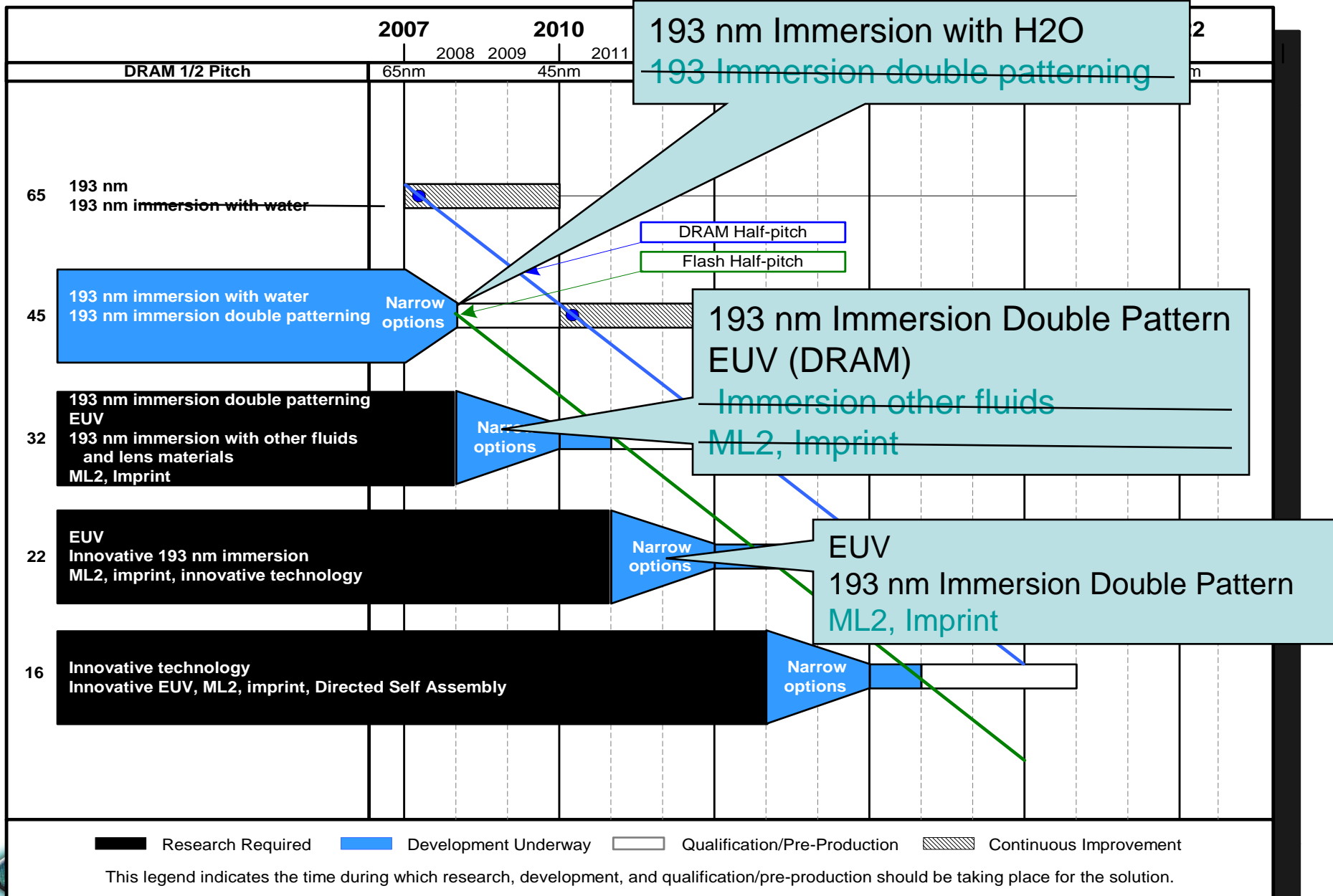


Litho 2008 Update (cont.)

- Lithography potential solutions are being narrowed for 45nm DRAM half-pitch
 - CoO is Driving 193 Immersion Single Exposure
 - 2009 update will be major decision point for 32nm DRAM half-pitch (Double Patterning or EUV)
- LER and CD Control Still remain as a Dominant Issue
- Relief on some near term specifications but imaging challenges remain
 - Flash pushing Half Pitch and Double Patterning
 - Overlay requirements for the Dependent Geometry will remain the challenge
 - Contact Imaging Remains a challenge for all device types
- Double exposure / patterning requires a complex set of parameters when different exposures are used to define single features



Litho Potential Solutions 2008 - 2009

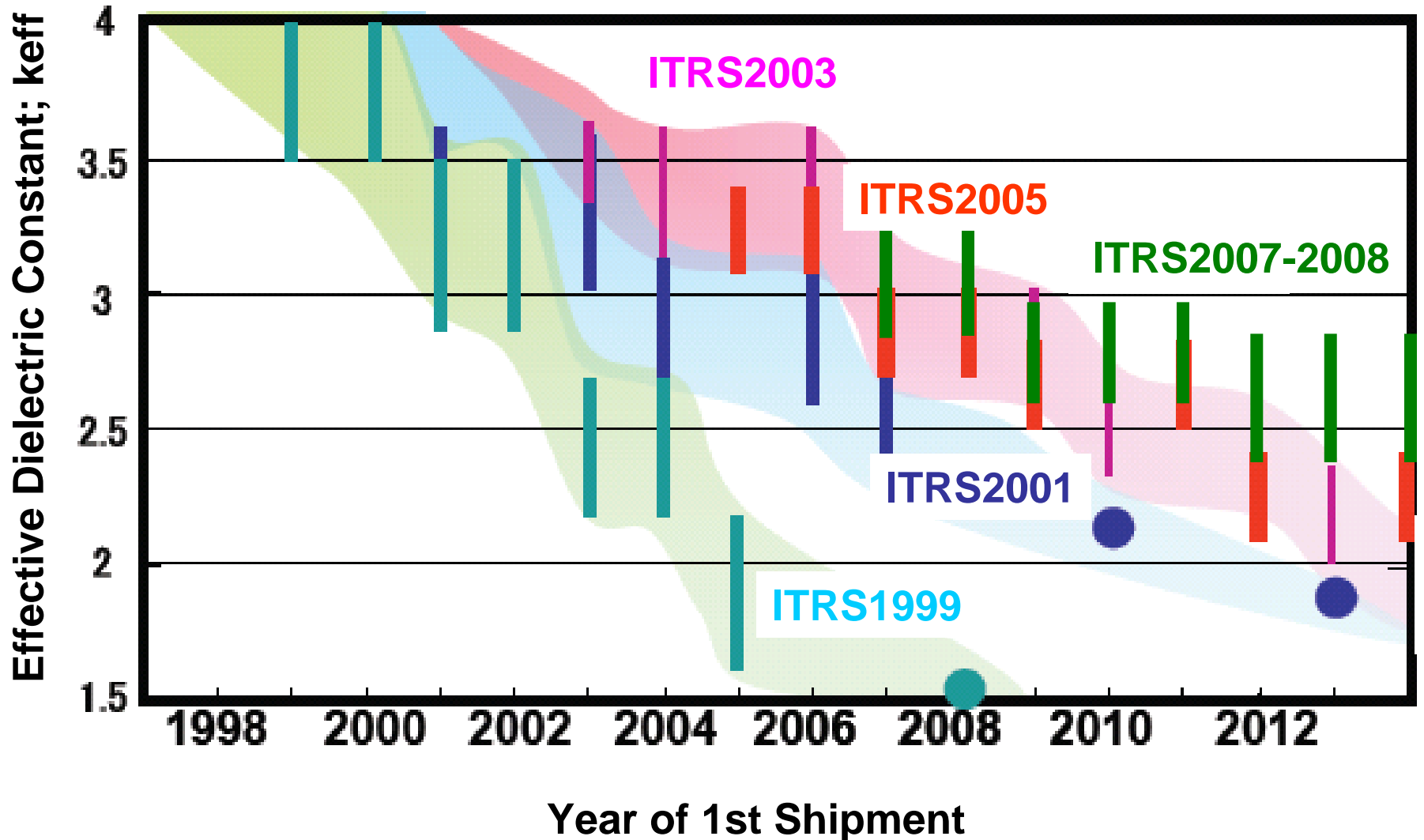


2008 TWG Highlights – Interconnect TWG

- Low-k Roadmap slowed in 2007-2008
- “Red Wall” Begins 2012 at 2.1-2.4



Historical Transition of ITRS Low-k Roadmap



2008 Low k update

<i>Year of Production</i>	<i>2007</i>	<i>2008</i>	<i>2009</i>	<i>2010</i>	<i>2011</i>	<i>2012</i>	<i>2013</i>	<i>2014</i>	<i>2015</i>
<i>MPU/ASIC Metal 1 1/2 Pitch (nm)(contacted)</i>	68	59	52	45	40	36	32	28	25
Interlevel metal insulator – bulk dielectric constant (κ)	2.5–2.9	2.5–2.8	2.3–2.6	2.3–2.6	2.3–2.6	2.1–2.4	2.1–2.4	2.1–2.4	1.9-2.2

<i>Year of Production</i>	<i>2016</i>	<i>2017</i>	<i>2018</i>	<i>2019</i>	<i>2020</i>	<i>2021</i>	<i>2022</i>
<i>MPU/ASIC Metal 1 1/2 Pitch (nm)(contacted)</i>	22	20	18	16	14	13	11
Interlevel metal insulator – bulk dielectric constant (κ)	1.9–2.2	1.9–2.2	1.7-2.0	1.7–2.0	1.7–2.0	1.5–1.8	1.5–1.8

- For those who think changes in k of 0.1 are significant – we aim to please
- For those who don't – try reaching consensus on low k with 100 people
- Proliferation of air-gap approaches

Values of effective k-value down to 1.7 with low crosstalk levels
 Localized air gaps to maintain good thermal and mechanical properties



2008 TWG Highlights – Assembly and Packaging TWG

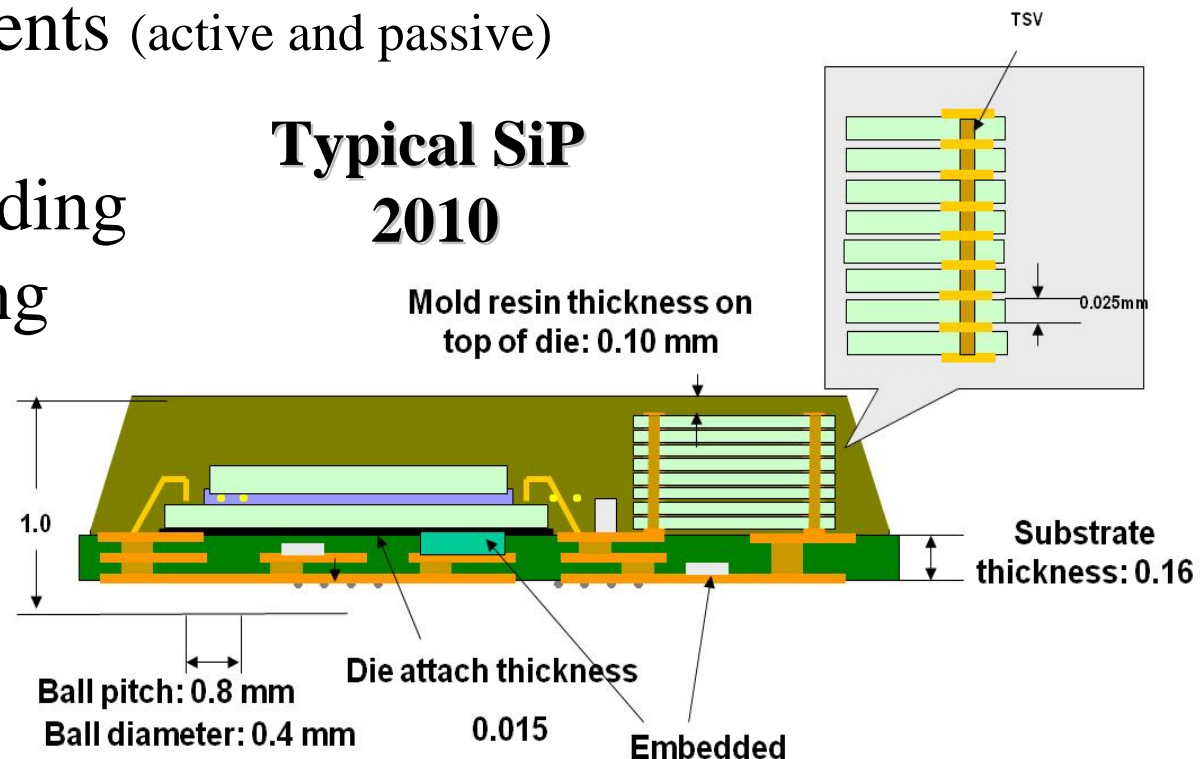
- Rapid growth in three dimensional electronics, System in Package (SiP) and other new technologies that enable “More than Moore” has resulted in an
- Accelerated pace of change in the Roadmap for Assembly and Packaging.
- There will be several sections added or expanded in the 2009 ITRS to address these emerging technologies.
- Several of these areas are initially addressed in the table changes for 2008.



New Packaging Requirements Stimulate Development of new Technologies with Difficult Challenges remaining

- Stacked die
- Wafer level packaging
- Through silicon vias
- Embedded components (active and passive)
- Wafer thinning
- Wafer to wafer bonding
- Die to wafer bonding
- New materials
- ...and more

Typical SiP 2010

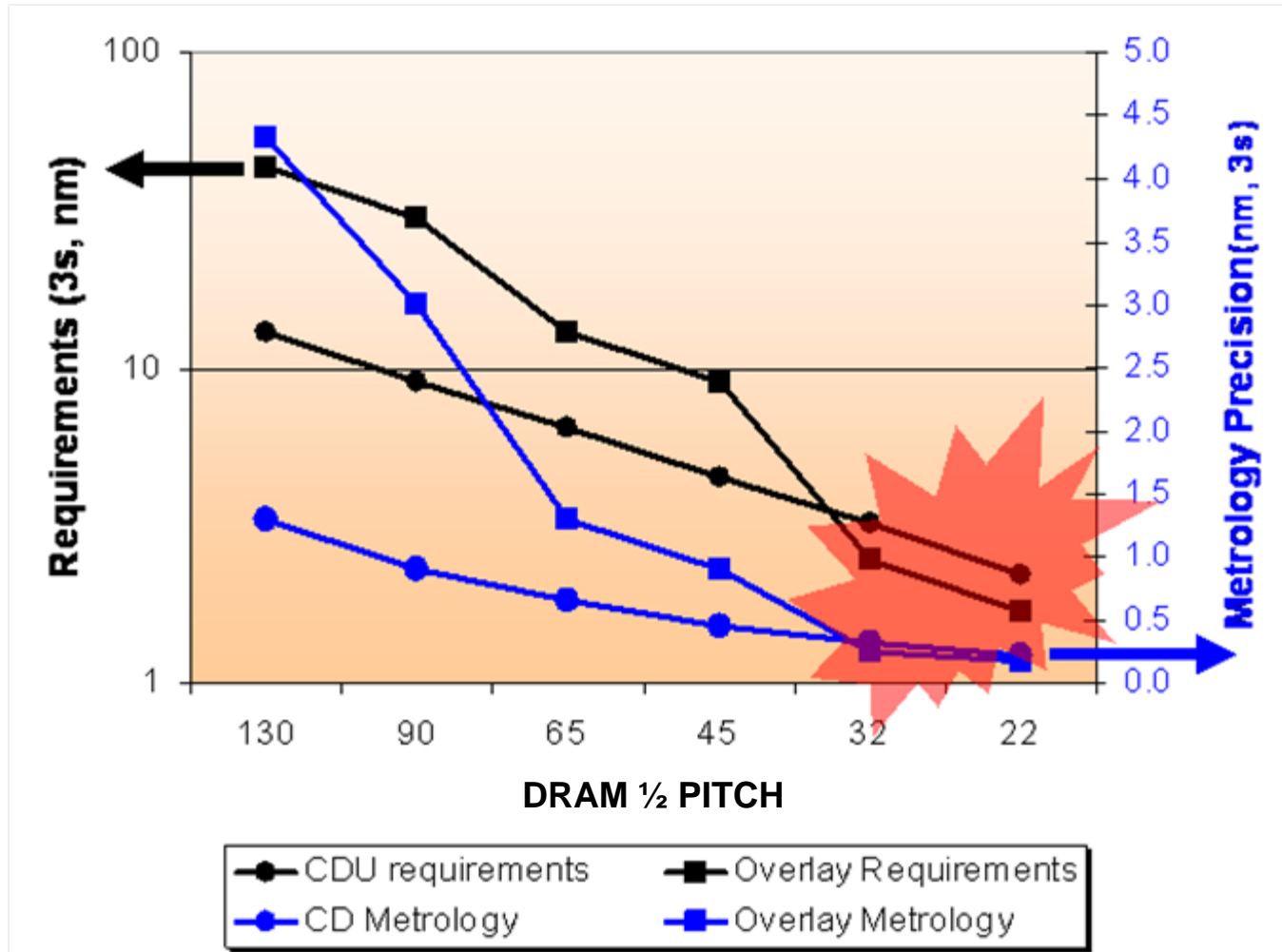


2008 TWG Highlights – Metrology TWG

- Focus on updating Lithograph Metrology and Front End Metrology Technology Requirements.
 - New Lithograph Processes such as double patterning, spacer double patterning, and double exposure present considerable challenges to the metrology community.
 - working in conjunction with the Lithography TWG assessed that general status of metrology needs
 - All forms of double patterning result in two distributions of CD and sidewall angle.
 - great challenge for all forms of CD metrology.
 - Furthermore, overlay control requirements are much stricter for double patterning and overlay impacts CD.
- In the area of FEP metrology, the timing of high k, metal gate and FD-SOI continue to impact metrology.



LITHO METROLOGY NEEDS



2008 ITRS Metrology Challenges

– As Usual, near-term “Red”

Year of Production	2008	2009	2010	2011	2012	2013	2014	2015
Flash ½ Pitch (nm) (un-contacted Poly)(f)	45	40	36	32	28	25	22	20
DRAM ½ Pitch (nm) (contacted)	59	52	45	40	36	32	28	25
MPU Printed Gate Length (nm) ††	38	34	30	27	24	21	19	17
MPU Physical Gate Length (nm) [after etch]	29	27	24	22	20	18	17	15
Lithography Metrology (Wafer) Technology Requirements								
Gate (MPU Physical Gate Length)								
Wafer CD metrology tool uncertainty (nm) P/T = 0.2 for isolated printed and physical lines	0.60	0.55	0.50	0.46	0.42	0.38	0.35	0.32
Dense Line (Flash 1/2 pitch, un-contacted poly)	45	40	36	32	28	25	22	20
Wafer CD metrology tool uncertainty (nm) * (P/T = .2 for dense lines**)	0.94	0.83	0.74	0.66	0.59	0.52	0.46	0.42
Double Patterning Metrology Requirements ****								
Image placement (nm, multipoint) for double patterning of independent layers	5.8	5.0	4.4	3.8	3.4	3.0	2.7	2.4
Metrology Uncertainty (nm, P/T=0.2)	1.2	1.0	0.9	0.8	0.7	0.6	0.5	0.5
Difference in CD Mean-to-target for two masks as a double patterning set	2.4	2.1	1.8	1.6	1.4	1.3	1.1	1.0
Metrology Uncertainty (nm, P/T=0.2)	0.2	0.2	0.2	0.2	0.1	0.1	0.1	0.1
FEP Metrology Requirements								
EOT measurement precision 3s (nm)	0.0040	0.0040	0.0028	0.0028	0.0024	0.0020	0.0026	0.0023
Lateral/depth spatial resolution for 2D/3D dopant profile (nm)	3.2	2.8	2.4	2.3	2	1.8	1.7	1.5
Elemental Composition Metrology for Metal Gate on Patterned Wafers (at %)	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1
Interconnect Requirements								
Measurement of deposited barrier layer at thickness (nm)	4.3	3.7	3.3	2.9	2.6	2.4	2.1	1.9
Detection of voids, 1% or more of total metal conductor volume of copper lines and vias.	5.7	5	4.5	4	3.5	3.2	2.8	2.5
Detection of killer pore in ILD (nm)	5.7	5	4.5	4	3.5	3.2	2.8	2.5



2008 TWG Highlights – Factory Integration TWG

- 300mm Prime and 450mm joint manufacturer and supplier planning and integration key to potential productivity solutions
- Consortia Standards and Guideline development underway, along with test bed for demonstrating AMHS tools and software



Planned Stepwise Productivity Improvement

Near Term Years	2008	2009	2010	2011	2012
Technology trend (nm)	57	50	45	40	35
Wafer Size (mm)	300	300	300	300	450

450mm
?
NGF ?

Planning for
NGF/450mm

Long Term Years	2013	2014	2015	2016	2017	2018	2019	2020	2021
Technology trend (nm)	32	28	25	22	20	18	16	14	13
Wafer Size (mm)	450	450	450	450	450	450	450	450	450

Start of NGF and/or 450mm
Implementation

- 2008 and future years are targeted to accommodate significant productivity improvement and relevant technology developments



Factory Integration 2007-08 Updates

- AMC, Process Control needs and AMHS data needs are being addressed
- Added small lot (12 wafer) metrics to reflect various business models
- Added metric to address Equipment sleep mode needs
- Addressing Technology requirement and potential solutions for 300Prime/450mm
- Productivity waste reduction roadmap in 2008 will address fab and equipment productivity



2008 TWG Highlights – Environment, Safety, Health (ESH) TWG

Resource Efficiency

- Primary Focus for 2007-08 is the Management of Resources
 - Chemicals
 - Reduction of Energy Use
 - Reduction of Raw Water Use
- New Energy Focus (“Green ITRS”),
 - Energy Special Topic published in 2008 Overview
 - www.itrs.net - http://www.itrs.net/Links/2008ITRS/Update/2008_Update.pdf



2008 TWG Highlights – Environment, Safety, Health (ESH) TWG (cont.)

- Focus for Environment on updating the roadmap for energy and water resource conservation requirements.
 - 2008 revised data and analysis model –
 - existing (2007 ITRS) values for these areas were potentially in conflict (meeting one goal could drive up the other and vice versa).
 - Analysis demonstrated that water and energy use are mutually dependent and therefore
 - Must have numerical values that reflect such dependence.
- The objective behind site water consumption reduction needs: ensure sustainable growth of the semiconductor industry that depends on this resource.
 - Updates for 2008 include a reduction in the numerical value for total consumption.
 - Recycling goals were held flat pending more in-depth analysis during 2009.
- Energy consumption concern: sustainability in support of industry growth.
 - Total factory level energy values were reduced, while short term tool energy values increased to reflect the next generation tool set.
 - Long-term tool energy values are flat or down, **excluding the potential impact of EUV equipment.**
 - Fab tool energy values established as a reflection of 2007 baseline energy consumption rather than an absolute number.



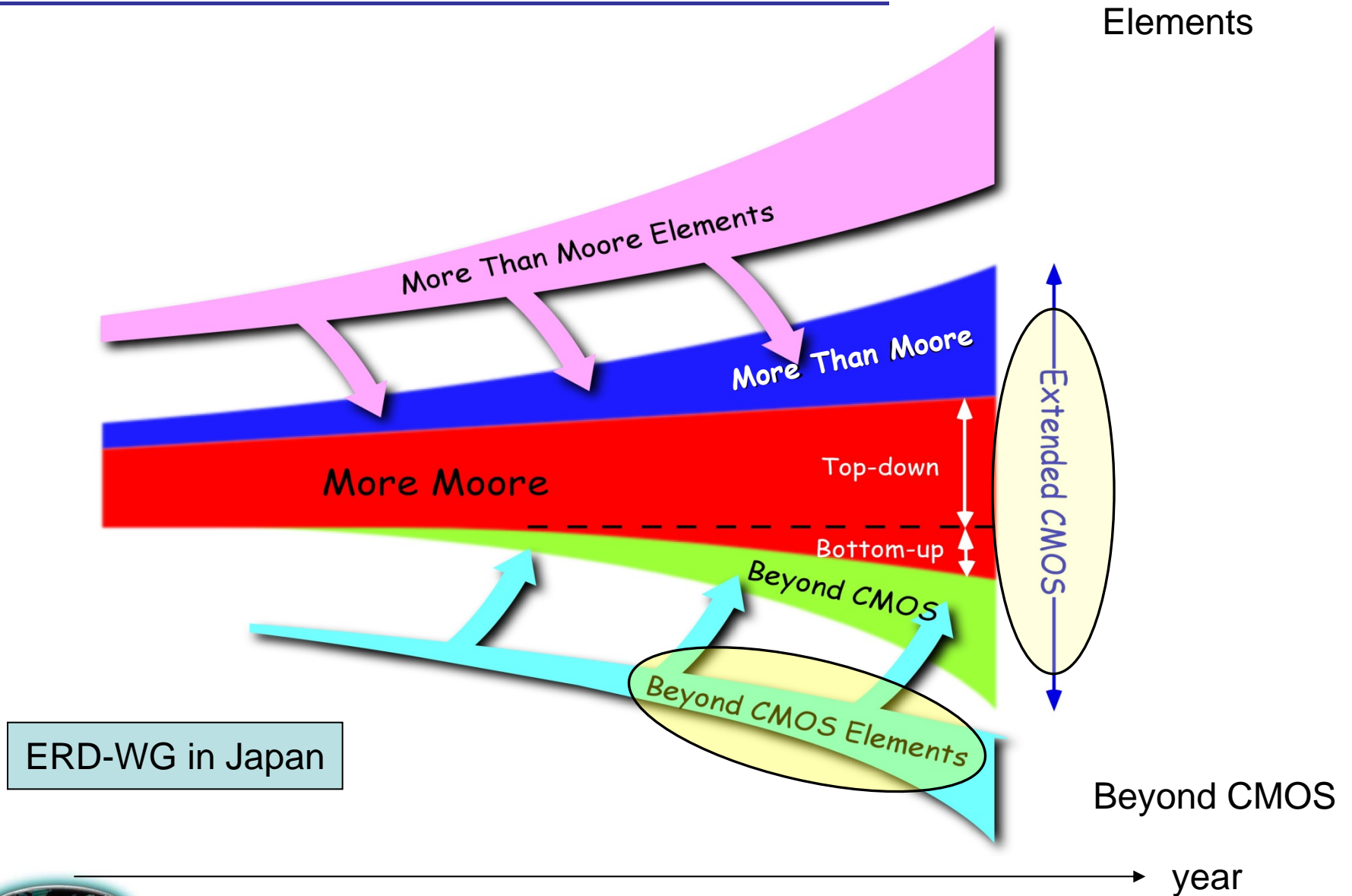
2008 TWG Highlights – ERD/ERM TWG

ERD and ERM accomplished major cross-region work on the IRC request to develop a “Beyond CMOS” “Next Switch and Storage Element” clarification

- New definition added to Glossary
- New “Beyond CMOS” graphical representation
- White-paper-reviewed workshops
- Public Seoul ERD and ERM presentations*
 - Published online at www.itrs.net public
 - target to develop table structures for passing over the closest-in candidates to PIDS and FEP and Factory Integration
 - identified potential solution candidates for long-range ITRS-horizon research (driven by PIDs needs tables);
 - and also including beyond the 2022 Roadmap horizon potential solutions



Evolution of Extended CMOS



New ERD/ERM Roadmapping Task

Determine which, if any, current approaches to providing a “Beyond CMOS” information processing technology is/are ready for more detailed roadmapping and enhanced investment.



Candidate Technologies for Information Processing

Device Technology Entry	Augment/Extend CMOS	Beyond CMOS
Nanoelectromechanical Switch	X	
Spin Transfer Torque		X
Collective Strongly Correlated Many-electron Spin Devices		X
Carbon-based Nanoelectronics	X	X
Atomic / Electrochemical Metallization Switches		X
Single Electron Transistors	X	
CMOL / FPNI (Field Programmed Nanowire Interconnect)	X	

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- Additional Details Available in Online Roadmaps and Public Presentations at www.itrs.net ; http://www.itrs.net/Links/2008ITRS/Update/2008_Update.pdf
- Future Fab 2008 ITRS special edition articles also online and linked at: www.itrs.net to <http://www.future-fab.com/welcome.asp>

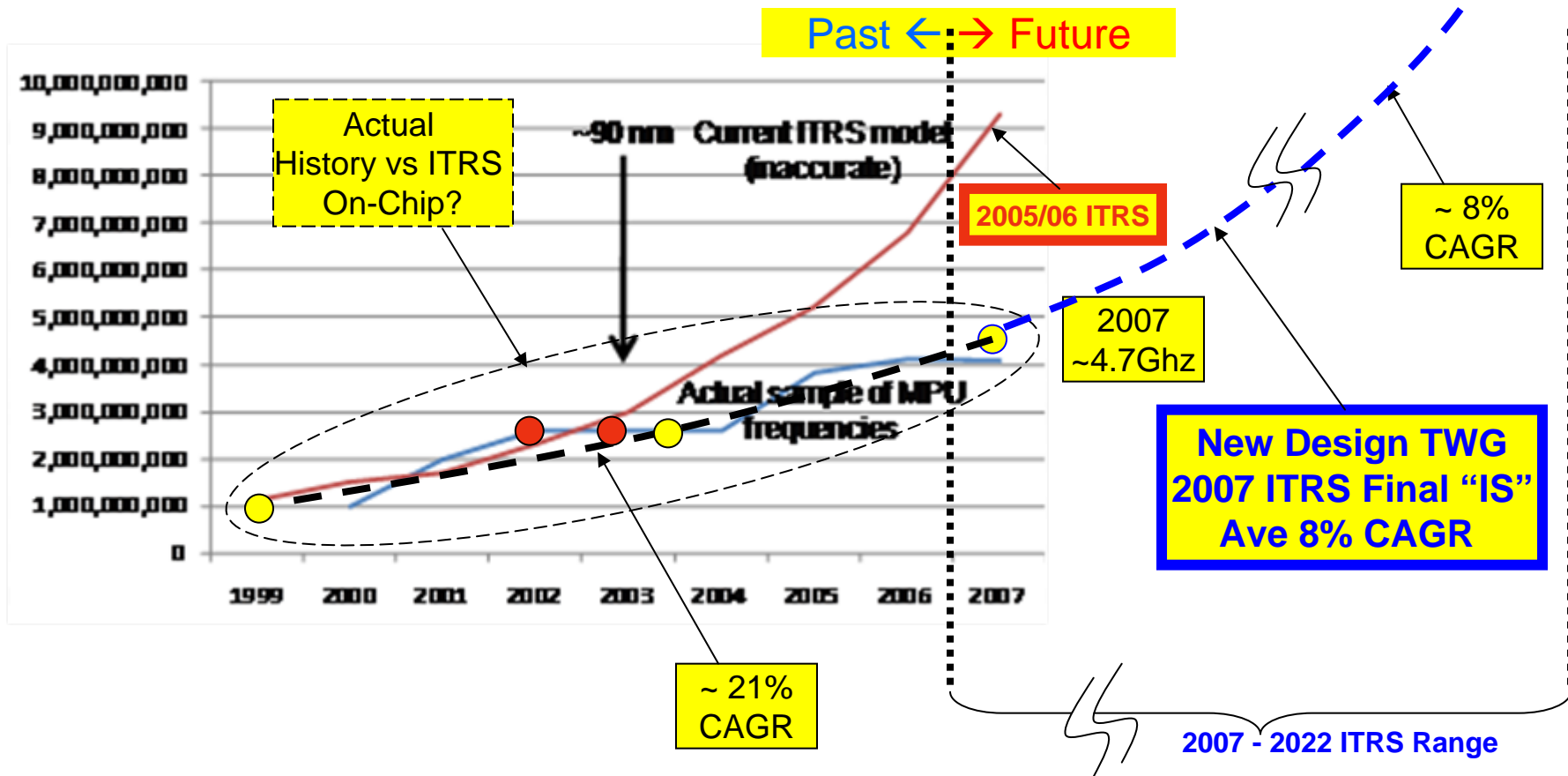


Backup

- Design On-Chip Frequency
- SICAS Technology, Wafer Generation Demand Update
- “More Moore” and “More than Moore” Definitions Update



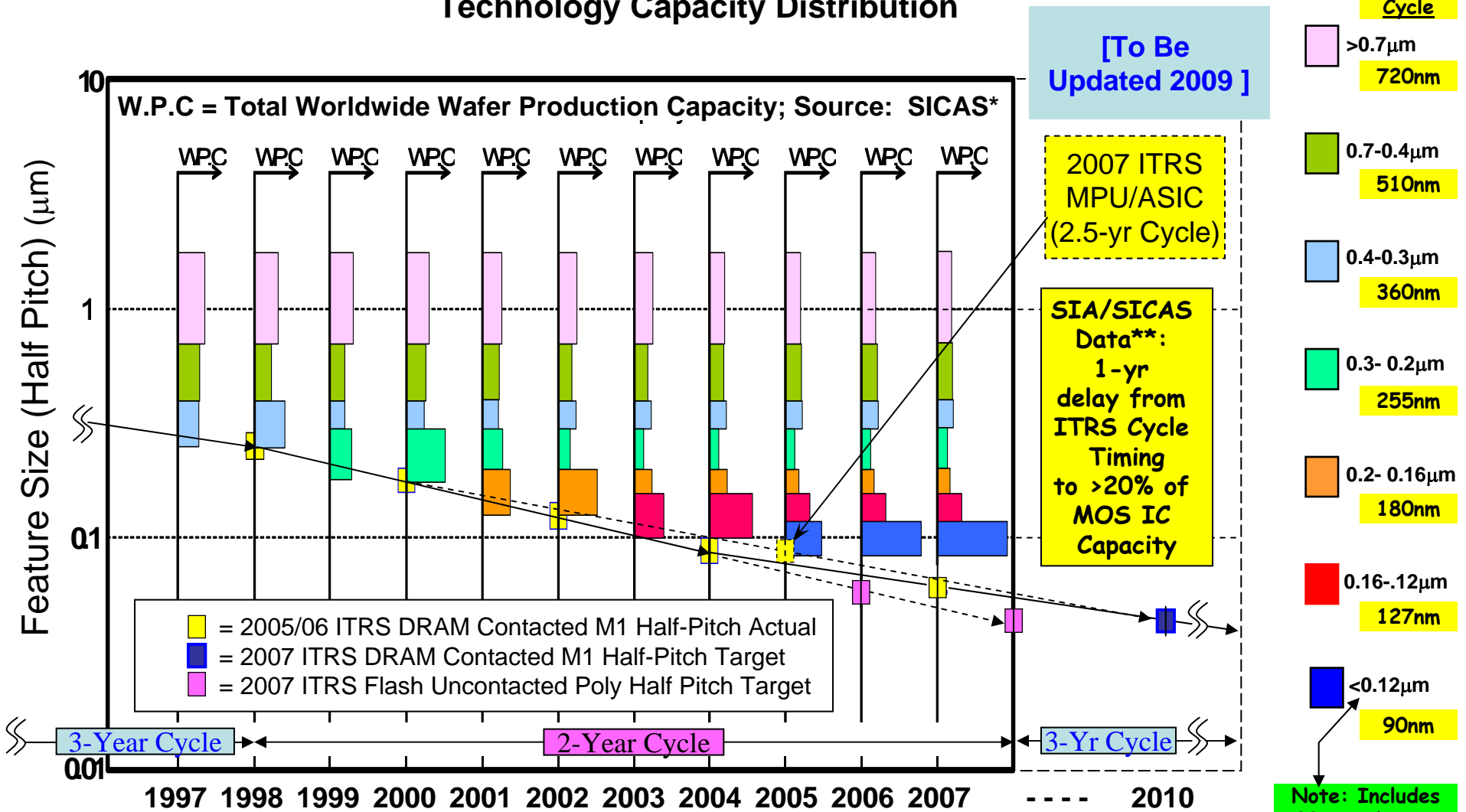
New Design TWG 2007 ITRS Frequency Historical Data vs 2005 ITRS And Proposed* Trend Ave ~8% CAGR



* Source: Various, per ITRS Design TWG ca August 2007



2007 "Fig 4" Technology Cycle Timing Compared to Actual Wafer Production Technology Capacity Distribution

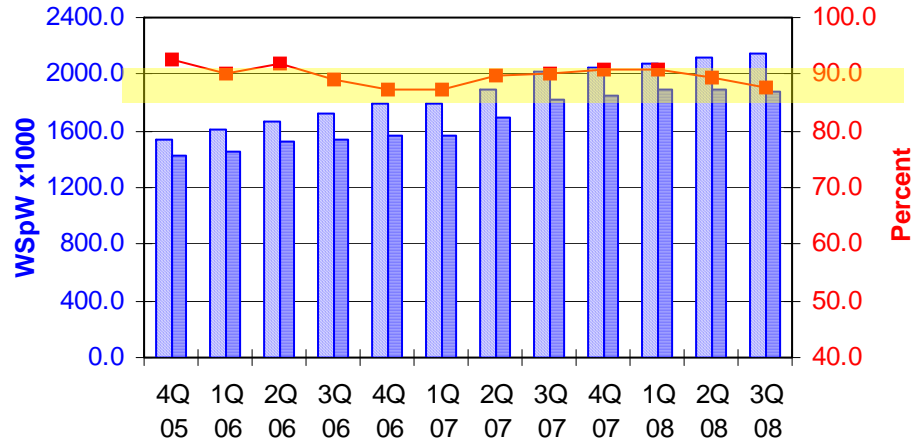


Note: The wafer production capacity data are plotted from the Semiconductor Industry Association (SIA) Semiconductor Industry Capacity Statistics (SICAS) 4Q data for each year, except 2Q data for 2007. The width of each of the production capacity bar corresponds to the MOS IC production start silicon area for that range of the feature size (y-axis). Data are based upon capacity if fully utilized.

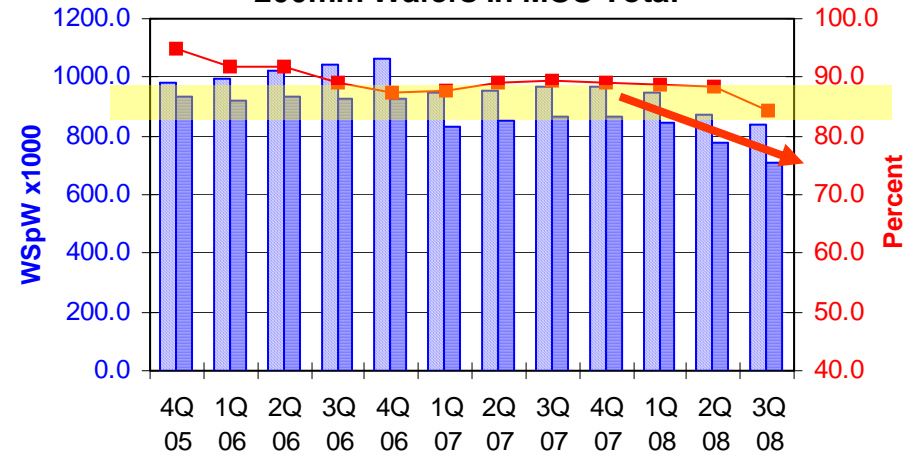
** Source: The data for the graphical analysis were supplied by the Semiconductor Industry Association (SIA) from their Semiconductor Industry Capacity Statistics (SICAS). The SICAS data is collected from worldwide semiconductor manufacturers (estimated >90% of Total MOS Capacity) and published by the Semiconductor Industry Association (SIA), as of August, 2007. The detailed data are available to the public online at the SIA website, http://www.sia-online.org/pre_stat.cfm.

SICAS – 3Q08 Status – [www.sia-online.org]

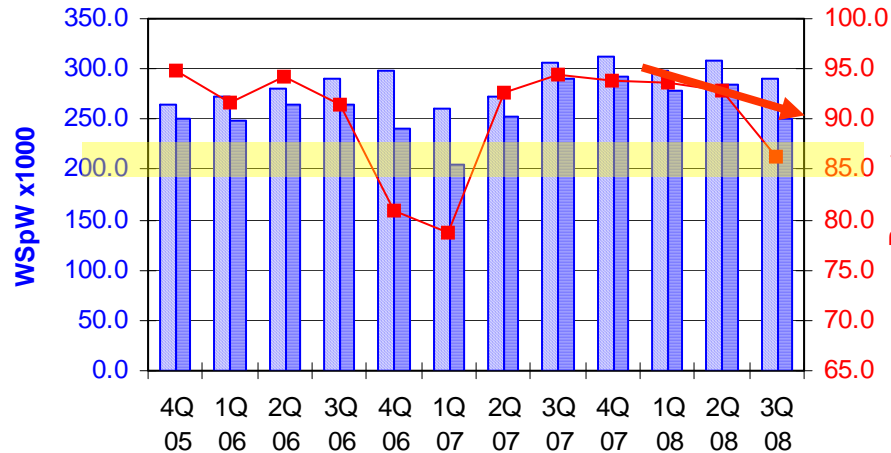
MOS Total



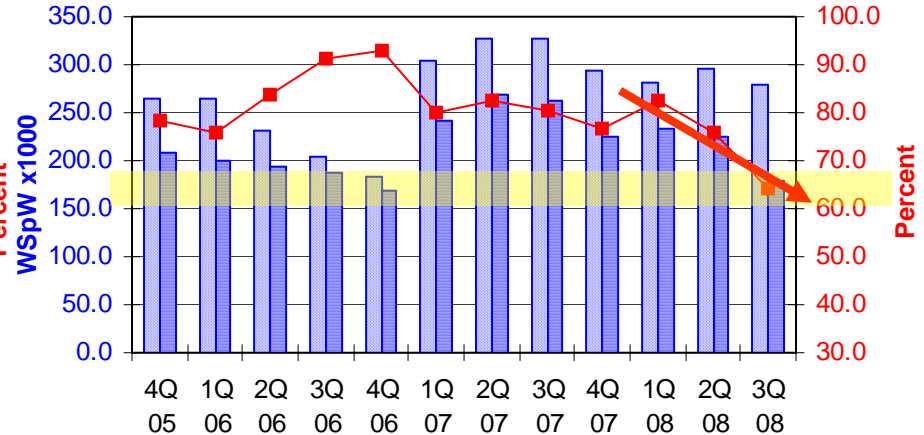
200mm Wafers in MOS Total



Foundry Wafers in MOS Total



Smaller than 200mm Wafers in MOS Total



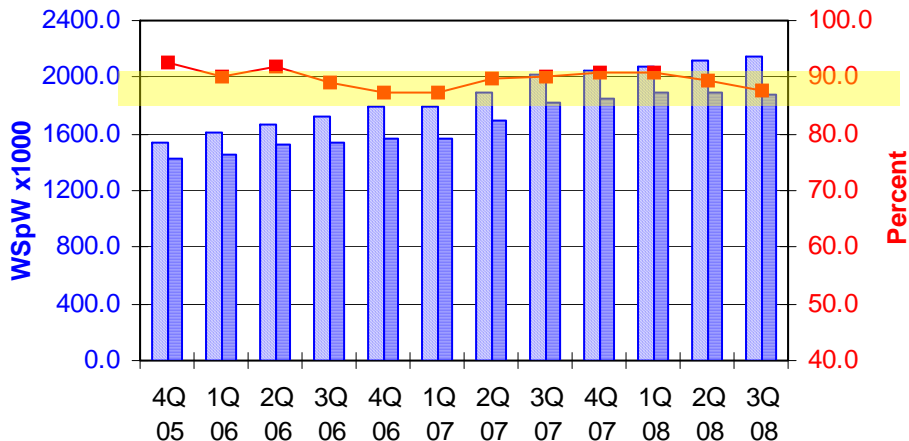
WSpW = Wafer-Starts per Week. All MOS data are expressed in 8 inch equivalent wafers [note: 300mm converted to 200mm equiv.]

Legends : Capacity WSpW Actual WSpW Utilisation of capacity in percent

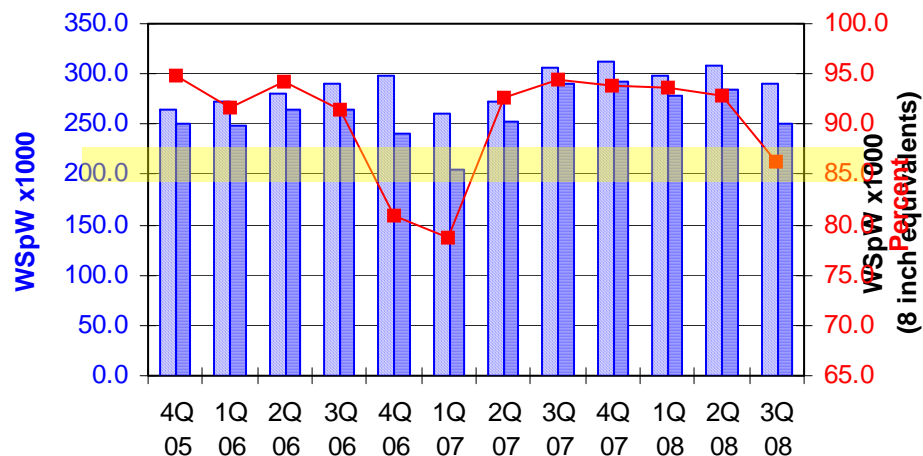
- Unit Growth peaked in 2Q (IC Insights) Capacity Growth drops – particularly Foundry
- Overall Utilization falls under 90%, Foundry dramatic drop (~86% from 93%)
- 200mm capacity, demand, and utilization drop in 4Q
- <200mm capacity growth in '07, but demand drops, crashing utilization to ~65%

SICAS – 3Q08 Status – [www.sia-online.org]

MOS Total



Foundry Wafers in MOS Total



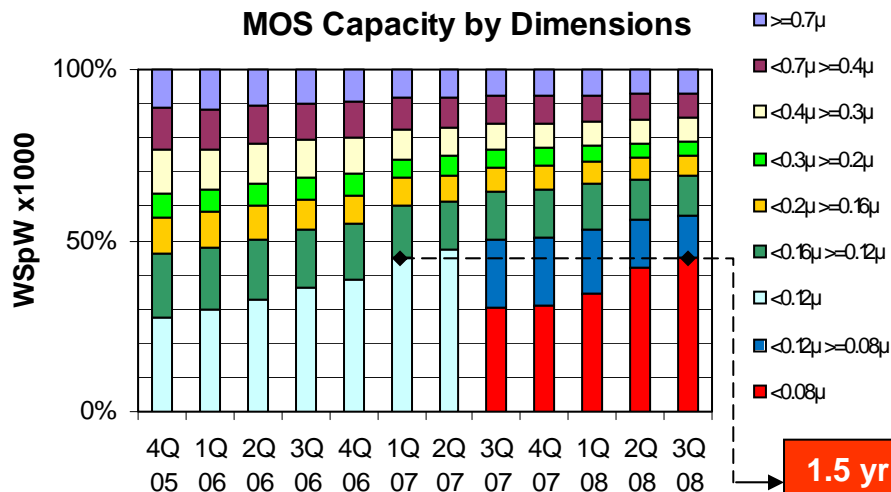
WSpW = Wafer-Starts per Week. All MOS data are expressed in 8 inch equivalent wafers [note: 300mm converted to 200mm equiv.]

Legends : Capacity WSpW

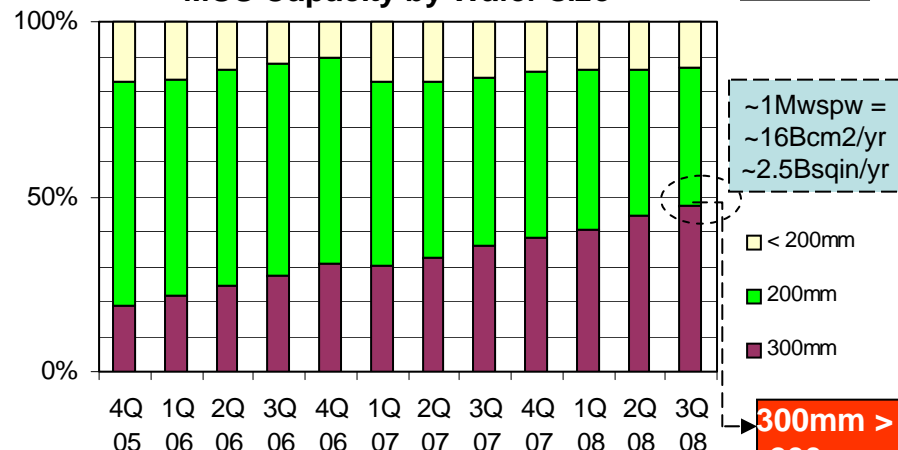
Actual WSpW

Utilisation of capacity in percent

MOS Capacity by Dimensions



MOS Capacity by Wafer-size



- Unit Growth peaked in 2Q (IC Insights) Capacity Growth drops – particularly Foundry
- Overall Utilization falls under 90%, Foundry dramatic drop (~86% from 93%)
- The >0.08u technology capacity accelerates to 1.5-year cycle (previous cycle was 2yrs)
- At nearly 50% of Total MOS, 300mm quarterly capacity exceeds 200mm for first time

Glossary [2008 ORTC Update - IS]

Key Roadmap Technology Characteristics Terminology

(with observations and analysis)

Moore's Law—An historical observation by Gordon Moore, that the market demand (and semiconductor industry response) for functionality per chip (bits, transistors) doubles every 1.5 to 2 years. He also observed that MPU performance [clock frequency (MHz) × instructions per clock = millions of instructions per second (MIPS)] also doubles every 1.5 to 2 years. Although viewed by some as a “self-fulfilling” prophecy, “Moore's Law” has been a consistent macro trend and key indicator of successful leading-edge semiconductor products and companies for the past 30 years.

Scaling (“More Moore”)—

- **Geometrical (constant field) Scaling** refers to the continued shrinking of horizontal and vertical physical feature sizes of the on-chip logic and memory storage functions in order to improve density (cost per function reduction) and performance (speed, power) and reliability values to the applications and end customers.

- **Equivalent Scaling (occurs in conjunction with, and also enables, continued geometrical scaling)** refers to 3-dimensional device structure (“Design Factor”) improvements plus other non-geometrical process techniques and new materials that affect the electrical performance of the chip.

- **Design Equivalent Scaling (occurs in conjunction with equivalent scaling and continued geometric scaling)** refers to design technologies that enable high performance, low power, high reliability, low cost, and high design productivity.

- “Examples (not exhaustive) are: Design for variability; low power design (sleep modes, hibernation, clock gating, multi-Vdd, etc.); and homogeneous and heterogeneous multicore SOC architectures.”

- Addresses the need for quantifiable, specific Design Technologies that address the power and performance tradeoffs associated with meeting “More Moore” functionality needs, and may also drive “More Moore” architectural functionality as part of the solution to power and performance needs.

Functional Diversification (“More than Moore”)—the incorporation into devices of functionalities that do not necessarily scale according to “Moore's Law,” but provides additional value to the end customer in different ways. The “More-than-Moore” approach typically allows for the non-digital functionalities (e.g., RF communication, power control, passive components, sensors, actuators) to migrate from the system board-level into a particular package-level (SiP) or chip-level (SoC) potential solution.

- Design technologies enable new functionality that takes advantage of More than Moore technologies.

- “Examples (not exhaustive) are: Heterogeneous system partitioning and simulation; software; analog and mixed signal design technologies for sensors and actuators; and new methods and tools for co-design and co-simulation of SIP, MEMS, and biotechnology.”

- Addresses the need for design technologies which enable functional diversification

Beyond CMOS—emerging research devices, focused on a “new switch” used to process information, typically exploiting a new state variable to provide functional scaling substantially beyond that attainable by ultimately scaled CMOS. Substantial scaling beyond CMOS is defined in terms of functional density, increased performance, dramatically reduced power, etc. The “new switch” refers to an “information processing element or technology”, which is associated with compatible storage or memory and interconnect functions.

- Examples of Beyond CMOS include: carbon-based nano-electronics, spin-based devices, ferromagnetic logic, atomic switch, NEMS switches, etc.

- Design/System Drivers TWG added More Moore and More than Moore Text Updates
- Emerging Research Devices/Emerging Research Materials TWG added “Beyond CMOS” Text

