Future ESD Challenges for IC Components and Systems

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Purpose

• Describe Electrostatic Discharge (ESD) and what it means to electronics applications
• Present the state-of-the-art ESD for components and systems
• Review the impact of advanced technologies on ESD and for future of the electronics
Outline

• ESD Control Status at Manufacturing
• Impact of ESD on Electronic Systems
• ESD Challenges from Advances in Silicon Technologies
• ESD Design Constraints from Advanced Circuit Features
• IC Package Technology Development and ESD
• System Level ESD Protection
• ESD Design Efficiency for System Level Protection
• Future Research Opportunities
Definitions

- **Electrical Overstress (EOS)**
  The exposure of an object to a current or voltage beyond its maximum ratings.

- **Electrostatic Discharge (ESD)**
  The transfer of electrostatic charge between bodies or surfaces at different electrostatic potential. ESD is a subset of EOS.
ESD Association

- The Electrostatic Discharge (ESD) Association
  - not-for-profit organization
  - founded in 1982
  - dedicated to advancing the theory and practice of ESD avoidance
  - Much of the understanding of ESD Control is a result of work by experts in the field
Definitions

EOS General

ESD  →  EOS Specific  ←  Lightning

High Voltage (1V –15kV)  →  Low Voltage (16V)
Short Duration  ←  Longer Duration
Very Low Power  →  Low Power
Fast Rise Time  (1-10 ns)  (1-10 ms)

Integrated Circuit (IC) chips used in consumer and medical electronics can be damaged with ESD

Houses, Buildings, Airplanes, Electronics, etc.

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What voltage levels are generated if ESD is not controlled?

<table>
<thead>
<tr>
<th>CONDITION</th>
<th>AVERAGE READING(V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Person Walking Across Linoleum Floor</td>
<td>5,000</td>
</tr>
<tr>
<td>Person Walking Across Carpet</td>
<td>15,000</td>
</tr>
<tr>
<td>Person Working at Bench</td>
<td>800</td>
</tr>
<tr>
<td>Ceramic Dips in Plain Plastic Tube</td>
<td>700</td>
</tr>
<tr>
<td>Ceramic Dips in Plastic Set-Up Trays</td>
<td>4,000</td>
</tr>
<tr>
<td>Ceramic Dips in Styrofoam</td>
<td>5,000</td>
</tr>
<tr>
<td>Circuit Packs as Bubble Plastic Cover Removed</td>
<td>20,000</td>
</tr>
<tr>
<td>Circuit Packs as Packed in Foam Box</td>
<td>11,000</td>
</tr>
<tr>
<td>Circuit Packs (Packaged) as Returned For Repair</td>
<td>6,000</td>
</tr>
</tbody>
</table>
But, humidity helps reduce static charge generation and accumulation

(values shown in volts)

<table>
<thead>
<tr>
<th>Event</th>
<th>Relative Humidity</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>10%</td>
</tr>
<tr>
<td>Walking across a vinyl floor</td>
<td>12,000</td>
</tr>
<tr>
<td>Motion of bench employee</td>
<td>6,000</td>
</tr>
<tr>
<td>Removing ICs from plastic tube</td>
<td>2,000</td>
</tr>
<tr>
<td>Packing PWBs in foam line box</td>
<td>21,000</td>
</tr>
</tbody>
</table>

* TED DANGELMAYER, ESSENTIALS PROGRAM MANAGEMENT, KLUWER ACADEMIC PUBLISHERS, 1999

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STATIC CONTROL MATERIALS
Materials that are used to control static electricity

• **INSULATIVE**: Non-conductive, removed from workplace whenever possible. Poses high risk of ESD damage.
  
  (> 1x10e12 Ohms)

• **CONDUCTIVE**: Lowest surface resistance. Care should be exercised using conductive surfaces if CDM issues exist in the process.
  
  (<10e4 Ohms)

• **DISSIPATIVE**: Bleeds off charges at optimum rate. Strongly preferred.
  
  (10e4 to < 10e11 Ohms)
If it is not properly controlled in a silicon manufacturing environment...

Thousands of volts can be generated

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How is ESD controlled?

1. Grounding Person Wrist Strap to Ground (or flooring/footwear)
2. Grounded Work Surface
3. ESD Protective Packaging

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Only hundreds of volts are generated

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IC Package Impact on ESD

- IC packages can have impact on ESD requirements for
  - Human Body Model (HBM)
    - Exposed IC package pins can be touched during normal handling
  - Charged Device Model (CDM)
    - IC packages that acquire charge in automated handlers can discharge with contact to ground
Human Body Model (HBM)

Exposed IC package pins can be touched during handling

Advanced dense pin packages are making it less critical

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Courtesy: ESD Association
IC package pins that acquire charge can discharge to ground

Advanced large pin packages are making it more critical

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Courtesy: ESD Association
What about touching the systems themselves?

Electric and magnetic fields produced by ESD couple to the system in multiple ways, causing failures.
A human holding a metallic object (e.g. keys, screwdriver) discharging accumulated static charge through an electronic product (e.g. cellular phone, computer).
Cable Discharge During Computer Connections

- Cables could acquire electrostatic charges primarily due to tribo-charging.
- A discharge could occur when a charged cable is plugged into an electronic equipment.
- The electronics inside must be protected.

**Discharge from a 100m long cable charged to 2000V**
Comparison of Different Stress Events (EOS can have different rise times and durations)

EOS Compared to ESD: EOS can have slower rise times, lower current, but very long duration to cause severe damage.

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IC Chip pins are protected with protection devices (diodes) on the chip.

The Input and Output pins of the IC are protected from ESD.
On-Chip Protection Design

The Input and Output pins of the IC protected from ESD

The clamp turns only when ESD is detected

These clamps introduce capacitance and reduce circuit speed

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**NMOS Bipolar Physics**

**Characteristics of the LNPN:**

- Parasitic Bipolar Gain (Beta)
- Avalanche Multiplication Factor (M)
- Effective Substrate Resistance ($R_{sub}$)

\[ I_D = I_{DS} + I_c + I_{gen} \]

\[ \beta = \frac{(\beta + 1)I_D}{\beta (I_D - I_{sub}) + 1} \]

\[ M = \frac{(\beta + 1)I_D}{\beta (I_D - I_{sub})} \]

\[ R_{sub} \approx 0.8 \frac{I_{sub}}{I_D} \]

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Transmission Line Pulsing

Pulse width: 100ns
Rise time: 200 ps to 10 ns

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Measured TLP Curves

It2 information is used to design for ESD protection
ESD Protection Window

ESD Design must operate within the window.
Any type of ESD clamp must protect the gate oxide at <Bvox.

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The scaling features have strong impact on ESD; junction depth \((X_j)\), the channel length \((L)\), electric fields at the junctions, or the oxide thickness.

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Characterization for ESD

• Junction avalanche voltage
  – Transistor design
• Oxide reliability
  – Oxide damage and breakdown with ESD
• Metal failure current density
  – High current conduction through the interconnect metal leads
• Substrate resistance
  – Choice of silicon starting material
Common IO Protection Design Methods

**Local Clamp Approach:**
- Conducts ESD current at the IO Pad
- More traditional approach
- Introduces higher capacitance and leakage

**Rail Clamp Approach:**
- ESD current diverted to the Vdd Bus
- Currently more popular
- Useful for high speed circuit applications due to lower capacitance/leakage at the IO
ESD Development (last 30 years)

1979
Static Material Development

1983
Learning of Basic ESD Control

1988
Silicon Physics

1993
Design Optimization

1998
Advanced ESD Control

2003
Technology Optimization

2008
Polymer Materials

Control

Device

Design

Killer Effects from Technology & IC Design
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Every technology advance has significant impact on ESD design for the IC circuits.
• Metal thickness and pitch are reduced each new node
• Aspect ratio ~ constant \( \Rightarrow R_{\text{SHEET}} \uparrow \text{ and } C_{\text{LINE}} \downarrow \)

\[ I_{\text{FAILURE,NORM}} (\text{A/um}) \]

\[ \begin{array}{c}
65\text{nm} \\
90\text{nm} \\
130\text{nm}
\end{array} \]

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Interconnect Current Density Under HBM
$R_{SHEET}$ $\uparrow$ and $C_{LINE}$ $\downarrow$

Wider metal leads with larger parasitic capacitance needed at advanced nodes
- BV per nm ($E_{BD}$) ↑ as the thickness ↓
- Poly depletion, which ↑ as the thickness ↓

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With silicon scaling, both metal lead current density and oxide breakdown voltage reduction are closing the ESD Window for High Speed Designs making it difficult to maintain 2kV HBM.
Silicon Technology Advances and Challenges...

• Smaller transistors (<100 nm feature sizes) for higher speed circuits (5-10 GHz)
  – These transistors are much more delicate for ESD protection

• Complex circuit designs with multiple functions on the same chip
  – Continuous challenge to protect them and still maintain high speed performance

• Larger and advanced IC packages producing higher current levels during discharge
  – Making sure all types of packages are equally protected
IMPACT ON HIGH SPEED DESIGNS

- Data Rates are influenced by the ESD loading capacitance
- The requirement of low capacitance in turn degrades ESD levels
- At 100 fF and below 2kV HBM cannot be achieved
Multi-gate Transistors (MUGFETs) with very small dimensions

- Fin height: 66-80nm (present), 30-40nm (target)
- Fin width: 50nm (present), 20-30nm (target)
- Capability to carry ESD current?

C. Duvvury  C. Russ ESD Symp. 2005
Impact from FinFETs

• 3D-View of a FinFET Device

- With mature process acceptable intrinsic I_t2 can be achieved
- Optimization of both process and layout parameters are critical
- Gate length, gate thickness and fin spacing can lead to improved ESD performance

Gossner et al., IEDM 2005

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Impact from FinFETs

FinFETs in MOS-diode mode (1/2)

- Larger mobility
- lower $R_{ON}$
- less heating
- higher ESD robustness

Current [mA] vs. Voltage [V]

- Strain ($V_{HBM}=160V$)
- No strain ($V_{HBM}=140V$)
Impact from FinFETs

FinFETs in bipolar mode (1/2)

Larger mobility
lower holding voltage
less heating

Current [mA]

Voltage [V]

strain
($V_{HBM}=200V$)

no strain
($V_{HBM}=150V$)

Holding voltage

Giffoni et al., IEDM 2008
Impact from Strain Engineering

Impact of Strain Engineering on ESD performance

- Bandgap Reduction
  - E-Field ↓
  - Majority carrier µ ↑
  - Heat Q ↓
  - R_on, V_hold ↓

- Mobility Modulation
  - Minority carrier µ ↓
  - Minority carrier accumulate
  - Substrate Potential & β ↑

- Thermal
  - Heat capacity ↓ at compressive stress
  - Heat capacity ↑ at tensile stress
  - Thermal conductivity ↓

As technology continues to scale down, the enhancement of strain engineering on ESD performance increases!

Impact from:
- Band-gap engineering
- Mobility modulation (majority & minority)
- Thermal conductivity modulation

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Lu et al., IEDM 2009
Circuit Challenges: New Designs

- Increased Analog IO applications
- Analog Integration
- High speed IO interfaces
- Increased RF integration
- New IO features
- USB applications
Drain Extended NMOS and ESD

- DENMOS are integrated into 90nm technology with 20Å gate oxide
- Drain voltage tolerance make them very attractive for high voltage analog applications (7V and 12V)

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Very poor bipolar behavior for ESD with $I_{T2} \sim 0$

Substrate bias somewhat alleviates this

Hence, the DENMOS ESD protection requires new challenging concepts such as substrate pumping
Device Research UC at Santa Barbara

Weak Snapback
Gradual Movement
Surface to Bulk

Strong Snapback
Abrupt Movement
Surface to Bulk

Path 1
Path 2

SG
SB

Gate
Source
Drain

E-Density

Log $I_D$ (Drain Current)

Voltage

DS
G
GSD
B

Device Research UC at Santa Barbara

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E-Density
Important Findings → IIT Bombay

- **RESURF DeMOS** → Very low $I_{T2}$ value → Insight towards the 3D filamentation and failure → Helped to Engineer devices → Modified device shows 5X improvement → Same mixed signal performance [M. Shrivastava, IRPS 2010]

- **ESD Protection Device** → HRB DeNMOS for Power clamps → Engineered device with moving filaments → Improved $I_{T2}$ [M. Shrivastava, IRPS 2009]

- **ESD Protection Device** → IGBT Plugged-in SCR device → For low voltage clamps → Very less transient overshoot, Same $I_{T2}$, Ultra Fast triggering → Excellent option for CDM protection concepts [M. Shrivastava, EOSES 2009]

- **Technology co-optimization** → Comparision between FinFET and ETSOI Devices → ETSOI was found to have excellent SoC performance [M. Shrivastava, IEDM 2009]
Important Findings

(a) STI DeNMOS Device
(b) Standard RESURF DeNMOS Device
(c) Modified RESURF DeNMOS Device

STI DeNMOS

Resurf DeNMOS

HBM Performance

Thermal failure

Base-push-out driven failure

Fail @ 2.5mA/μm

Fail @ 1.2mA/μm

Std Device (Min. DL)

Mod. Device (Large DL)

Fail @ 1.6mA/μm

High I_T2 and V_T2

Low current

Fail at low current.
ESD protection concept

- Usage of an Nwell diode’s parasitic pnp bipolar action to provide substrate biasing to the DEnMOS

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Digital, Analog, and RF on the same chip require three different ESD protection strategies.

Interactions through the different ground planes require complex ESD bus architecture.
Impact of ESD on RF Performance

Effects from RC Behavior of ESD Device:

- Degrades RF performance; Reduces RF Gain and Increases RF Noise
- To maintain good RF performance, ESD load cap < 100 fF
- Where to place the ESD Clamp? A co-design effort is needed
- Pos. 1: good for ESD; Pos. 2: good for RF (if external Lg is required)

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ESD performance is dependent on package type and the package lead design.

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Courtesy of Darvin Edwards (TI)
• Thinner and larger packages result in higher currents.

• Package parameters with impact on CDM behavior:
  – lead capacitance
  – bond wire and die attach
  – package substrate
  – package type
Higher pin count devices at every new tech node are market driven by HSS pins on microprocessors.
Package Size on ESD Current

CDM Peak Current at 500 V

Protection design is difficult for large packages
For HSS and RF designs the CDM levels are limited
65/45nm Protection Approach for HBM/CDM

- Commonly used for High Speed Serial Link (HSS) designs
- CDM clamp is critical to provide a voltage drop to protect the gate oxide

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Achievable CDM current levels are limited between 2-5 Amps depending on the circuit speed requirement.
Both Stacked Die and Stacked Package trends can lead to unknown ESD stress discharge currents
ESD Threshold Population Trends

Analysis by Dr. Terry Welsher, Dangelmayer Associates

Slide Courtesy Dangelmayer Associates

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Industry Council
ESD Qualification Issues
The Impetus for Change in ESD Targets

• Since 2003 there has been an increased awareness that many IC products are routinely failing ESD qualification

• This pattern was found to be consistent from company to company

• The associated cost of ESD has been mounting while it became apparent that products shipped with lower than the specification level ESD have not seen associated field returns
HBM Levels can be lowered to <2kV

- ESD/EOS failures as provided by various members of the Industry Council
- Includes both automotive products and consumer ICs
- A vast majority of the returns are often found to be due to EOS
- Total return rate due to EOS/ESD fails < 1 dpm
- No obvious correlation of EOS/ESD returns to HBM levels of 500 V … 2 kV

This data represents products shipped at various ESD levels with the same basic factory control

November 2010

Industry Council

9.3 billion sold with 2kV HBM
5.7 billion sold with 1.5kV HBM
0.7 billion sold with 1kV HBM
5.7 billion sold with 1.5kV HBM
4.8 billion sold with 500V HBM

Based on 21 billion devices
### Proposed New HBM ESD Levels

<table>
<thead>
<tr>
<th>HBM Level of IC</th>
<th>Impact on Manufacturing Environment</th>
</tr>
</thead>
<tbody>
<tr>
<td>2 KV</td>
<td>Basic ESD control methods allow safe manufacturing with wide margin.</td>
</tr>
<tr>
<td>1 kV</td>
<td>Basic ESD control methods allow safe manufacturing with sufficient margin.</td>
</tr>
<tr>
<td>500 V</td>
<td>Basic ESD control methods allow safe manufacturing.</td>
</tr>
<tr>
<td>100 V to &lt;500 V</td>
<td>Advanced ESD control methods (ANSI/ESD S20.20 or IEC 61340-5-1) are required to safely handle sensitive parts.</td>
</tr>
</tbody>
</table>

- ✓ Currently accepted by JEDEC
- ✓ Lowering to 1kV or 500V would reduce the impact on circuit performance and lead to less qualification delays
- ✓ The new levels would also reduce the ESD demand
IC design requirements create severe limitations for CDM protection

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New Recommended CDM Classification
Based on Factory CDM Control

<table>
<thead>
<tr>
<th>CDM classification level (tested acc. to JEDEC)</th>
<th>ESD control requirements</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CDM} \geq 250\text{V}$</td>
<td>• Basic ESD control methods with grounding of metallic machine parts and control of insulators</td>
</tr>
</tbody>
</table>
| $125\text{V} \leq V_{CDM} < 250\text{V}$     | • Basic ESD control methods with grounding of metallic machine parts and control of insulators +  
• Process specific measures to reduce the charging of the device  
OR to avoid a hard discharge (high resistive material in contact with the device leads). |
| $V_{CDM} < 125\text{V}$                     | • Basic ESD control methods with grounding of metallic machine parts and control of insulators +  
• Process specific measures to reduce the charging of the device  
AND to avoid a hard discharge (high resistive material in contact with the device leads) +  
• Charging/discharging measurements at each process step. |

Published as JEP157
Combined Package and Design Influence on CDM for 45nm

- **Digital Designs:** Stress Voltage @8A
  - DIP: 750V
  - QFP: 500V
  - TQFP: 400V
  - BGA: 300V
  - LGA: 250V
  - BGA: <200V

- **Advanced Digital Designs:** Stress Voltage @6A
  - DIP: 750V
  - QFP: 500V
  - TQFP: 400V
  - BGA: 300V
  - LGA: 250V
  - BGA: <200V

- **High Speed Designs:** Stress Voltage @4A
  - DIP: 500V
  - QFP: 400V
  - TQFP: 300V
  - BGA: 250V
  - LGA: <200V

- **RF Designs:** Stress Voltage @2A
  - DIP: 500V
  - QFP: 400V
  - TQFP: 300V
  - BGA: 250V
  - LGA: <200V

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ESD Control is becoming increasingly critical!
System Level ESD

What is an ESD Event?
- Object becomes charged - discharges to another
- Charging levels from 1 V to 50,000 V
- Discharge currents of 1A to 60 A or more

What is a System Level ESD Event?
- An electrical system experiences an ESD Event

What can happen in a System Level ESD Event?
- System continues to work without problem
- System is upset/lockup but no physical failure
  • “Soft Error”
  • May or may not require user intervention
- Physical Damage to System
  • “Hard Failure”
System Level ESD

What are some sources of System ESD Events?
- Charged Human
- Charged Human with a Metallic Tool
- Charged cables (Charger, Headset, USB, HDMI,..)
- Charged Products themselves

How is Event Transmitted to System
- Direct contact to a system I/O
- Direct contact to a system’s case
- Arc through a vent hole or seam to a circuit board
- Pickup of EM radiation from arc by system
Stages of ESD Protection Methods and Design

**Component ESD**
- **Fab environment**
  - Measure: Ionizer, Static handling
- **IC Assembly & Test**
  - Measure: Grounding, Ionizer
- **Board assembly & repair**
  - Measure: System level protection
- **End customer operation**
  - Measure: Shielding, Prerunning ground

**System level ESD**
- **Wafer**
- **IC component**
- **Board**
- **System**

*ESD Protected Area*

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ESD on Systems

Any electronic equipment can be damaged by ESD

“End Equipment”

PDAs
Cell Phones
Corded Phones
Computers
Printers
Copy machines
Automotive electronics
Telephone Switching gear
...any electronic end product!

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Digital Electronics...
Increasingly becoming part of daily lives
Music, Movies, TV Shows, Home Video, Photos, Audiobooks, Podcasts
…At Home

Consumers just want to turn it on and enjoy high quality digital content

Real Time A/V streaming, Data/Control, Decoder/Encoder, Content Protection
...On the Road
We need to make sure all electronics are protected!
The design of overall system protection requires understanding of the “Residual Pulse” going into the IC pin with external interface.
System-Efficient ESD Design (SEED) Concept

**PCB With Components**

- Utilizes the existing component level ESD as a starting point for design
- For an efficient system protection design, the IC pin breakdown characteristics play a critical role
- Effective IEC protection design can be achieved for any IC pin that interfaces with the external world

Industry Council 2010
Differentiation of Internal Vs. External Pins

- Internal Pins and External Pins should meet minimum HBM and CDM levels as defined by component handling requirements.
- But for achieving system level ESD robustness, the External Pins must be designed with proper protection strategy independent of their HBM/CDM protection levels.
USB2-OTG INTERFACE

- “Passives” includes
  - Bypass capacitors
  - EMI filter
    - Common Mode Filter
    - Chip Ferrite Bead

- 4 ports to protect
- Primary protection TVS
- Secondary protection IC ESD cells
- Hidden protection “Passives” & PCB Interconnect
Board Implementation

- 10 Layers PCB Stack up
- Layout/Board representative of an End – Application
- PCB interconnect

Distance TVS → IC

Distance TVS → USB2 Receptacle
Spice Methodology Overview

- IC Failing Limits
  - $I_t$ (slow transient)
  - $I_p$ (fast transient)

- TLP model
  - IC ESD cells
  - TVS

- $[S]$ parameters for "Passives" & PCB

- TLP Info
  - $I_t$ (slow transient)
  - $I_p$ (fast transient)
  - 100-ns Pulse IV

- CDM Info: $I_p$
- TLP Info: $I_t$
New Research: Polymer Voltage Suppressors (PVS) low capacitance ESD protection increases GHz Electronics availability by increasing reliability.

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1) Solution specific trigger voltage
2) Sub 1 ns response times
3) Extremely low capacitance
4) Freed circuit board space
5) Lower Impedance

Circuit to be protected

Courtesy: Electronics Polymers Inc.
Can this polymer be integrated into IC package?

No protection Damages IC

Polymer in IC Package

Polymer ESD Protection

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### Package ESD Sensitivity*

<table>
<thead>
<tr>
<th>Condition</th>
<th>Classification</th>
<th>Sensitivity Scale</th>
</tr>
</thead>
<tbody>
<tr>
<td>No IC Chip</td>
<td>Discretes</td>
<td>0 (None)</td>
</tr>
<tr>
<td>IC in Package</td>
<td>Memory OMAP</td>
<td>3 (Low)</td>
</tr>
<tr>
<td></td>
<td>Analog Digital</td>
<td></td>
</tr>
<tr>
<td>IC in Package</td>
<td>CMOS BiCMOS</td>
<td>4 (Low)</td>
</tr>
<tr>
<td>IC in Package</td>
<td>65nm and beyond</td>
<td>6 (Moderate)</td>
</tr>
<tr>
<td>IC in Package</td>
<td>RF CMOS</td>
<td>7 (Moderate)</td>
</tr>
<tr>
<td>IC in Package</td>
<td>RF GaAs</td>
<td>8 (High)</td>
</tr>
<tr>
<td>IC in Package</td>
<td>5-10 GHz</td>
<td>9 (Very High)</td>
</tr>
<tr>
<td>Wafer Scale</td>
<td>TBD</td>
<td>9 (Very High)</td>
</tr>
</tbody>
</table>

ESD levels <500V HBM are considered sensitive

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Summary and Outlook

• ESD is always a major concern for IC components and electronics systems that are built with these components
• Every consumer must be aware of ESD as they handle their personal electronics
• Rapid advances in technologies and circuit performance requirements are making ESD reliability into a constant challenge
Summary and Outlook

• Newer IC packages will make ESD testing even more complicated
• Integration of ESD suppressive materials into the IC package itself is one option that needs to be explored
• Package research must also address innovation towards non-exposed pins or sealed IC pins to minimize the ESD threat
• Research into ultra low capacitance package types will also be crucial for maintaining safe ESD levels for very large packages

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Research Opportunities

• Understanding of high voltage transistor behavior and optimization for ESD
• Protection device layout for on-chip system protection
• Thermal modeling for ESD
• Whole chip and IC package modeling for ESD development
• Disposable ESD protection devices
Acknowledgments

• ESD Association (ESDA)
• More information on ESD can be obtained from www.esda.org
• Mr. Dave Swenson, Affinity Static Control Consulting, LLC.
• Mr. Ted Dangelmayer, Dangelmayer and Associates
• Dr. Karen Shrier, Electronics Polymers Inc.