Half-day Symposium on Compact Modeling
Friday, May 7, 2004

12:30 PM   Registration
1:00 PM     Introduction
            Raif Hijab, SCV-Chapter EDS Chair
            Narain Arora, EDS-Compact Modeling Committee Chair

Speaker Introduction: Samar Saha and Narain Arora


2:00 PM     The Development of the Next Generation BSIM for Sub-100nm Mixed-Signal Circuit Simulation, J.
            Xi, University of California, Berkeley.

2:45 PM     A Practical Examination of MOS Transistor Model Accuracy in Modern CMOS Technology, P.

3:15 PM     Coffee Break

3:30 PM     Self-consistent Surface-Potential-based Model HiSIM: Advantages and Applications, M. Miura-
            University, Japan, *Semiconductor Technology Academic Research Center, Japan.

4:15 PM     Interconnect Modeling for Frequency-Dependent Crosstalk Noise Analysis, S. Yu, S.-P. Sim, S.

5:00 PM     Compact Modeling for Snapback-based ESD Protection, P. Jansen, V. Vassilev, N. Mahadeva, and G.
            Groeseneken, IMEC, Belgium.

5:30 PM     Modeling and Characterization of On-chip Inductance for Sub-100nm Cu CMOS Process, N. Arora,
            L. Song, Cadence Design Systems, and *V. Chang, Cadence Design Systems, *TSMC.

6:00 PM     Closing Remarks: Raif Hijab

Abstract--Moore's Law scaling has led to ultra-short channel length devices that, while giving multi-GHz performance, present a host of new challenges. This talk will look at a range of "other" issues that face compact modeling of nano-meter scale technology. This will include a growing list of parasitic effects related to: gate leakage, substrate coupling and thermal limitations. There are also issues of intrinsic device scaling; there is growing momentum for open source, high-level specifications, for models that facilitate new paradigms for model portability. This paradigm shift will be considered for both intrinsic and parasitic modeling needs.

Biography: Professor Robert Dutton attended the University of California, Berkeley where he received the B.S., M.S. and Ph.D. degrees in Electrical Engineering. He joined the faculty of Electrical Engineering at Stanford University where he has served as Director of Research at the Center for Integrated Systems (CIS) and is currently Director of the Integrated Circuits Laboratory (ICL).

His research career has focused on computer simulation of integrated circuit technology, including both models of the IC fabrication processes and electrical behavior of new transistor and circuit structures. The simulation tools and software pioneered by Prof. Dutton's group has been universally adopted by industry and used prolifically in support of technology development.

In 1980 he founded the first commercial Technology Computer Aided Design (TCAD) company, Technology Modeling Associates, that became a public company in 1996 (TMAI, Nasdaq), which merged with Avanti and is now part of Synopsys. He had industrial experience at: Fairchild Semiconductor, Bell Labs, IBM, Hewlett-Packard and Matsushita.

His awards include: IEEE Fellow, J.J. Ebers and Jack A. Morton Awards, Member of the National Academy of Engineering (NAE) and the Recipient of the Computers and Communications (C&C) Prize, Japan.

2. The Development of the Next Generation BSIM for Sub-100nm Mixed-Signal Circuit Simulation, Jane (Xuemei) Xi, University of California, Berkeley.

Abstract--This talk describes the next generation BSIM model for aggressively scaled CMOS technology. New features in the model include more accurate non-charge-sheet based physics, completely continuous current and derivatives, and extendibility to non-traditional CMOS based devices including SOI and double-gate MOSFETs.

Biography: Dr. Xuemei (Jane) Xi received her B.S., M.S. and Ph.D. degrees in electrical engineering from Peking University, Beijing, China. She became a faculty member at Peking University at 1995 and was an associate professor from 1997-1999. From 1999 to 2000, she was with Digital-DNA Laboratory, Motorola China in Beijing where she was a senior engineer and technology manager. Since November 2000, she has been the BSIM Program Manager at the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley. Her research areas include bulk, silicon-on-insulator (SOI) and Double-Gate (DG) CMOS device physics, modeling and technologies. She is also Compact-Model-Council (CMC) member and offering technical support to the BSIM3/4 users from both industry and academics.


Abstract--Compact MOS transistor models are critical infrastructure for circuit design and simulation in modern CMOS technology. However, MOS modeling has become isolated from related disciplines, and has developed less than optimum "quality of work" benchmarks and guidelines, unaffected by the needs and constraints related to circuit design use of those models. The term "model accuracy" has as a result become badly abused. In this paper, model accuracy is considered from a more practical and wide-ranging viewpoint. In particular, we look at binned versus un-binned models, refute some myths about the accuracy of each, and finally look at digital timing libraries using various "less accurate" and "more accurate" models, showing that less accurate models are in many cases quite adequate with significant advantages over more accurate models.

Biography: Dr. Peter Bendix received a B.S. degree in physics from Caltech in 1968 and a Ph.D. in theoretical particle physics from the University of British Columbia, Canada, in 1973. He worked for Etec, AMD, VLSI Technology, TMA (Technology Modeling Associates), and now LSI Logic in various roles related to bipolar and MOS device modeling, characterization, and management. He is currently the director of device technology at LSI Logic.

Abstract--Conventionally MOSFET models are described as a function of applied voltages. Due to severe approximations applied for deriving the description the model accuracy is no more sufficient for advanced MOSFET circuits utilizing limiting device performances. Here we present the MOSFET model HiSiM, developed based on the physical approach of a self-consistent surface-potential solution. Its advantages and applications will be demonstrated.

Biography: Professor Mitiko Miura-Mattausch received the Dr. Sc. degree from Hiroshima University. She joined the Max-Planck-Institute for solid-state physics in Stuttgart, Germany as a researcher from 1981 to 1984. From 1984 to 1996, she was with Corporate Research and Development, Siemens AG, Munich, Germany, working on hot-electron problems in MOSFETs, the development of bipolar transistors, and analytical modeling of deep submicron MOSFETs for circuit simulation. Since 1996, she has been a professor in the Department of Electrical Engineering, Graduate School of Advanced Sciences of Matter at Hiroshima University, leading the ultra-scaled devices laboratory.


Abstract--An interconnect model suitable for frequency-dependent crosstalk noise simulation in deep sub-micron designs is presented. It efficiently represents self and mutual impedances and takes into account multiple return paths provided by the power/ground grid. The power grid is transformed into a single effective return path and modeled to capture frequency-dependent characteristics. The parameters of the transformed system are calculated for three frequency regimes and an RL ladder network is constructed to model frequency-dependent behavior. The lumped circuit representation is constructed using our model, and investigated for various input rise times. SPICE simulation confirms that our model accurately adjusts for changes in input rise time. While a conventional noise simulation yields the waveforms at only a single frequency, our model accurately provides crosstalk noise over a wide frequency range. Further, a complete modal analysis is introduced to derive the crosstalk voltage waveform in multiconductor coupled systems. In addition to the capacitance and inductance matrices, it also includes a resistance matrix. The off-diagonal terms of the resistance matrix are related to the return path, which is important for accurate noise modeling at high frequency. It is shown that the error in crosstalk peak noise can be as high as 30% if the return path resistance is ignored.

Biography: Sunil Yu received the B.S. degree in Physics from Seoul National University in 1989 and M.S. degree from Pohang Institute of Science and Technology (POSTECH) in 1991. From 1991 to 2002, he was with Semiconductor Division, Samsung Electronics, where he worked on the development of logic process integration, especially 0.35(m and 0.18(m processes. Since 2002, he has been working toward the Ph.D degree in Electrical Engineering from Korea Advanced Institute of Science and Technology (KAIST). He is currently a visiting researcher in the Center for Nanostructures at Santa Clara University. His research interests include on-chip interconnect crosstalk noise and related issues in VLSI circuits.


Abstract--The development of circuit and device Electrostatic Discharge (ESD) response simulation tools is one of the critical reliability challenges for implementing the ITRS roadmap. This talk presents an approach for compact modeling of the ESD stress domain (current ~ [A], time ~ [ns]) breakdown and snapback behavior of state-of-the-art MOSFET structures for pre-silicon ESD protection circuit optimization. The impact of the technology downscaling on the MOSFET snapback characteristics will be discussed, including the increased breakdown regime tunneling currents and electric fields. An equivalent circuit model will be presented together with its implementation in SPECTRE, using SPECTRE AHDL. The model parameter extraction methodology will be outlined, including the implementation in IC-CAP. Application examples using the snapback MOSFET models for optimization of the ESD protection behavior of digital I/O cells and verification examples will be presented and discussed.

Biography: Dr. Philippe Jansen received the M.S. degree and the Ph. D. degree in Electrical Engineering from the K.U. Leuven, Belgium in 1988 and 1993 respectively. He worked as a post-doctoral researcher
at Hitachi, Central Research Laboratories, Tokyo, Japan from 1993 to 1994. He is working for IMEC since 1994 in various functions in the field of advanced CMOS integration, packaging and reliability (ESD research). He is a member of technical staff and also manages the US business development office for IMEC.


Abstract-- On-chip inductance modeling has become important as IC operating speed increases and processing technology node advances. With the introduction of low resistive copper as interconnect material, the effect of interconnect inductance becomes more significant in sub 100nm Cu CMOS process. In this presentation we will discuss results of on-chip inductance obtained from a test chip that was fabricated by a 90nm Cu CMOS process. The test structures were designed to study various inductive return paths and inductance impacts. High speed S parameter and ring oscillator measurements were used to characterize inductive effects. The inductive effects of sub-100nm Cu interconnects vs. sub-μm Al interconnects are compared and discussed.

Biography: Narain Arora, Ph.D., Fellow IEEE, is the Vice President of Technology at Cadence Design Systems. Prior to that (1996-2002) he was Vice President and Chief Scientist at Simplex Solutions. Before joining Simplex, he held several engineering and management positions within DEC's semiconductor division over a period of 14-years. The most recent being consulting engineer and manager of DEC's device and interconnect modeling group. His field of interest is semiconductor process/device design and modeling/characterization including VLSI device/circuit reliability simulation and parasitic (interconnect) modeling and extraction. He has given various invited talks and published over 55 journal papers, has 3 patents to his credit and authored a book "MOSFET Modeling for VLSI Circuit Simulation: Theory and Practice", pp. 596. Springer-Verlag, NY 1993.