A Single-Chip Quad-Band GSM/GPRS Transceiver in 0.18µm Standard CMOS

Berkäna Wireless Inc.
Campbell, California
Desired Features of Commercial Radios

- Low Cost
- Small Form Factor
- Long Range
Presentation Outline

• GSM/GPRS Implementation Challenges
• Transceiver Architectural Tradeoffs
• CMOS Quad-Band GSM/GPRS Transceiver
• Test Results
• Conclusions
Key Receiver Specifications

GSM 900 Blocking Profile

- Range of the Mobile => Sensitivity < -102dBm
- Near-Far Problem => Large Dynamic Range
- Presence of Nearby Users => IIP3 > -17dBm
Key Transmitter Specifications

**TX Noise in RX Band**

- Transmit Band: 20MHz
- Spacing: 20MHz
- Receive Band: freq

- Receive Band Noise at 20MHz offset, PN < -162dBc/Hz
- Modulation Mask at 400kHz offset requires high linearity and low phase noise
- Modulation Accuracy of: $\phi_{RMS} < 5^\circ$

**Modulation Mask**

- Requirement
- - 60dBc
- $f_C$, 400 kHz

- +33dBm
- < -162dBc/Hz
RX Direct Conversion

Properties of Direct Conversion

+ Low frequency signal facilitating programmable filters
- Problematic 1/f, DC offset and IP2 interference
Low IF Receiver

Properties of Low-IF Receivers

+ Less susceptible to low frequency interference
- Image rejection must be addressed
+ Leverage narrowband signal to facilitate integration
Direct Conversion Transmitters

Properties of Direct Conversion Transmitters

- Single conversion eliminates IF filter
- Requires Pre-PA filter for harmonic rejection
- Wideband modulator noise demands filtering
TX Offset Phase-Locked Loop

- PLL frequency translates phase modulated signal
- PLL transfer function filters mixer spurs and noise
- More design complexity compared to Direct Conversion
- Leverage narrowband signal to enable integration
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Quad-Band GSM/GPRS Transceiver
PLL Phase Noise vs. Settling Time

![PLL Diagram](image)

- **Phase Noise @ 3MHz**
  - dBc/Hz vs. \( C_2 \)

- **PLL Settling Time**
  - µs vs. \( C_2 \)

- Reference Oscillator
- Loop Filter
- PFD
- CP
- N/N+1
- VCO
- TX & RX LO Input

Equations:
- \(-146\) dBc/Hz
- \(-146\) dBC/Hz
Typical PLL Settling Characteristics

- VCO calibration minimizes control voltage range
- Small charge pump current

\[ T_{\text{Slew}} = \frac{C_2 \cdot V_{dd}/2}{I_{CP}} \]
Principle of Fast Charging PLL

Range of $V_C$ (Post VCO Calibration)

$T_{Slew} = \frac{C_2 \times V_{dd}/2}{I_{Boost}}$

- VCO calibration minimizes control voltage range
- Small charge pump current
PLL Fast-Charge Amplifier

Class AB Amplifier

\[ V_{dd}/2 \rightarrow V_i \rightarrow \text{PC} \]

\[ V_o = V_c \]

\[ V_o \leq V_{dd}/2 \]

\[ I_{Boost} \geq 15mA \]

\[ C_2 \]

\[ V_{CO} \]

\[ R_1 \]

\[ C_1 \]

\[ M_z \]
Receiver RF and IF

- Fully differential signal path
- Complex Butterworth filter response
- Receive gain is 100dB in 2dB steps
High-Band RF Front End

Band Sharing LNA Loads

Folded Mixer

DCS Band  PCS Band
Receive IF Filter and PGA Stage
Transmit Output Driver

- Rail-to-Rail Signal Path
- Ko Push-Pull Driver
- $P_O \approx i_{op}^2 R_{LOAD}/2$
- Minimal Area
Principle of the Ko Push-Pull Amp

High Input State

Low Input State

\[ V_I \rightarrow \text{Mp} \rightarrow V_O \rightarrow C_{ac\_couple} \rightarrow i_{odn} \rightarrow \text{LOAD(Effective)} \]

\[ V_I \rightarrow \text{Mn} \rightarrow V_O \rightarrow C_{ac\_couple} \rightarrow i_{odp} \rightarrow \text{LOAD(Effective)} \]

\[ V_{dd} \]

\[ V_I \]

\[ r_{onn} \rightarrow r_{onp} \rightarrow \sim Z_{out} \]
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→ • Test Results

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Chip Radio Evaluation Board

- SAW Filters & Matching
- VC-TCXO
- Quad-Band Transceiver
- Power Amp Module
- Antenna Switch Module
PLL Settling Time

w/ Fast Charge Amp.

w/o Precharge Amp

PLL settling time of 150\(\mu s\)
Receiver Sensitivity (EGSM900)

3GPP GSM Spec (-102dBm)

Measured EGSM Sensitivity
In-Band Blocker Performance (PCS)

- Blocker Offset Frequency (MHz)
- Margin Relative to 3GPP
- Measured Blocker Level
- 3GPP Spec for Blocker Level Input at Antenna

-50 -40 -30 -20 -10 0 10 20 30 40 50

-50 -44 -38 -32 -27 -21 -15 -9.2 -3.4 3.4 9.2 15 20.4 26.2 32 37.8 43.6 49.4

-26dBm
TX Modulation Mask & Phase Error

EGSM900 Modulation Mask

-400.000 kHz
-66.828 dB

EGSM900 RMS Phase Error

Phase Error:
1.03 ° rms
2.89 ° pk
at bit 70.40

Freq Error:
-9.85 Hz
I/Q Offset:
-41.13 dBc
Avg Type:
Maximum
T0 Offset:
---

File Operation Status: A:\EGSM900LIM file loaded

File Operation Status: A:\SCREEN069.601 file saved
TX Phase Error at PA Output (PCS)

- Peak Phase Error
- RMS Phase Error
- 3GPP Required Peak Phase Error
## Receiver Performance Summary

<table>
<thead>
<tr>
<th>Receiver Measurements</th>
<th>GSM850 / EGSM900</th>
<th>DCS1800 / PCS1900</th>
</tr>
</thead>
<tbody>
<tr>
<td>Noise figure (dB)</td>
<td>2.7</td>
<td>2.7</td>
</tr>
<tr>
<td>Input IP3 (dBm)</td>
<td>-15</td>
<td>-15</td>
</tr>
<tr>
<td>Input IP2 (dBm)</td>
<td>40</td>
<td>40</td>
</tr>
<tr>
<td>RX gain (dB)</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>Sensitivity at antenna (dBm)</td>
<td>-110</td>
<td>-109</td>
</tr>
<tr>
<td>RX current (mA)</td>
<td>93</td>
<td>95</td>
</tr>
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</table>
## Transmitter Performance Summary

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<tr>
<td>RMS Phase Error (degrees)</td>
<td>1.0</td>
<td>1.2</td>
</tr>
<tr>
<td>Output Modulation Spectrum at 400kHz Offset (dBc)</td>
<td>-66</td>
<td>-65</td>
</tr>
<tr>
<td>Noise at 20MHz Offset (dBc/Hz)</td>
<td>-165</td>
<td>-162</td>
</tr>
<tr>
<td>Worst Case PLL settling time (µs)</td>
<td>160</td>
<td>160</td>
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<tr>
<td>Output Power (dBm)</td>
<td>+6</td>
<td>+6</td>
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<tr>
<td>Carrier Suppression (dBc)</td>
<td>40</td>
<td>40</td>
</tr>
<tr>
<td>Sideband Suppression (dBc)</td>
<td>45</td>
<td>45</td>
</tr>
<tr>
<td>Current (mA)</td>
<td>108</td>
<td>112</td>
</tr>
</tbody>
</table>
Conclusions

• Single-Chip CMOS Transceiver Demonstrates Cellular Performance

• Low Power/Noise Inductorless PA driver

• Fast Settling PLL Supports GPRS Class 12 Operation

• State of the Art RX Sensitivity Performance in Standard CMOS