5.5: A 3.2 to 4GHz, 0.25μm CMOS Frequency Synthesizer for IEEE 802.11a/b/g WLAN

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Outline

- System Requirements
- Architecture and Circuit Description
- Measurements
- Conclusions
Design Goals

- Tuning Range 3.2 - 4.0 GHz

- Reference Frequencies:
  13.33M, 6.66M, 3.33M, 10M

- Drive LO Buffers at $f_{VCO}$ and
  I,Q LO Buffers at $f_{VCO}/2$

- Low Phase Noise

- Low Spurs
Design Choices

- **Low VCO gain**
  - Good VCO phase noise
  - Low LPF resistor noise contribution

- **High charge pump current**
  - Low LPF resistor noise contribution
  - Low charge pump noise
Voltage Controlled Oscillator (VCO)

Regulated $V_{DD}$ (2.5V)

7-bit control
High-Frequency Divide-by-2

Adjustable Tuning

Adjustable C

\[ R_p = L \omega Q \]

Equivalent parallel resistance

Adjustable L

ampl vs freq

freq
Multi-tap Inductors
Charge Pump

Regulated $V_{DD}$

Control Voltage

Replica Bias

$I_{BIAS}$

$C_P$

$M_P$

$C_N$

$M_N$

$+ -$

$dn$

$up$

$dn$

$up$
Programmable Integrated LPF

$R_{\text{series}}$, $C_{\text{series}}$, $C_{\text{parallel}}$, $V_c$
8/8.5 Dual Modulus Divider

Phase Multiplexer

\[ V_{DD} \]

\[ \text{out} \quad \text{out} \]

\[ f_4 I \quad f_4 I \quad f_4 Q \quad f_4 Q \]

\[ s_0 \quad s_0 \quad s_1 \quad s_1 \quad s_2 \quad s_2 \quad s_3 \quad s_3 \]

\[ \text{VDD} \]

\[ \text{out} \]

\[ \text{VDD} \]

\[ \text{VDD} \]
Control Logic

- Successive approximation search for the 7 bits that control the VCO tuning capacitors
- Coarse digital alignment of the feedback clock with the reference clock
- Optimize for the control voltage value
- Take corrective action when the control voltage drifts out of the acceptable range or when no-lock is detected
Measurement Setup

- 802.11a Transmitter
- 4.8 - 6 GHz RF output

DC Input
- $BB_I$
- $BB_Q$
- $f_{VCO}/2$
- $f_{VCO}$

40MHz

- Measured Phase Noise at RF output is ~3.5 dB higher than at the VCO frequency.
$F_o=5.44\text{GHz}, \ F_{\text{ref}}=13.3\text{MHz}, \ (S=0)$
Output Spectrum (2)

\[ F_o = 5.30 \text{GHz}, \quad F_{\text{ref}} = 13.3 \text{MHz}, \quad (S=9) \]
Measured Phase Noise (1)

**F_{out}=5240MHz, F_{ref}=13.3MHz**

Phase Noise (dBc/Hz)

-105 dBc/Hz

-107 dBc/Hz

-115 dBc/Hz
Measured Phase Noise (2)

\( F_{\text{out}} = 5240 \text{MHz}, \quad F_{\text{ref}} = 13.3 \text{MHz} \)

VCO Phase Noise: \(-121 \text{ dBc/Hz}\)

@ 1MHz offset, 5.24 GHz carrier
Measured Phase Noise (3)

- $F_{out}=5745M, F_{ref}=3.33M$
- $F_{out}=5250M, F_{ref}=6.66M$
- $F_{out}=5240M, F_{ref}=13.3M$

Phase Noise (dBc/Hz)

Frequency Offset (Hz)
# Performance Summary

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.25 µm CMOS, 1P5M, MIM capacitors</th>
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<tbody>
<tr>
<td>Power Dissipation</td>
<td>93 mW</td>
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<tr>
<td>Area</td>
<td>1.7 mm(^2)</td>
</tr>
<tr>
<td>Spot Phase Noise</td>
<td></td>
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<tr>
<td>(F_{\text{out}} = 5240\text{MHz}, F_{\text{ref}} = 13.3 \text{ MHz})</td>
<td>-105/-107/-115 dBc/Hz @ 10K/100K/1M</td>
</tr>
<tr>
<td>Integrated PN (from 1K to 10M)</td>
<td></td>
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<tr>
<td>(F_{\text{out}} = 5240\text{MHz}, F_{\text{ref}} = 13.3 \text{ MHz})</td>
<td>-45.3 dBc (0.31°)</td>
</tr>
<tr>
<td>(F_{\text{out}} = 5250\text{MHz}, F_{\text{ref}} = 6.66 \text{ MHz})</td>
<td>-43.3 dBc (0.40°)</td>
</tr>
<tr>
<td>(F_{\text{out}} = 5745\text{MHz}, F_{\text{ref}} = 3.33 \text{ MHz})</td>
<td>-40.9 dBc (0.54°)</td>
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<tr>
<td>Spurs</td>
<td>&lt;=-64dBc</td>
</tr>
<tr>
<td>Settling Time</td>
<td>&lt;150µs</td>
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</table>
Synthesizer Micrograph
Conclusions

- Fully integrated, wideband, 0.25\(\mu\)m CMOS synthesizer

- Excellent phase noise, spur performance and settling time

- Design highlights:
  - On-chip voltage regulation
  - Tuning with switching inductors
  - Low noise VCO
  - Charge pump topology