5.4: A Single-Chip, Dual-Band, Tri-Mode CMOS Transceiver for IEEE 802.11a/b/g Wireless LAN

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Outline

- Introduction
- Overall System Architecture
- Circuit Design
  - Receiver
  - Transmitter
- Summary
### IEEE 802.11 Wireless LAN

<table>
<thead>
<tr>
<th></th>
<th>IEEE 802.11a</th>
<th>IEEE 802.11b</th>
<th>IEEE 802.11g</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Available Spectrum</strong></td>
<td>555MHz</td>
<td>83.5MHz</td>
<td>83.5MHz</td>
</tr>
<tr>
<td><strong>Frequency of Operation</strong></td>
<td>5.150 - 5.350 GHz, 5.470 - 5.825 GHz</td>
<td>2.400 - 2.483 GHz</td>
<td>2.400 - 2.483 GHz</td>
</tr>
<tr>
<td><strong>non-overlapping channels</strong></td>
<td>27</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td><strong>Modulation</strong></td>
<td>OFDM</td>
<td>CCK</td>
<td>CCK/OFDM</td>
</tr>
<tr>
<td><strong>Data Rate</strong></td>
<td>6 - 54 Mbps</td>
<td>1 - 11 Mbps</td>
<td>1 - 11 Mbps, 6 - 54 Mbps</td>
</tr>
</tbody>
</table>
Overall System Architecture

- Digital Baseband
- Radio Transceiver
- DAC
- ADC
- Digital Core
- Control
- RX/TX Switch
- Balun
- Dual-Band Antenna (I)
- Dual-Band Antenna (II)
- External PA (Optional)
- Transmitter
- Receiver
- Dual Transmitter
- Synthesizer
- Dual Receiver
- 5G
- 2.4G
- External LNA (Optional)
Transceiver Architecture

- Dual conversion with sliding IF
  - Low LO leakage
  - Weak LO pulling
  - No need for complicated DC offset cancellation
  - Can be designed to have comparable power dissipation to direct conversion
Frequency Plan

5GHz Mode

LO₁ = 2/3 f_RF

LO₂ = 1/3 f_RF

2.4GHz Mode

LO₁ = 2/3 f_RF

LO₂ = 1/3 f_RF

IF

5GHz Band

2.4GHz Band

672MHz

☐ Share the signal path between different modes
  • Reduce the die size
Low-Noise Amplifier (LNA)

Overall Receiver NF = 4.5/5.5dB @ 2.4/5GHz
Receiver Baseband Filters

Replica Biquad → Phase Detector → State Machine

10MHz

Low-Q Biquad → High-Q Biquad → Transresistance Amplifier

V_{in} → V_{out}

I_{in} → -g_{m3} → g_{m1} → g_{m3} → g_{m4} → I_{out}

Calibration Loop
Baseband Filters Frequency Response
Over Process and Temperature
5GHz Receiver Linearity

![Graph showing 5GHz Receiver Linearity with RF Input (dBm) on the x-axis and Baseband Output (dBm) on the y-axis. The graph includes points for Fundamental and IM3, with IIP3 = 5dBm highlighted.]
5GHz Receiver Sensitivity

- Sensitivity (dBm)
- Channel Frequency (MHz)

- 64QAM, 54Mbps
- BPSK, 6Mbps
Transmitter Block Diagram

5GHz

PA

LO$_2$ = $\frac{2}{3}f_{RF}$

Q

I

LO$_1$ = $\frac{1}{3}f_{RF}$

2.4GHz

PA

RF Gain Control

672 MHz

Q

I

Baseband Gain Control

$\frac{2}{3}f_{RF}$

RC-CR

$\frac{2}{3}f_{RF}$
Transmitter Baseband Filters

- 3rd order Butterworth, with $f_{3dB} = 15$MHz
- Needs to be flat within 0.5dB in the passband
- Requires 40dB attenuation at the DAC sampling frequency of 160MHz
- No auto-tuning required
PA with Dynamic Biasing

Conventional Class A

Dynamically Biased

- OFDM signal has a 17dB peak-to-average ratio
- BUT signal peaks are infrequent
Simplified PA Block Diagram

Pre-drivers

PA

Envelope detectors

1/α

Input → Pre-drivers → PA → Output

Envelope detectors
Simplified PA Schematic

- **Envelope Detector**
- **Dynamic Bias**
- **Fixed Bias**

PA Input (PA_in)

S1

Dynamic Bias

C1

2.4GHz: Psat = 26dBm
5GHz: Psat = 19dBm

C2

M1

M2

PA Output Stage
1/2 of the differential circuit

3.3V

PA Output (PA_out)
2.4GHz PA Characteristics

64-QAM

- EVM (dB)
- Pout (dBm)

Ipa = 130mA
Dynamic Bias

I_{Dynamic} = 130mA
5dB

I_{Dynamic} = 50mA

I_{Dynamic} = 65mA
2.4GHz Transmitter Performance

EVM @ $P_{out} = 5$dBm

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>EVM</td>
<td>-32.32 dB</td>
</tr>
<tr>
<td>Mag Error</td>
<td>-34.62 dB</td>
</tr>
<tr>
<td>Phase Error</td>
<td>1.41 deg</td>
</tr>
<tr>
<td>Rate</td>
<td>54 Mbps</td>
</tr>
</tbody>
</table>

IEEE 802.11g OFDM Mask

Spectral Mask
Synthesizer Phase Noise

Measured at the RF output

Phase Noise (dBc/Hz) vs. Frequency Offset (Hz)

-5 GHz
-2.4 GHz
Die Micrograph

Dual RX

2.4GHz PA

5GHz PA

Dual TX

Synth 1

Synth 2

Bias

Control
# Measured Performance

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.25 µm CMOS, 1P5M</th>
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<tbody>
<tr>
<td><strong>Transmitter Power Dissipation</strong></td>
<td></td>
</tr>
<tr>
<td>2.4 GHz</td>
<td>741 mW @ Pout = 5 dBm</td>
</tr>
<tr>
<td>5 GHz</td>
<td>710 mW @ Pout = 5 dBm</td>
</tr>
<tr>
<td><strong>Receiver Power Dissipation</strong></td>
<td></td>
</tr>
<tr>
<td>2.4 GHz</td>
<td>370 mW</td>
</tr>
<tr>
<td>5 GHz</td>
<td>320 mW</td>
</tr>
<tr>
<td><strong>TX EVM</strong></td>
<td></td>
</tr>
<tr>
<td>2.4 GHz</td>
<td>-32 @ Pout = 5 dBm</td>
</tr>
<tr>
<td>5 GHz</td>
<td>-30 @ Pout = 5 dBm</td>
</tr>
<tr>
<td><strong>RX Noise Figure</strong></td>
<td></td>
</tr>
<tr>
<td>2.4 GHz</td>
<td>4.5 dB</td>
</tr>
<tr>
<td>5 GHz</td>
<td>5.5 dB</td>
</tr>
<tr>
<td><strong>Phase Noise @ 100 kHz offset</strong></td>
<td></td>
</tr>
<tr>
<td>2.4 GHz</td>
<td>-109 dBC/Hz</td>
</tr>
<tr>
<td>5 GHz</td>
<td>-107 dBC/Hz</td>
</tr>
</tbody>
</table>
Conclusions

- IEEE 802.11a/b/g radio transceiver in 0.25 µm standard CMOS
- No external filters
- Sharing of the blocks between the 2.4 and 5GHz modes of operation: reduced die size
- Integrates:
  - Dual-band Receiver
    - 4.5/5.5dB noise figure for 2.4/5 GHz
  - Dual-band Transmitter
    - -32/-30dB EVM @ Pout=5dBm for 2.4/5 GHz
  - Frequency Synthesizers
    - -109/-107 dBc/Hz @100KHz offset for 2.4/5GHz
Acknowledgements