Circuit Technologies for Multi-Core Processor Design

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Outline

• Dual-core architectural directions
• Interconnect trends
• Power and leakage reduction
  – Cache Sleep and Shut-off Modes
  – Long-Le Transistor Usage
• Voltage domains
• Clock distribution
• Package details
• DFT/DFM features
• Thermal management
• Summary
Dual Core Processors Everywhere!

Intel tips Viiv, Yonah in consumer push
Mark LaPedus, 01/06/2006
SAN JOSE, Calif. — Making a big splash in the consumer market, Intel Corp. on Thursday unveiled a dual-core processor, PC platform and several content alliances that are said to provide the foundation for digital entertainment and wireless laptops.

Intel unwraps dual-core Xeon server processors
Tom Krazit, 10/10/2005
At an event Monday in San Francisco, Intel unveiled its first dual-core Xeon chips for two-processor and four-processor servers, previously known by the Paxville code name.

Intel ready to ship dual-core processors
Daniel A. Begun, 3/15/2005
Earlier this year, Intel announced that desktop processors using dual-core technology will be available by the end of June, but the company recently hinted at March's Intel Developer Forum (IDF) that dual-core processors could be available even sooner than that.
Tulsa – Xeon® Processor

- Process technology: 65 nm, 8 Cu interconnect layers
- Transistor count: 1.328 Billion
- Die area: 435 mm²
Montecito – Itanium® 2 Processor

- Process technology: 90nm, 7 Cu interconnect layers
- Transistor count: 1.72 Billion
- Die area: 596mm²
Yonah – Mobile/Desktop/Blade Server

- Process technology: 65 nm, 8 Cu interconnect layers
- Transistor count: 151 Million
- Die area: 90.3 mm²
Process technology scaling enables the number of cores to double every two years.
Server Processors L3 Cache Trend

On-Die L3 Cache [MB] vs. Process Technology Node

Cache size doubles with every process generation

- Xeon® Processors
- Itanium® Processors
SRAM Cell Size Scaling

SRAM cell size scales ~0.5x per generation
Server Processors L3 Cache Trend

<table>
<thead>
<tr>
<th>Dual-core Processor</th>
<th>Process</th>
<th>L3 cache per core [MB]</th>
<th>L3 cache per thread [MB]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Itanium®</td>
<td>90nm</td>
<td>12</td>
<td>6</td>
</tr>
<tr>
<td>Xeon®</td>
<td>65nm</td>
<td>8</td>
<td>4</td>
</tr>
</tbody>
</table>

Large per-core and per-thread caches enable server-class performance.
On-chip Interconnect Trend

- Local interconnects scale with gate delay
- Global interconnects do not scale

Source: ITRS
Layout Techniques to Reduce Coupling

- Interleave bussed signals with other busses that switch at a different time
  - Eliminates capacitive coupling and reduces inductive noise

- Switch bit order of bussed signals at every turn
  - Noise will not be additive across the entire bus route
Layout Techniques (Cont)

• Interleave narrow Vcc/Vss lines through bus

• Use staggered inverting buffers [7]
L3 Cache Sleep and Shut-off Modes

**Active Mode**
- Sub-array
- Virtual VSS
- Block
- Select
- Sleep Bias
- Shut off

**Sleep Mode**
- Sub-array
- 2x lower leakage
- 250mV

**Shut-off Mode**
- Sub-array
- 520mV

Voltage

- 0V
- 1.1V
Leakage Shut-off Infrared Images

16MB SKU
All 16MB in sleep mode

8MB SKU
8MB in sleep mode
8MB in shut-off mode

Shut-off feature reduces the leakage of the 8MB disabled sub-arrays by about 3W
Dynamic Intel® Smart Cache Sizing

• First implementation in Yonah dual-core mobile processor
  – Dynamic implementation of the shut-off mode

• HW based algorithm predicts cache usage requirements
  – Considers the % of time the CPU is in Active state compared to the various sleep states

• During periods of low activity or inactivity the processor dynamically adapts its effective cache size
  – Cache content is gradually flushed to system memory
  – Cache ways are gradually turned off (physically as well as logically), thus reducing power

• Cache ways are re-powered on demand to deliver full performance when needed
Leakage Mitigation: Long-Le Transistors

- All transistors can be either nominal or long-Le
- Most library cells are available in both flavors
- Long-Le transistors are about 10% slower, but have 3x lower leakage
- All paths with timing slack use long-Le transistors
- Initial design uses only long channel devices
Long-Le Transistors Summary

Percentage of Long-Le device width excluding RAM arrays:

- **Cores**
  - Nominal: 46%
  - Long-Le: 54%

- **Uncore**
  - Nominal: 24%
  - Long-Le: 76%

To reduce sub-threshold leakage, most devices will be slower and only a handful of transistors will be fast.
Stack Forcing

Equal Loading

\[ W = W_u + W_l \]

- Force one transistor into a two transistor stack with the same input load
- Can be applied to gates with timing slack
- Trade-off between transistor leakage and speed

[Narendra, et al – ISLPED 2001]
Montecito Voltage Domains [2]

Core 0, frequency tracks voltage, 40W

Core 1, frequency tracks voltage, 40W

12MB L3 cache, asynchronous operation, 2.5W

Bus Arbiter
Fixed frequency, 2.5W

Foxton Control
1GHz fixed frequency

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Tulsa Voltage Domains

- Core
- PLL
- Uncore
- I/O

Voltage Profile
Cut Line

1.25V
- Cores
- Ctrl + Tag
- 16MB array

0.25V
- Virtual VSS

1.10V

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Tulsa Clock Domains [4]

Legend:
- **Core**
- **PLL**
- **Uncore**
- **I/O**

System Clock (BCLK)
Tulsa Uncore Clock Distribution [4]

- PLL (Clock Generator)
- Core dense MCLK grid
- Un-Core ZCLK grid
- Un-Core pre-global ZCLK spine
- Un-Core sparse SCLK grid
- Un-Core pre-global MCLK spine
- De-skew buffer

Vertical clock spines
Horizontal clock spines
Montecito Clock System [5]

Fixed Supply
- Pins
- Fuses
- Frequency Translation Table
- Divisors

Core0
- PLL
- 1/M

Core1
- Foxton
- I/Os
- Bus Logic

Bus Clock
- 1/1

Variable Supply
- RVD
- RAD
- SLCB

Balanced Tree Clock Distribution
- CVD
- Gater
- 1/N

Balanced Tree Clock Distribution Components:
- CVD
- Gater

Balanced Tree Clock Distribution Connections:
- DFD
- SLCB
- RAD
- PLL

Frequency Translation Table Connections:
- Fuses
- Pins

Phase Aligner Connections:
- CVD
- Gater
- 1/N

Bus Logic Connections:
- DFD
- SLCB
- RAD

Foxton Connections:
- DFD
- SLCB
- RAD

Core Connections:
- DFD
- SLCB
- RAD

PLL Connections:
- DFD
- SLCB
- RAD

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Montecito Clock Distribution [6]

- **L0 route**
  - Bus Logic
  - REPEATERS
  - Bus Clock
  - PLL
  - core0
  - core1
  - Foxton
  - IOs

- **L1 route**
  - DFD
  - DFD
  - DFD
  - DFD

- **L2 route**
  - SLCB
  - RAD
  - SLCB
  - CVD
  - GATERS

- **L3 Route**
  - Latches
  - Latches
  - Latches
  - Latches

**Fixed frequency**
- Low Voltage Swings

**Variable Frequency**
- Full Rail Transitions

**Differential**

**Single Ended**

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Single-Ended vs. Differential Clocks

• Differential clock
  – Lower skew
  – High power
  – Longer distance between repeaters

• Single-ended clock
  – Lower power
  – Need sharp edges to control skew
Dense vs. Sparse Grid Tiles

Core Full Grid Tile

Un-Core Sparse Tile

Un-Core Dense Tile
Xeon® Processor Package

- 12 layers organic package (53.3 mm/side)
- 4-4-4 stacking
- Integrated heat spreader (38.5 mm/side)
- 604 total pins
- 366 signal I/Os
- System management components and decoupling capacitors on package
Itanium® 2 Processor Package

Power delivery connector

Heat spreader

Decoupling Caps

System Management Components
Intel® Core™ Duo Processor Package
Design for Test and Debug Features

Die-level DFT/DFM
- Parallel structural core test with XOR
- Scan and observability registers (scan-out)
- Three TAP controllers (core0, core1, uncore)
- Within-die process monitors
- On-die clock shrink

L3 cache DFT/DFM
- Built-in pattern generator (PBIST)
- Programmable weak-write test
- Low-yield analysis
- Stability test mode
- 32-entry cache line disable (Pellston)

FSB DFT/DFM
- I/O loopback
- I/O test generator
Itanium® 2 Thermal Map

- Two thermal sensors per core
- Mux thermal diodes into VCOs to measure temp
Xeon® Infra-red Emission Image

Temperature Sensors

Thermal Diode
Potential Multi-Core Thermal Control

- Multiple core designs require a central thermal management unit and an efficient mechanism for transmitting thermal sensor measurements [8]
Summary

- Dual-core processors cover the entire compute spectrum, from laptops, to desktop and servers
- Moore’s Law applied to multi-core processors:
  - Process technology scaling enables number of cores and cache size to double every two years
- Power and leakage reduction circuit techniques are essential for multi-core processors
  - Massive Long-Le usage → many slow transistors and a few fast devices
  - Cache sleep and shut-off modes (static and dynamic)
- Multiple on-die clock and voltage domains are required to control active power and leakage
  - Need new verification tools and automated checks
References