Architectures and circuits for time-interleaved ADC’s

Sandeep Gupta
Teranetics, Santa Clara, CA
Outline

• Introduction to time-interleaved architectures.
• Conventional Sampling architectures and their application space:
  – High accuracy (>7ENOB) for relatively lower sampling speeds (<1GS/s)
  – High sampling speeds, >1GS/s, up-to 20GS/s, lower accuracy (<7 ENOB)
• Proposed architecture (ISSCC 2006) for broader application space.
• Measured results for a 1GS/s 11 bit ADC based on the proposed architecture.
Time-interleaved architectures

- Time interleaved architectures:
  - Efficient architectures for achieving accuracy at high speed.
- Caveats: SNR limitations due to
  - Gain & Offset mismatches: Present in all time-interleaved architectures.
  - Phase & bandwidth mismatch: Dominant only in some time-interleaved architectures.
Mismatch errors: Intuitive reasoning

Nyquist ADC, NOT interleaved

Sub-sampled ADC outputs, time-interleaved output

Sub-sampled ADC outputs recombined with perfectly matched array

All periodic repetitions cancel except at integer multiples of Fs
Offset, gain, Phase Skew and bandwidth mismatch

Sub-sampled ADC outputs

Offset mismatch

Gain mismatch

Phase, bandwidth mismatch

Magnitude independent of signal freq.

Magnitude dependent on signal freq.
Phase and bandwidth mismatches

• Phase mismatch:
  – Systematic mismatches in clocks
    • Layout ΔRC effects
    • generation of sub-sampled clocks
  – Random mismatch in clocks
    • Jitter

• Sampling bandwidth mismatches
  – Primarily due to mismatch in switch resistance, layout ΔRC effects.
  – Dominant mechanism the phase shift caused by different sampling bandwidths.
SNDR vs. phase/bandwidth mismatch

- SNDR $\sim \alpha - 20 \cdot \log_{10}(\text{phase error})$
- Phase error (jitter/skews) $= 2\pi \cdot \text{fin} \cdot (\sigma_j / \text{fs})$
  - Wherein, $\sigma_j$ is the RMS jitter OR the standard deviation of the clock skew
  - $\text{fs}$, the sampling clock frequency
- Phase error due to sampling bandwidth mismatch $= 2\pi \cdot \text{fin} \cdot \sigma_N / f_{BW}$
  - Wherein $f_{bw}$ is the sampling bandwidth of a normalized sub-channel.
  - Wherein $\sigma_N$ is the standard deviation of the bandwidth mismatch between sub-channels.
SNDR vs. interleaving factor

- SNDR $\alpha - 10\log_{10}{[1-1/N]}$, mismatch $\sigma$ being constant. (Ref: Seng Pan U et. al., IEEE trans. Inst. and measurement, Aug. 2004.)

- However, physically mismatches (systematic/random) can increase with N (not taken in account in graph above)
Conventional Architectures and their application landscape
Conventional architecture 1

Advantage:
1. Phase skews in p<i>, Bandwidth mismatch errors, not much loss of accuracy.

Disadvantages:
1. N/2 Sub-ADCs loading on first sampler limits its BW, performance,
   - Sub-ADC sampling speed still high, if N kept low.
2. Sub-ADC input signal held only for short time (<(T/2=1/2Fs))
Possible implementation

- Full speed operation => bottom plate sampling scheme not feasible
- Charge injection, tracking distortion in the switch
- Additionally in the source follower driving the Sub-ADC’s …

Ref: C-C Hsu, ISSCC 2007
Source follower buffer for Sub-ADC’s

- \( C_L \propto N/2 \) sub-ADC caps, power/non-linearity increases as \( N \) increases for a given Sub-ADC speed to achieve high \( F_s \).

- If \( \omega C_L \gg (g_{mb} + g_{ds}) \), \( Z_{in} = 1/sC_{gs} + 1/sC_L - g_m/\omega^2 C_{gs} C_L \)

- As \( C_L \) increases, negative impedance becomes worse in value, that too at lower frequencies.
  
  - Transfer function ripple in the ADC increases.
  
  - Further restricts value of \( N \), and therefore \( F_s \)
Applications for conventional architecture 1

• Based on
  a) no accuracy loss due to phase/bandwidth mismatch
  b) Restriction on value of N for a given speed, accuracy and choice of architecture of sub-ADC,

• Optimally applied for
  – Relatively lower speed time-interleaving (<1GS/s), medium to high accuracy (~7-9 ENOB)
Conventional architecture 2

Advantages:
1. Scalable, high speed operation.
2. No need for Fs rate clock, fully sub-sampled

Disadvantage:
Complex DSP for phase & bandwidth mismatch
-residual errors degrade SNR, worse at high N and high Fin
Possible implementation

• Source follower/sub-channel performance independent of N.
• Phase/bandwidth mismatch increases severely as N increases, limits accuracy.
Applications for conventional architecture 2

- Based on
  a) Value of N not restricted for realizing BW/high accuracy in the sub-channel circuits
  b) Phase/bandwidth mismatch of channels limiting accuracy of the time-interleaved output, worst at high N.

- Optimally applied for
  - Relatively higher sampling speeds (~1GS/s<Fs<~20GS/s), low to medium accuracy (~<7 ENOB)
Proposed architecture (ISSCC 2006) for broader applications.
Need for newer architecture

• Need to
  – Cover the landscape of high speed (≥1GS/s) time-interleaved ADC’s with a considerable higher accuracy.
  – AND/OR
  – Possibly realize at lower speeds (<1GS/s)
    • for the same power higher accuracy (>9 ENOB)
    • OR for the same accuracy lower power
  Compared to conventional architecture 1.

• Based on adopting the advantages of each of the conventional architectures mentioned before, and mitigating the disadvantages.
  – Ref: S. Gupta. Et. al., ISSCC 2006
  – The target application here was 1GS/s, ~9ENOB at very low power, in relatively older CMOS 0.13um technology.
Architecture development: Step 1

- $p^i$ duty cycle < 1/N
- **1 sub-sampler loads the S/H switch at any time.**
- BW, performance independent of N, scalable to high speed.
- $p^i$ turnoff when Fs is off
  - Phase skews do not contribute to loss of SNR.
- Sub-ADC input held longer.
Desirables for performance/power

- Sample and hold instead of a track and hold

\[ T_1 + T_2 = T_{\text{sub}} = \frac{N}{F_s}, \quad T_1 < \left( \frac{1}{F_s} \right) \]

- Use double sampling, for maximal power utilization.
- Buffer faces full swing -- replace with a virtual ground amplifier
Architecture development: Step 2

- Adapt structure in step 1 to bottom plate sampling
  -- Can achieve all three desirables

Clocking scheme:

a) p1e turns off during the off period of Fs clock.

b) p1_s is the 1/N duty cycle clock.
Final Time-interleaved Architecture

Switch-C load

$p_{1_s}^{<j>}$ $p_{2e}^{<j>}$

$p_{2}^{<j>}$ $p_{1e}^{<j>}$

$p_{2_s}^{<j>}$ $p_{1e}^{<j>}$

$p_{1}^{<j>}$ $p_{2e}^{<j>}$

$j^{th}$ stage out of $N/2$
double-sampled stages

To other $N/2-1$ sub-sampled stages

11 bits
Clocks for the Final Architecture

Example clocks for N=4.
In this design N=8
ADC linearity

- Dominated by the first switch’s track mode and charge injection distortion.
  - First switch bootstrapped
    - maintain constant $V_{GS}$.
  - First switch driven by a source follower

![Diagram showing ADC linearity with bootstrap circuit to N/2 double-sampled, sub-sampled stages]
Sub-ADC architecture

- 11 bit, 250MS/s output rate. Double sampled
- Pipelined ADC architecture a logical choice.

```
4bit stage, 8X gain
4bit Flash
4

4bit stage, 8X gain
4bit Flash
4

5bit Flash

correction logic

output buffers

11b output data
```
Measured results for the proposed architecture
FFT with & w/o Gain/Offset errors

<table>
<thead>
<tr>
<th></th>
<th>SNDR</th>
<th>SFDR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Without gain or offset correction</td>
<td>40.9 dB</td>
<td>42.9 dB</td>
</tr>
<tr>
<td>With gain and offset correction</td>
<td>54.9 dB</td>
<td>58.5 dB</td>
</tr>
</tbody>
</table>
FFT for 2-tones at high frequency

$\text{Fin} = 470 \text{ & } 471\text{MHz, SFDR(Signal/IM3)} = 53.1\text{dB}$
SNDR and SNR vs. frequency

SNR and SNDR (dB) vs. Input frequency (MHz)

- SNDR
- SNR
## ADC performance summary

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sample rate</td>
<td>1 GS/s</td>
</tr>
<tr>
<td>Effective Resolution BW</td>
<td>500 MHz</td>
</tr>
<tr>
<td>Resolution</td>
<td>11 bits</td>
</tr>
<tr>
<td>SNR at 5 MHz</td>
<td>58.6 dB</td>
</tr>
<tr>
<td>SNR at 400 MHz</td>
<td>57.6 dB</td>
</tr>
<tr>
<td>Peak SNDR</td>
<td>55 dB</td>
</tr>
<tr>
<td>2-tone IM3 @ 470 MHz</td>
<td>53 dB</td>
</tr>
<tr>
<td>SFDR @ 5 MHz</td>
<td>58.5 dB</td>
</tr>
<tr>
<td>Power consumption</td>
<td>250 mW</td>
</tr>
<tr>
<td>ADC core area</td>
<td>3.5 mm²</td>
</tr>
<tr>
<td>Technology</td>
<td>0.13 μm digital CMOS</td>
</tr>
<tr>
<td>FOM (Power/2^{ENOB}<em>2</em>ERBW)</td>
<td>0.5pJ/conversion step</td>
</tr>
</tbody>
</table>
Talk Summary

- Applications landscape of time-interleaved ADC’s studied
  - Conventional architecture 1 usable for lower speed, higher accuracy
  - Conventional architecture 2 more optimal for higher speed, lower accuracy.
  - Proposed architecture (ISSCC 2006) covered a broader landscape of ADC’s providing at
    - Higher speeds: higher accuracy,
    - Lower speeds:
      - same accuracy at low power
      - higher accuracy at similar power