A Very Low Power CMOS Mixed-Signal IC for Implantable Pacemaker Applications

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Questions:

(1) What year was the 1st pacemaker introduced?

(2) How many transistors are there in the 1st pacemaker?

(3) How many transistors are there in today’s (2004) pacemaker?
Outline

- Overview of Cardiac Pacemaker
- Overview – Sensing
- Overview – Output Therapy System
- Overview – Battery Management System
- Overview – Low Power Logic Design
- Overview – Low Power Memory Design
- Overview (MEMS) – Activity Sensor
- Overview (MEMS) – Magnet Sensor
- Silicon Results
Overview of Cardiac Pacemaker – What is it?
Cardiac Pacemaker System

Pulse Generator

Pacing Leads

Left Atrium

Left Ventricle

Right Atrium

Right Ventricle

Picture of an actual Implantable Pacemaker

2 inch
Die Photograph

Power ~ 8uW

7000μm
Overview of Cardiac Pacemaker – Cardiac Sensing System
Sensing System Block Diagram

Cardiac Inputs ($\mu$V-mV)

Passive Filter Network

MUX

Passive Filter Network

MUX

Passive Filter Network

MUX

Low-Power Switched-Capacitor Filters/Amplifiers

Out # 1

ADC

Out # N

ADC
Low Power SC Circuits - Problem

Illustrated by a SC SH amplifier:
- Residual leakage current (~pA) when CMOS switch is off
- Cardiac/Neuro-signals have low frequency content ~0.1Hz
- Signal amplitude of interest ~μV-mV

If leakage=1pA, Chold=1pF, hold time=100mS, then Vout drift = 100mV (Unacceptable)
Leakage Cancellation Technique - Concept

The concept of "Leakage Cancellation Technique"

Self-adjusted current source

$I_{cancel} = I_1 + I_2 + I_3$

$V_{out}$

The concept of "Leakage Cancellation Technique"
Introducing the “Replica SH Circuit”, with $C_{rep} \ll C_{hold}$
Leakage Cancellation Technique - Design

A design example of the “Leakage Cancellation Technique”

\[
\frac{dV_{\text{hold}}}{dt} = \frac{I_{\text{delta}}}{\text{Chold} - \text{Crep}} = f\left(\frac{A_{\text{out}}}{A} + V_{\text{offset}}\right)
\]
Leakage Cancellation Technique - Results

SHA (Original)
1Hz sine input, Fs=10Hz
I leakage ~ 0.1pA total

SHA with Leakage Cancellation
1Hz sine input, Fs=10Hz
I leakage < 0.01pA (effective)
Overview of Cardiac Pacemaker – ADC
8-bit ADC

- ADC is used to digitized the cardiac sensing outputs
- Successive Approximation Architecture
- Typical power consumed by:
  - S/H
  - DAC
  - Comparator
- To minimize power, this ADC:
  1. Uses capacitor-array for both DAC and SHA
  2. Use an integrated-opamp for both SHA and comparator
8-bit ADC – Architecture

Successive Approximation Controls and Registers

Clk_16K → Successive Approximation Controls and Registers

V_{in} → Capacitor array for S/H and DAC

V_{REF_1} → SHA & Comparator

V_{REF_0} → SHA Out

8b Output → Comp Out

Done

Integrated “S/H-comparator”
8-bit ADC – Timing

- Analog Input
- Clock
- SHA
- SAR
- Done
- Output[7:0]

Sample1

Data1
8-bit ADC – Measured Results

8-bit ADC INL

10Hz input sinewave (-6dB of full scale)
## 8-bit ADC – Measured Results

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>8-bits</td>
</tr>
<tr>
<td>Sampling Rate</td>
<td>1 KS/s</td>
</tr>
<tr>
<td>Input Voltage Range</td>
<td>500mVpp</td>
</tr>
<tr>
<td>INL</td>
<td>&lt; 1.5 LSB</td>
</tr>
<tr>
<td>DNL</td>
<td>&lt; 1.5 LSB</td>
</tr>
<tr>
<td>SFDR</td>
<td>&gt; 48 dB</td>
</tr>
<tr>
<td>Supply Current (On)</td>
<td>~ 150nA @ 2V</td>
</tr>
<tr>
<td>Supply Current (Standby)</td>
<td>~ 20nA</td>
</tr>
<tr>
<td>Gain error</td>
<td>&lt; ±10% FS</td>
</tr>
<tr>
<td>DC offset error</td>
<td>&lt; 3 LSB</td>
</tr>
</tbody>
</table>
Complete Sensing System – Measurement Setup
Complete Sensing System (SC Filters and ADC) – Example ECG Results

An example ADC output of Electrocardiogram (ECG) processed by different SC filters.
Overview of Cardiac Pacemaker – Output Therapy System
High Voltage Output System

• To stimulate the heart muscle (e.g. initiate a heart beat), a high-voltage output pulse is delivered to the heart through the pacing leads.
• Multiplying the battery voltage is needed to generate the necessary high voltage.
  ➢ A Voltage Multiplier Circuit is used
• The amplitude and pulse width of the high-voltage output pulse is customized for the patients.
  ➢ A High Voltage DAC is used
High Voltage Multiplier

Voltage on chip (Not to scale)

Battery (Vdd ~ 2.8V)

Voltage regulator

Vreg

Voltage Multiplier

2*Vdd

3*Vdd

Hi-volt output pulse

On-chip analog & digital

Battery management & references

Usage

Voltage Multipliers and Regulators for the complete IC
Capacitive Voltage Multiplier – Design

Capacitive 2X and 3X voltage multiplier

$V_{dd}$, $V_{ss}$

$\phi_1, \phi_2$: Non-overlapping clocks

$C_{res2} = 2*V_{dd}$

$C_{res3} = 3*V_{dd}$
High-Voltage DAC – Design

Hi-Voltage Output Pulse Generator: Equivalent model

Hi-Voltage Output Pulse Generator: Switched-Cap DAC

Power Supply = 2* or 3* Vdd

Hi-Volt DAC

Pulse Amplitude

Vref

Vss

\( \phi_{pre} \)

\( \phi_{out} \)

\( C_1 \)

\( C_2 \)

Output Pulse

\( V_{out} \)
High-Voltage DAC – Design

High-Voltage DAC utilizing 2-in-1 opamp

2-in-1 (HV/LV) CMOS opamp
High-Voltage DAC – Measured Results

Output Pulse Vs input code

Linearity of Output Pulse Amplitude
Overview of Cardiac Pacemaker – Battery Management System
Battery Management System

- A primary battery (~2.8V) is typically used for a 5-10 years of device life time.
- Battery status must be accurately monitored to guarantee reliable operations.
- The status of the battery is determined by measuring its output voltage. However, it may NOT be very accurate due to the flat output voltage characteristics.
- **To enhance accuracy:**
  - A Battery Charge monitoring circuit (Battery Charge Meter) is proposed.
Battery Management System Block Diagram

Battery Charge Meter:
- Low offset, high linearity VCO
- Continuously monitors 0.5µA-100µA of current
- Very low power consumption
Battery Management System – Battery Charge Meter

- VCO output frequency:

\[ Freq_{VCO} = K_{VCO} \times I(t) \times R \]

- The output of the counter:

\[ Count = \int Freq_{VCO} \cdot dt = \int K_{VCO} \times I(t) \times R \cdot dt \]

- Re-arrange to give:

\[ Q = \text{Charge} = \int I(t) \cdot dt = \frac{Count}{K_{VCO} \times R} \]

- Knowing “Count, \( K_{VCO} \) and \( R \)”, the total charge depleted from the battery can be accurately calculated.
Battery Charge Meter - Design

Battery Charge Meter – VCO block diagram

Low Offset VCO:
Battery Charge Meter – VCO Design

Low-Power Auto-Zero Switched-Cap Integrator

Comparator

Vin_p, Vin_n

\( f_1, f_2: \) Non-overlapping clocks

\[ V_{\text{ramp}}(\text{per step}) = \frac{(V_{\text{in}_p} - V_{\text{in}_n}) \times C_s}{C_{\text{int}}} \]

\[ f_{\text{vco}} = \frac{(V_{\text{in}_p} - V_{\text{in}_n}) \times F_s \times C_s}{2(V_{\text{ref}_p} - V_{\text{ref}_n}) \times C_{\text{int}}} \]
Battery Charge Meter – Measured Results

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Range</td>
<td>0mV - 50mV</td>
</tr>
<tr>
<td>VCO Gain</td>
<td>80 Hz/V</td>
</tr>
<tr>
<td>Input Offset Error</td>
<td>&lt; 150µV</td>
</tr>
<tr>
<td>Sampling Rate</td>
<td>8 KHz</td>
</tr>
<tr>
<td>Supply Current (On)</td>
<td>~ 100nA @ 2.8V</td>
</tr>
<tr>
<td>Supply Current (Standby)</td>
<td>&lt; 10nA</td>
</tr>
</tbody>
</table>

Battery Charge Meter - VCO Linearity

Output Frequency (Counts per 60 sec) vs Differential Input Voltage (V)
Now, we have:

- \(K_{\text{vco}} = 80\text{Hz/V}, \ R = 500\Omega\) and assume a 1A-h battery

\[
Q = \text{Charge} = \int I(t) \cdot dt = \frac{\text{Count}}{K_{\text{vco}} \times R}
\]

- At the end of battery life, the counter output will reach: 144,000,000 counts
  (It is also independent of the battery output voltage!)
Overview of Cardiac Pacemaker – Low Power Logic Design

by:

Raymond Okamoto

Raymond Okamoto received his B.S. ECE from U.C. Santa Barbara. He has 15+ years in both hardware and software designs. He has previous worked for ArgoSystems, Trimble Navigation, Intel and Mentor Graphics. He has designed both GPS and networking ASICs as well as other hardware systems. He joined St Jude Medical in 2003.
Programmable Logic, Timing Control and Therapy Algorithms

- CPU Configuration Registers
- Timing and control for Analog Functions
- Finite State Machine under CPU control for Therapy Algorithms
- Hardware Control Finite State Machine in backup (fail safe) mode to delivery therapy
- RTL to GDSII design flow
- Low Power Design (nW)
Digital Core Lower Power Techniques

- Minimize Voltage
  - Trade off custom low power library vs standard library
  - Backend Flow with multiple power
- Minimize Clock Frequency
  - Gated Clock Design
  - Review of minimum clock frequency required
- Minimize Capacitance (Logic Area)
  - Design for minimum logic at the RTL level
  - Reduce clock domains (trade off with min clock frequency)
- Customize Clock Synthesis Tool for low power vs high speed trees
Clock Tree Synthesis
Custom Approach to minimize buffer insertion

Hand Placed Initial Clock Buffer

Minimize Buffer Insertion to balance system clock to 8 Clock Domains

Added hand placed buffers
Around clock divider Flip Flops to minimize Clk to Q Delay
(reduce buffers for clock balancing)

5 : 1 Aspect Ratio for Digital Core
Overview of Cardiac Pacemaker – Low Power Memory Design

by:

Joseph Ahn

Joe Ahn received his B.S. and M.S. EE from Lehigh University. He has 11+ years in hardware design. He has previous worked for Virtual Silicon Technology, C-Cube Microsytems and Aspec Technology. He has designed various components including SRAM’s, ROM’s, datapath blocks, I/O’s and standard cells. He joined St Jude Medical in 2002.
Ultra-Low Power SRAM for Pacemakers and ICD’s

• The three components of power
  - Capacitance
    – Reduce switching of high capacitive nodes
  - Voltage
    – Reduce the voltage swing
  - Frequency
    – Lower operating frequency
Reduce switching of high capacitive nodes

- Smaller subsections
- Shorter word-lines and bit-lines
- Disable inactive circuitry
- Local decoders vs. global decoders
Reduce the voltage swing

- Partial voltage swings
- Low power sense amp
- Special manufacturing processes
  - Lower operating voltage
  - Leakage current
  - High Vt devices
Lower operating frequency

• Lower operating frequency
Overview of Cardiac Pacemaker – MEMS Activity Sensor
Patient Activity Sensor

- Patient activity sensor is used to:
  - Sense patient’s body movements, and to determine the appropriate pacing rates for correct therapy.
  - An “Accelerometer Sensor” is placed inside the device.
  - Be able to differentiate between patient movements from surrounding noise (e.g., vehicle vibration, vacuum cleaner)
Activity Sensor Interface Circuit

- It generates a charge/voltage proportional to the patient’s acceleration.
- The VCO generates an output signal whose frequency is proportional to the voltage sensed at the input. The number of cycles of the VCO output is proportional to the average patient physical accelerations.
- Low power consumption ~ 40nA
Overview of Cardiac Pacemaker – MEMS Magnet Sensor
Magnet Detection Sensor

• A magnet detector can be used to:
  – Open the telemetry channel
  – Disable the device
  – Put the device into a special operating mode, e.g. in emergency
Magnet Detection Sensor

Two types of magnetic sensors are typically used:

1. Reed Switch
2. Giant Magneto Resistive (GMR) Sensor
Reed Switch Interface Circuit

- Low pass filter
- Debouncing circuit to filter out glitches
- Very low power consumption ~ 20nA
Overview of Cardiac Pacemaker – Silicon Results
# Silicon Results

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>2.0V – 2.8V</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>~ 8µW</td>
</tr>
<tr>
<td>Die Size</td>
<td>7mm x 7mm</td>
</tr>
</tbody>
</table>