CMOS RF Power Amplifiers: Nonlinear, Linear, Linearized

David Su

Atheros Communications
Sunnyvale, California
Outline

• Introduction
• Nonlinear Power Amplification
• Linear Power Amplification
• Linearization using Envelope Elimination and Restoration
• Conclusion
RF Power Amplification

- **Purpose:** Delivers “narrow-band” RF power to a 50-ohm antenna
- **Performance:** Output Power, Efficiency, Linearity
## Traditional PA Classification

<table>
<thead>
<tr>
<th>Class</th>
<th>Modes</th>
<th>Conduction Angle</th>
<th>Output Power</th>
<th>Maximum Efficiency</th>
<th>Gain</th>
<th>Linearity</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Current Source</td>
<td>100%</td>
<td>moderate</td>
<td>50%</td>
<td>Large</td>
<td>Good</td>
</tr>
<tr>
<td>B</td>
<td>Current Source</td>
<td>50%</td>
<td>moderate</td>
<td>78.5%</td>
<td>Moderate</td>
<td>Moderate</td>
</tr>
<tr>
<td>C</td>
<td>Current Source</td>
<td>&lt; 50%</td>
<td>small</td>
<td>100%</td>
<td>Small</td>
<td>Poor</td>
</tr>
<tr>
<td>D</td>
<td>Switch</td>
<td>50%</td>
<td>large</td>
<td>100%</td>
<td>Small</td>
<td>Poor</td>
</tr>
<tr>
<td>E</td>
<td>Switch</td>
<td>50%</td>
<td>large</td>
<td>100%</td>
<td>Small</td>
<td>Poor</td>
</tr>
<tr>
<td>F</td>
<td>Switch</td>
<td>50%</td>
<td>large</td>
<td>100%</td>
<td>Small</td>
<td>Poor</td>
</tr>
</tbody>
</table>
PA Classification & Input Drive

- Class C
- Class AB
- Class A
- Class D, E, F

- Conduction Angle (V_{DC})
- Input Signal Overdrive (V_{in})

Switch

Current Source
Power Amplifier Classification

- **Class A**: Saturated
- **Class B**: Conduction Angle \((V_{DC})\)
- **Class C**: Input Signal Overdrive \((V_{in})\)
- **Class AB**: Current Source
- **Class D, E, F**: Switching

The diagram illustrates the classification of power amplifiers based on the conduction angle and input signal overdrive.
CMOS for RF Power Amplification

• Traditional RF PAs use GaAs / Bipolar.

• Advantages of CMOS:
  Low cost, high-yield, high-integration
  Efficient switched-mode amplifier

• Disadvantages of CMOS:
  Low bandwidth
  Low breakdown voltage
Simplified RF Output Stage

\[ I_D = g_m V_{in} \]

\[ I_L \leq \frac{V_{DD}}{R_L} \]
Class-A (Linear) Operation

\[ P_{out} = \frac{1}{2} I_L^2 R_L \leq \frac{V_{DD}^2}{2R_L} \]

For \( P_{out} = 1 \text{ W (Class A)} \), \( R_L = 4.5 \, \Omega \) @ \( V_{DD} = 3 \text{ V} \)
\( R_L = 3.1 \, \Omega \) @ \( V_{DD} = 2.5 \text{ V} \)

⇒ Needs Impedance Transformation Network → 50 \( \, \Omega \) antenna
⇒ Keep parasitic loss \( << \) \( R_L \) of 3.1 \( \, \Omega \)
Efficiency of Class A operation

\[ P_{\text{out}} \leq \frac{V_{DD}^2}{2R_L} \]

\[ P_{\text{supply}} = I_{DC} \times V_{DD} = \frac{V_{DD}^2}{R_L} \]

Efficiency = \( \frac{P_{\text{out}}}{P_{\text{supply}}} \leq 50\% \)

\[ P_D = I_D \times V_D \quad \Rightarrow \quad \text{Efficiency} \]
Efficiency-Linearity Tradeoff

- Large input signal
- Square wave output $I_D$ and $V_D$
- Non-overlapping $I_D$ and $V_D$

\[ P_{\text{out}} = \frac{V_{DD}^2}{R_L} \]

\[ P_D = 0 \Rightarrow \text{Efficiency} = 100\% \]
Low-Voltage Operation

\[ P_{out} \approx \frac{VDD^2}{nR_{load}} \]

\[ R_{load} \approx \frac{VDD^2}{nP_{out}} \]

Switched-Mode: \( n = 1 \)
Class A,B: \( n = 2 \)
Class C: \( n > 2 \)
LOAD PULL Optimization
1. Impedance transformation: Output Power
2. Harmonic Tuning: short @ 2fc & open@ 3fc for non-overlap I_D & V_D to maximize efficiency
3. Input drive: V_DC -> Conduction Angle; Vin -> current source vs switch
Nonlinear Power Amplifier

- Hewlett Packard Labs (with W. McFarland)
- 800-MHz 32dBm AMPS PA with 42% PAE in 0.8 µm CMOS
Choose \( n = 1.5 \) (assume 67% efficiency due to \( \text{Ron} > 0 \)),
VDD = 2.5V,
For Pout = 1 W,
\[
\text{Ron} = 1 \, \Omega
\]
\[
\text{I}_{\text{DC}} = 0.49A
\]
\[
\text{R}_{\text{load}} = 4.2 \, \Omega
\]
\[\text{Pout} \approx \frac{\text{VDD}^2}{n\text{R}_{\text{load}}}\]
⇒ Output transistor sizing: \( \text{Ron} < 1 \, \Omega \)
Output Stage Design

VDD = 2.5V

Z_{load}

IN 5dBm

A = 25dB

2.5Vₚ

ID

VD

OUT

50Ω

3.8nH 3.8pF

7.6pF

25pF

|Z_{load}|

ID

VD

Impedance (ohm)

Q~5

10^7 10^8 10^9 10^10 10^11
Complete Amplifier

**Diagram:**
- **CMOS IC bond wires**
- **RF choke**
- **Bond wires**
- **Freq. 824 – 849 MHz**
- **VDD 2.5V**
- **Pout 30 dBm**

**Specifications:**
- **Freq:** 824 – 849 MHz
- **VDD:** 2.5V
- **Pout:** 30 dBm
Die Photo

0.8 µm CMOS

1.5 mm²
Measured $P_{OUT}$ and Efficiency

![Graph showing the relationship between output power (dBm) and power supply voltage (Volts), with a noted efficiency of ~68%]

Drain Efficiency ~ 68%
Linear Power Amplifier

- Atheros Communications (with D. Weber et al)
- 5-GHz 18dBm OFDM PA for IEEE 802.11a in 0.25 µm CMOS
Spectral-Efficient Modulation

- 64-QAM (Quadrature Amplitude Modulation)
  - Large signal to noise ratio $> 30$dB

- OFDM (Orthogonal Frequency Division Mux)
  - Large peak to average power ratio of $\sqrt{52}$ or 17dB

→ Requires High Linearity in PA
Power Amplifier Design

- Large peak to average ratio (PAR) of $\sqrt{52}$ or 17dB
- Signal peaks are infrequent: 0.25dB SNR degradation when PAR reduced to 6dB for 16-QAM*.

- Implications:
  - Poor power efficiency
  - With 6dB PAR, to obtain 40mW (16dBm) requires Psat of $\sim 22$dBm or 160mW
  - With 17dB PAR, to obtain 40mW (16dBm) requires Psat of $\sim 33$dBm or 2W

*Van Nee & Prasad, OFDM for Wireless Multimedia Communications, Artech House, 2000
Linear PA makes efficient radios

- Frequency bandwidth is precious
  -- Maximize network capacity
- Energy/bit (battery life)
  More bits sent per second
  -- PA + the rest of the radio
  are ON for shorter duration
Linear PA Design

- Input load impedance
  - signal dependency
  - cascode
- $V_{GS}$ overdrive
  - dc bias with capacitive level-shift
- Output load impedance
  - impedance matching network
- Stability
  - cascode
Power Amplifier Topology

- Class A operation
- Cascoded
  - 3.3V supply voltage
  - Stability
- Capacitive Level-shift
  - Metal-2,3,4,5 stacks
- Inductive loads
- Differential
  - Off-chip balun

V_{pa} = 3.3V

L2\* C2 L3
M2 M3
L4\* Bias

Output

* C.P. Yue and S.S. Wong, IEEE JSSC, May 1998
Power Amplifier Schematic

Vin+
L1p
C1p
Vout+
Bias
L3p
M2p
L4p
Bias
M3p
Vin-

Vin-
L1n
L2n
Vout-
Bias
L3n
M2n
L4n
Bias
M3n

P_{SAT} = 22 \text{ dBm}
Die Photograph
Measured BPSK OFDM Spectrum

$P_{\text{OFDM}} = 17.8 \text{ dBm}$
Measured Transmit Output Power

OFDM Output Power (dBm)

Data Rate (Mbps)
Linearized Power Amplification

- Hewlett Packard Labs (with W. McFarland)
- Linearization IC for NADC with efficiency improvement from 36% to 49% using envelope elimination and restoration
Applying Integration to RF PA

Transistors are *cheap*.

- LARGE Output Power: Use switched-mode output stage
- HIGH Efficiency: Use switched-mode output stage
- GOOD Linearity: Use linearization circuits so that the output stage does not need to be linear.

**SOLUTION:** Switched-mode output stage + linearization.
Envelope Elimination and Restoration

Ref: L. Kahn, Proc IRE, July 1952
Closed-Loop EER Implementation

RF Input

Envelope Detector

Envelope Detector

Limiter

Phase

Buffer

RF Power Amplifier

△-Mod Class-D Switching Power Supply

Magnitude

Atten.

RF Output
$\Delta$-Modulated Switching Power Supply

- Closed-loop system
- Modulation to generate a two-level output
  \[ \Rightarrow \text{Pulse width modulation vs. Delta modulation} \]
- Efficient Class-D driver
Switched-cap Circuit for $\Delta$ Modulation

Subtraction & Compensation

Comparator

Output Buffer

Lowpass Filter

Off-Chip
Die Photograph

- Envelope Detector (0.03 mm²)
- Limiter (0.34 mm²)
- Δ-Mod Switching Power Supply (2 mm²)
- Buffer (1.9 mm²)
Switching Power Supply

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>3.0V</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>0.1 to 2.65V</td>
</tr>
<tr>
<td>Output Current</td>
<td>0.75 A</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>100 kHz</td>
</tr>
<tr>
<td>Harmonic Distortion</td>
<td>–55 dBC</td>
</tr>
<tr>
<td>Efficiency</td>
<td>80%</td>
</tr>
<tr>
<td>Die Area</td>
<td>3.9 sq mm</td>
</tr>
</tbody>
</table>

![Output Spectrum Graph]

Frequency (in kHz)

Output Spectrum (in dB)
Spectral Mask of CMOS PA

Amplitude (10 dB/div)

Frequency (15kHz/div)

RBW: 300 Hz
VBW: 100 Hz

Saturated Output

Linearized Output

ACP1  -30dBc
ACP2  -48dBc
π/4 QPSK Constellation of CMOS PA

Without Linearization

With Linearization

Mag Err = 2.2% rms
Phase Err = 1.5° rms
Efficiency of 4.8-V GaAs PA

Peak Linear Power: 26.5dBm → 29.5dBm
Peak Linear PAE: 36% → 49%

- Output Power (dBm)
- Power-added Efficiency (%)
Conclusion

• Nonlinear (switched-mode) PA provides
  (+) large output power and high efficiency
  (−) poor linearity

• Linear PA provides
  (+) linearity, spectral efficiency
  (−) poor efficiency

• Linearization using envelope elimination and restoration
  (+) linear RF output + high efficiency
  (−) implementation complexity