An 802.11a/b/g SoC for Embedded WLAN Applications

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Outline

- Introduction
  - Embedded WLAN applications
- SoC block diagram
- Power management
- Transceiver architecture
  - 5GHz/2.4GHz transmitter
  - 5GHz/2.4GHz receiver including ADC
  - Frequency synthesizer
- Measurement results
Embedded WLAN

- **Applications:** Wi-Fi phones, digital cameras, networked gaming, PDAs, MP3 players, etc.
  - Long battery life → low sleep/standby power
  - Small form-factor → single chip integration

- **Support for wide range of crystal frequencies**
  - Share crystal oscillator with host system

- **Support for common I/O interfaces**
  - SDIO, SPI, CF, etc.

- **Dual-band operation at 2.4GHz and 5GHz**
SoC Block Diagram

19.2, 24, 26, 38.4, 40 or 52 MHz crystal or external reference
Low frequency 32kHz crystal

SoC

RF Transceiver

Data Converters

Digital PHY & MAC

I/O Interface

Host System

Power Management

BB PLL

CPU

RX/TX & Diversity Switches

Ant1

Ant2

5G

2.4G

5G

2.4G
Power Management

- Operating modes: Sleep, Standby, RX, TX

- Programmable LDO regulators used to lower the supply voltage in sleep mode
  - All register states maintained.
  - Reduced supply leakage current

- Standby power depends on RX duty cycle
  - Reduce power by staggering the power-on of analog blocks based on settling time.
  - Gate clock signals to inactive digital circuits
  - Run off of the 32kHz clock when idle
Sliding-IF Architecture

- Only one synthesizer needed to generate LO frequencies
- \( f_{VCO} = \frac{2}{3} f_{RF5}, \frac{4}{3} f_{RF2} \rightarrow \text{No LO Pulling} \)

5GHz Band: 4.9 - 5.925 GHz
2.4GHz Band: 2.412 - 2.484 GHz
Dual-Band Transmitter

- **5G**
  - RF Gain Ctrl
  - PA
  - RFVGA1 & 2

  \[ \text{LO}_{RF5} = \frac{2}{3} f_{RF5} \]

- **2.4G**
  - RF/IF Gain Ctrl
  - PA
  - RFVGA
  - IFVGA

  \[ \text{LO}_{RF2} = \frac{2}{3} f_{RF2} \]

- **DAC**

- **3rd-Order LPF**

- **BB Gain Ctrl**

- **160/176 MS/s**

- **I**

- **Q**
Transmit Power Control

- 5b DAC to correct power detector DC offset
- TX gain adjusted on a per packet basis
Dual-Band Receiver

LO_{RF5} = \frac{2}{3} f_{RF5}

LO_{RF2} = \frac{2}{3} f_{RF2}

5GHz: NF = 5.5dB
2.4GHz: NF = 5.0dB

5G
LNA
RFVGA
RF Gain Ctrl

2.4G
LNA
RFVGA
RF Gain Ctrl

I Offset Correction
Q Offset Correction

40/44 MS/s
Dual Input ADC

I
Q

I
Q

DAC

DAC

I

Q

LNA
RFVGA
Dual-Input A/D Converter

- Time-multiplexed pipeline architecture
  ⇒ I & Q inputs are sampled simultaneously
  ⇒ Pipeline stages run at 80/88 MHz (2×\(f_S\))

- Almost half the area and similar power as 2 non-multiplexed ADC’s
  ⇒ Area: 0.45mm x 1.0mm, Power: 48mW
ADC Sample/Hold Circuit

\[ f_s = \frac{1}{f_s}, \quad f_s = 40 / 44 \text{ MS/s} \]

- \( I_p, I_n, Q_p, Q_n \)
- \( C_1, C_2, C_3, C_4 \)
- \( \phi_{S}, \phi_{H,I}, \phi_{H,Q} \)
- \( \text{Sample Hold I Hold Q Wait} \)
- \( \text{out}_n, \text{out}_p \)
Fractional-N Synthesizer

Xtal Osc

Ref. Div.

19.2 - 52 MHz

PFD

Regulator

3\textsuperscript{rd} Order Loop Filter

Z(s)

R,C cntrl

Regulator

VCO

V_c

8 coarse tuning

I_{CP} cntrl

I_{CP}

f_{VCO}

\frac{f_{VCO}}{8P+S+N_{\Sigma-\Delta}}

f_{REF}

\text{P \& S counters}

3

\sum-\Delta Modulator

\frac{P \& S counters}{\div 8/9 Prescaler}

3.2 - 4 GHz

To LO Buffers and Dividers

Frequency Divider
CMOS LC-tank VCO

- Tuning range: 3.2 - 4 GHz
  ⇒ 8-bit switch-capacitor bank for coarse tuning
  ⇒ diode varactor for continuous fine tuning

- Voltage-to-freq. gain:
  \[ K_{VCO} = 2\pi^2 L \cdot f_{VCO}^3 \cdot \frac{\partial C}{\partial V_C} \]

- Large variation in \( K_{VCO} \):
  \( K_{VCO} = 34\text{MHz/V @3.2GHz} \)
  \( K_{VCO} = 66\text{MHz/V @4GHz} \)
Synthesizer Design

- Loop Gain = \[
\frac{I_{CP} \cdot Z(s) \cdot K_{VCO}}{s \cdot N_{div}}
\]
where \( N_{div} = \frac{f_{VCO}}{f_{REF}} \)

\[\Rightarrow\] \( I_{CP} \) is digitally varied as \( 1/f_{VCO}^2 \) for constant loop gain over tuning range.

- On-chip programmable loop filter, \( Z(s) \)
  \[\Rightarrow\] Program for 50° PM with given \( f_{REF} \)
  \[\Rightarrow\] Optimize loop BW for low integrated PN
  \[\Rightarrow\] For stability, 3rd pole of \( Z(s) \) \( \gg \) loop BW.
LO Buffer with AGC

- Inductively-tuned
- \(3.2\text{GHz} < \text{LO}_{RF5} < 4\text{GHz}\)
- Desire an LO amplitude \(\approx 1V\_\text{diff}\)
- Use AGC to minimize bias current
  \(\Rightarrow 3.5\text{mA} < I\_\text{tail} < 12\text{mA}\)
  over P.V.T. & freq.
5GHz TX Phase Noise

Center Frequency: 5.32GHz

-93dBc/Hz

-110dBc/Hz
**Σ-Δ Modulator Noise Contribution**

Center Frequency: \( \approx 5.2 \text{GHz} \)

- With \( \Sigma-\Delta \) Modulation
  - Phase Noise (dBC/Hz) decreases by 9 dB

- No Modulation

Frequency Offset (Hz)

Phase Noise (dBC/Hz)
Transmit EVM @ $P_{\text{out}} \approx -4\text{dBm}$

2.4GHz Band

- EVM (dBm): -24, -25, -26, -27, -28, -29, -30
- Channels: 2400, 2420, 2440, 2460, 2480
- EVM Spec.: 802.11g spec.
- Deviation: 2.7 dB

5GHz Band

- EVM (dBm): -24, -25, -26, -27, -28, -29, -30
- Channels: 5000, 5200, 5400, 5600, 5800, 6000
- EVM Spec.: 802.11a spec.
- Deviation: 2.2 dB
Receiver Sensitivity

2.4GHz Band

- Sensitivity (dBM) vs. Channel Frequency (MHz)
- 54 Mbps
- 6 Mbps
- 802.11g spec.
- 11dB

5GHz Band

- Sensitivity (dBM) vs. Channel Frequency (MHz)
- 54 Mbps
- 6 MHz
- 802.11a spec.
- 4dB
- 5dB
Die Photo

- Process: 0.18\textmu m CMOS with 3V I/O
- Die Size: 6.6 \times 6.7 \text{ mm}^2
- Analog Area: 13.5 \text{ mm}^2
- Packages: 216-pin BGA or CSP

Digital MAC & Baseband

ADC
BIAS
PLL
DAC
TX BB FILTER
2.4/5GHz TX RF
2.4/5GHz RX RF
RX BB FILTER
Synth
## Performance Summary

<table>
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<tr>
<th>Parameter</th>
<th>2.4GHz Band</th>
<th>5GHz Band</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Transmit EVM at 54Mbps</strong></td>
<td><a href="mailto:-27.5dB@-3.5dBm">-27.5dB@-3.5dBm</a></td>
<td>-28dB@-4dBm</td>
</tr>
<tr>
<td><strong>Receiver Sensitivity for 6Mbps</strong></td>
<td>-94dBm</td>
<td>-91dBm</td>
</tr>
<tr>
<td><strong>Receiver Sensitivity for 54Mbps</strong></td>
<td>-76dBm</td>
<td>-73dBm</td>
</tr>
<tr>
<td><strong>Receiver Noise Figure</strong></td>
<td>5.0dB</td>
<td>5.5dB</td>
</tr>
<tr>
<td><strong>SoC Power Dissipation</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RX mode</td>
<td>424mW</td>
<td>398mW</td>
</tr>
<tr>
<td>TX mode ($P_{\text{out}}=-4\text{dBm}$)</td>
<td>380mW</td>
<td>425mW</td>
</tr>
<tr>
<td><strong>RF Transceiver Power</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RX (excl. ADC)</td>
<td>287mW</td>
<td>267mW</td>
</tr>
<tr>
<td>TX ($P_{\text{out}}=-4\text{dBm}$, excl. DACs)</td>
<td>272mW</td>
<td>310mW</td>
</tr>
<tr>
<td><strong>Sleep Power Dissipation</strong></td>
<td>&lt; 300μW</td>
<td></td>
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<tr>
<td><strong>Technology</strong></td>
<td>Standard 0.18μm CMOS w/ 3V I/O</td>
<td></td>
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<tr>
<td><strong>Die Area (analog area)</strong></td>
<td>44.6 (13.5) sq. mm</td>
<td></td>
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Conclusions

- Demonstrated a single-chip IEEE 802.11a/b/g SoC suitable for embedded WLAN

- Receiver sensitivity of -76dBm and -73dBm at 54Mbps for 2.4GHz and 5GHz, respectively

- Fractional-N frequency synthesis allows operation with a range of crystal frequencies

- Power management features reduce sleep and standby current
Acknowledgements

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