26.8: A 1.9GHz Single-Chip CMOS PHS Cellphone

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Outline

- Introduction
- Overall Architecture
- RF Transceiver
  - Synthesizer
  - Receiver
  - Transmitter
- Calibration
- Measurement Results
Integrated PHS SoC Solution

■ Personal Handy-Phone System (PHS)
  • Commercially launched in 1995
  • Resurgence in China (> 50M subscribers in 2004)

■ Single-Chip PHS Solution in 0.18μm CMOS
  • RF/Analog: RF transceiver, audio/voiceband data converters and audio amplifiers
  • Digital: PHS MODEM, TDMA, CPU, Voice subsystem, Interfaces

■ PHS System
  • TDMA/TDD - Time Domain Multiple Access / Duplexing
  • $\pi/4$ QPSK modulation with 192kHz channel bandwidth
  • 1.9GHz frequency band, 300kHz channel spacing
  • Support seamless handover $\rightarrow$ fast channel switching
Advantages of System-on-Chip

- Low cost, small form factor with fewer external components
- Digital calibration
  - Wide digital-analog interface without package pins and associated power for I/Os
  - Digital calibration to repair analog impairments, eases requirements of analog RF circuits
Block Diagram of Single-Chip PHS Cellphone

- Power Mgmt
- PHS TDMA
- PHS MODEM
- PHS RF Transceiver
- Interfaces
- CPU
- Voice Subsystem
- Audio Amplifiers Data-Converters
- SRAM
- Flash
- LCD
- Display
- LED
- Keypad
- WLAN
- Microphone
- Earpiece
- Speaker
RF Transceiver Block Diagram

Transmitter
- XPA
- PA
- DAC
- LO

Receiver
- RF Loop back
- ADC
- LO

Channel Frequency
- 3.8GHz

Sigma Delta Fractional-N Synthesizer

\[ f_{vco} = 2 \times f_{rf} \]
- weaker PA pulling
- smaller inductor
- easy quad. LO gen
Sigma-Delta Fractional-N Synthesizer

38.4MHz crystal / TCXO

Total current = 25mA
Voltage Controlled Oscillator

Regulated $V_{DD}$ (1.8V)

7-bit control

$V_c$
Fast Synthesizer Settling (I)

- Seamless handover support → requires fast channel switching

Traditional approach: Use two interleaving synthesizers → power and area penalty

We use only one synthesizer with fast settling
Fast Synthesizer Settling (II)

- Tradeoff between settling time and phase noise: Loop bandwidth optimization
  - Wide loop BW for fast settling
  - Low loop BW to suppress $\Sigma\Delta$ quantization noise
  - Optimized loop BW = 120kHz

- Avoid over-design → Minimizing loop BW variation
  - $BW = (K_{vco} I_{cp} R_s) / (2\pi N)$
  - $V_{ctrl}$ within 200mV → $K_{vco}$ is roughly constant
  - $I_{cp}$ tracks process variation of $R_s$ → $I_{cp}R_s$ constant

- Loop BW dynamically adjusted during switching to speed up frequency transient response

- Resulting settling time = 15$\mu$s
Direct Conversion Receiver

Total current = 32mA
Receive Mixer and LO Buffers

Passive I/Q Mixer Using NMOS Native Devices

Common-Mode Feedback and Replica Bias

Two-Stage Inductorless LO Buffer
Direct Conversion Transmitter

Total current = 29mA

RF Loopback to RX
Segmented Power Amplifier

\[ V_{\text{in}}^+ \] \quad M1 \quad M2 \quad \ldots \quad M3 \quad M4
\[ V_{\text{in}}^- \] \quad b1 \quad \text{SW1} \quad \ldots \quad b4 \quad \text{SW4}

\[ V_{\text{dd}} \]

\[ V_{\text{out}}^+ \]

\[ V_{\text{out}}^- \]
Digital Calibration and RF Loopback

- Calibration of Analog Imperfections
  - Receiver filter bandwidth
  - Receiver DC offset
  - I/Q mismatch
  - Transmitter carrier leak
Receiver Sensitivity

Channel Frequency (MHz)

Sensitivity (dBm)

Receiver Noise Figure = 3.5dB

Sensitivity = -106dBm

PHS Sensitivity Standard

9dB
Adjacent Channel Selectivity (dBc)

Channel Frequency (MHz)

Receiver Adjacent Channel Selectivity (ACS)

ACS Spec = 50dBc

PHS modulated blocker at 600kHz offset

PHS Signal -94dBm

600kHz

PHS Blocker

600kHz
**Receiver 2-Tone Intermodulation**

Intermod Spec = 47dBc

2 equal sized single-tone blockers at 600kHz & 1.2MHz offset

PHS Signal -94dBm

Blockers

600kHz, 1200kHz

Channel Frequency (MHz)
Transmit Spectrum

PHS standard requires OBW < 288kHz

OBW = Occupied BW containing 99% signal power

Measured OBW < 250kHz for all channels

Center 1.907GHz
Res BW 10kHz

Span 2MHz

Ref
10dBm

Log
10dB/

-10dBm
Transmitter Modulation Accuracy

Frequency: 1 906.847 373 1 MHz
Frequency Error: -2.626 9 kHz
RMS Vector Error: 3.80%
Peak Vector Error: 7.82%
Output Power: 0dBm

Frequency: 1 906.847 366 4 MHz
Frequency Error: -2.633 6 kHz
RMS Vector Error: 1.03%
Peak Vector Error: 2.50%
Output Power: -10dBm

PHS Standard requires EVM less than 12.5%
Transmit Adjacent Channel Power (ACP)

![Diagram showing Transmit Adjacent Channel Power (ACP)]

- **Spec**: 600kHz ACP
- **8dB Margin**
- **900kHz ACP**
- **PHS signal 18.5dBm with xPA**
- **>8dB Margin**
- **600kHz**

Channel Frequency (MHz):
1895, 1898, 1901, 1904, 1907, 1910, 1913, 1916, 1919
Synthesizer Phase Noise at 1895.15MHz

Phase Noise @ 600kHz = -118dBc/Hz
Measured Synthesizer Settling Time

Settling Time to 1 kHz = 15 μs
Die Micrograph
## Performance Summary

<table>
<thead>
<tr>
<th>Power Dissipation</th>
<th></th>
<th></th>
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</thead>
<tbody>
<tr>
<td>RF Transmitter</td>
<td>29mA</td>
<td></td>
</tr>
<tr>
<td>RF Receiver</td>
<td>32mA</td>
<td></td>
</tr>
<tr>
<td>RF Synthesizer</td>
<td>25mA</td>
<td></td>
</tr>
<tr>
<td>Talk Mode (1/8 duty cycle Tx &amp; Rx)</td>
<td>81mA (including audio and digital)</td>
<td>1mA (including audio and digital)</td>
</tr>
<tr>
<td>Standby Mode</td>
<td>1mA</td>
<td>1mA</td>
</tr>
</tbody>
</table>

| Phase Noise @ 1.9GHz               | -118dBc/Hz @ 600kHz offset |
| Settling time to +/- 1kHz          | 15μs    |
| Receive Sensitivity                | -106dBm |
| Receiver Noise Figure              | 3.5dB   |
| Transmit Power (EVM compliant)     | +4 dBm  |
| Transmit EVM                       | 4% rms @ 1dBm |
|                                    | 1% rms @ -10dBm |
| Technology                         | Standard 0.18μm CMOS |
| Supply Voltage                     | 3.0V with internally regulated 1.8V |
| Die Size:                          | 33 mm² |
| RF and Analog                      | 12 mm² |
| Package                            | 276-pin BGA |
Conclusions

- Demonstrated single-chip PHS cellphone in 0.18 μm standard digital CMOS
- SoC performance meets or exceeds all PHS specifications
- System on a single chip allows for digital calibration to ease requirements of analog circuits
Acknowledgments

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