20.2: A Dual-band CMOS MIMO Radio SoC for IEEE 802.11n Wireless LAN

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Outline

- Introduction
- SoC architecture
- Circuit implementation
- Measurement results
- Conclusions
# 802.11n MIMO Wireless LAN

<table>
<thead>
<tr>
<th></th>
<th>Legacy 802.11(g/a)</th>
<th>802.11n (Draft)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Spectrum Available</td>
<td>83.5/555MHz</td>
<td>83.5/555MHz</td>
</tr>
<tr>
<td>Channel Bandwidth</td>
<td>20MHz</td>
<td>20/40MHz</td>
</tr>
<tr>
<td>Non-overlapping channels</td>
<td>3/24</td>
<td>3/24</td>
</tr>
<tr>
<td>Max. Data Rate (Mbps)</td>
<td>54</td>
<td>$150 \times N_{\text{streams}}$</td>
</tr>
<tr>
<td>Modulation</td>
<td>DSSS, CCK, OFDM</td>
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</tr>
</tbody>
</table>

- Improved Throughput and range by employing:
  - Spatial diversity: transmitting multiple streams on multiple radios
  - Higher bandwidth per channel: 40MHz (HT-40)
  - More OFDM subcarriers: 56 vs. 52
  - Shorter guard intervals: 400ns vs. 800ns
  - Higher coding rate: 5/6 vs. 3/4

- Backwards compatible with legacy 802.11a/g networks
MIMO Radio Requirements

Compared to legacy 802.11, MIMO 802.11 radios demand:

- Better error-vector magnitude (EVM)
- Tighter spectral mask requirements

Which translates to:

- Lower phase-noise
- Better I/Q matching
- Better Linearity
- Less noise

In Addition, they require

- Faster ADCs and DACs
- Less in-band ripple in the baseband filter
- Careful SoC floorplanning to avoid chain-to-chain cross-talk
- Lower power, smaller and more modular design
SoC Block Diagram
Frequency Plan

- Direct Conversion for 2.4GHz
  - Lower power signal path
  - Smaller area
  - Avoid pulling by running VCO at $4/3f_{RF}$

- Dual Conversion for 5GHz
  - Lower frequency LO circuits
  - Simplified LO generation
  - Better I/Q matching

![Diagram of frequency synthesizer with 2.4GHz and 5GHz radio frequencies]
2.4GHz Radio Block Diagram

- LNA
- Vgm
- Vgm
- PA Driver
- Cal.
- 4.8G
- \( \div 2 \)
- PA

From BB filters

5GHz receiver mixer outputs

5GHz Transmitter mixer inputs

To BB filters
5GHz Radio Block Diagram

- **2.4GHz receiver mixer outputs**
- **2.4GHz Transmitter mixer inputs**
- **to BB filters**
- **From BB filters**

- LNA
- VGA
- Vgm
- Cal.
- 3.6G
- PA
- PA Driver
- 2

- Signal flow:
  - 2.4GHz receiver mixer outputs
  - From BB filters
  - 2.4GHz Transmitter mixer inputs
5GHz Receiver Down Conversion

Measured Receiver NF = 6dB
5GHz Dual Upconversion

Diagram showing a 5GHz Dual Upconversion circuit with labels for RF mixer and IF mixer, along with input and output ports labeled as follows:

- $\frac{2}{3} f_{RF}$
- $\frac{1}{3} f_{RF}$
- $I$
- $Q$
- $in$
- $ip$
- $qn$
- $qp$
- To the PA Driver
2.4 GHz Power Amplifier
Baseband Filters

- Active R-C Implementation
- Compared to gm-C can achieve
  - Better dynamic range
  - Lower power

![Diagram of Baseband Filters](image-url)

- Baseband I-Path
- To Digital (PHY, MAC, Interface)
- 2.4GHz Rx
- 5GHz Rx
- 2.4GHz Tx
- 5GHz Tx

- DAC
- Offset Control
Baseband Filters: Receive mode

- 5th order Butterworth
  - Single-pole $I \rightarrow V$ followed by 2 biquads
  - Bandwidth adjusted using programmable capacitor arrays
Baseband Filters: Transmit mode

- 2nd order Butterworth with $f_{-3dB} = 10/20MHz$
  - More than 52dB attenuation at the DAC sampling Frequency of 160MHz
Baseband Filters: Loop-Back

- Calibrate the cutoff frequency by adjusting the biquad poles
- Test tone generated by digital baseband
Time-Interleaved SAR ADC

- Each 9-bit ADC core including T&H:
  - Dissipates 7mA from 1.2V
  - Occupies less than 0.1mm²
Voltage-Controlled Oscillator

Linear range

$V_c$

$V_{c\text{ high}}$

$V_{c\text{ low}}$

Const-IR

State Machine

control bits

$V_{c\text{ low}}$

$V_{c\text{ high}}$

$V_{c\text{ low}}$

$V_{c\text{ high}}$
SoC Calibration

- Calibration reduces the impact of analog impairments on the radio performance
- Correction algorithms are generally implemented in the digital domain
  - Lower power
  - Smaller area
  - Better reliability
- Example:
  - Receiver DC offset
  - Transmit carrier leak
  - Baseband filters bandwidth
  - Receiver I/Q mismatch
  - Receiver noise floor
  - ADC gain & DC offset
Phase Noise

@5540MHz: Integ. PN = -39.3dBc
@2462MHz: Integ. PN = -42.4dBc

2462MHz: -100dBc/Hz
5540MHz: -102dBc/Hz
5GHz Sensitivity

- Sensitivity (dBm) vs. MCS Index
- 40MHz Channels
- 20MHz Channels
- 2-streams
- Single stream
- 64QAM
- BPSK

- RF Channel Centered at 5180MHz
- No external LNA
Transmitter Performance

Channel: 2442 MHz
2-Stream HT – 40
Pout = −8dBm
EVM = −31dB

Channel: 5220 MHz
2-Stream HT – 40
Pout = −4dBm
EVM = −31.5dB
Die Micrograph

- Process: 0.13 µm CMOS
- Die Size: 6 × 6 mm²
- Analog Area: 11 mm²
- Package: 88-pin QFN
## Performance Summary

<table>
<thead>
<tr>
<th>Parameter</th>
<th>2.4GHz</th>
<th>5GHz</th>
</tr>
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<tbody>
<tr>
<td>TX EVM (HT-40, MCS 15)</td>
<td>−31dB @ -8dBm</td>
<td>−31.5dB @ −4dBm</td>
</tr>
<tr>
<td>Receiver Noise Figure</td>
<td>4dB</td>
<td>6dB</td>
</tr>
<tr>
<td>Receiver Sensitivity (HT-40, MCS15)</td>
<td>−70dBm</td>
<td>−68dBm</td>
</tr>
<tr>
<td>Integrated Phase Noise</td>
<td>−42dBc</td>
<td>−39dBc</td>
</tr>
<tr>
<td>SoC Power Dissipation (HT-40, MCS 15)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Receive</td>
<td>800mW</td>
<td>830mW</td>
</tr>
<tr>
<td>Transmit</td>
<td>630mW</td>
<td>1230mW</td>
</tr>
<tr>
<td>Transceiver Power (HT-40, MCS 15)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Receive (Incl. ADCs)</td>
<td>360mW</td>
<td>400mW</td>
</tr>
<tr>
<td>Transmit (Incl. DACs)</td>
<td>285mW</td>
<td>860mW</td>
</tr>
<tr>
<td>Over-the-air TCP throughput</td>
<td></td>
<td>205 Mbps</td>
</tr>
</tbody>
</table>
Conclusions

- Demonstrated a $2 \times 2$ MIMO SoC radio that implements the IEEE 802.11n draft
- Receiver sensitivity of $-70\text{dBm}$ and $-68\text{dBm}$ at MCS15 for 2.4GHz and 5GHz, respectively without any external LNA
- Shared Baseband filters between receiver and transmitter
- Overall analog/RF area of $11\text{mm}^2$
Acknowledgements

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