Overview of CMOS Device Behavior and Modeling for Mixed-Signal/RF Circuit Design

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Bridging the gap between IC designers and foundries
Outline

• CMOS Technology Trends
• Device Behavior Overview
• Device Modeling Challenges
• Figures of Merit and Model Validation
• Summary
CMOS Technology Trends -- Nano-scale

- CMOS has been in nanoscale era.
- Silicon CMOS is still the mainstream IC technology in the next 7-10 years before other nano devices play roles.

Source: Intel

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Semiconductor Industry (SI) Trend

PC -> Communication (wireless)

• The data of voice, video and other information will be exchanged through any media at any time and any places by wireless devices!

Intel Inside Communication Everywhere

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IC -> Application Integration

- The revenue ratio of the system chip to overall semiconductor industry will increase to 21.9% (with a total revenue of 65.6 billions) in 2008 from 16.6% in 2002.
- Product integration is to integrate different products such as smart phone, camera, cell phone, PDA, TV, music player, based on one platform such as cell phone.
- The integration of end market will be the merge of markets such as computer, consumer, wired and wireless communications.
CMOS Technology Trends -- RF CMOS

- Recent speed improvements and better noise behavior of CMOS transistors have made it feasible to implement RF circuits for wireless products, such as cell phones, Global Positioning System, and Bluetooth.

- CMOS is one of the best suitable technologies to integrate RF circuits with analog and base-band digital circuits.

- Tremendous research effort is dedicated to RF CMOS, driven by System-on-Chip (SoC).

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**CMOS:**
- High integration density
- High yield
- Low power consumption
- Low cost

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An Illustration of RF SoC on CMOS

• RF SoC - Integrate a chipset system onto a same chip:
  • RF Front End (RFFE)
  • Analog Based-band (ABB)
  • Power Management and Audio Codecs (PMAC)
  • Digital Base-band (DBB)

• RFCMOS implementation challenges:
  • low cost
  • high performance

Design IC in Nano-scale/RF Era

Need to Well Understand the Device Behavior in Advanced Technology Nodes

Need to Develop Physical and Accurate Device Models for RF/Analog Design
Today’s MOSFETs show high $f_t$ and low NF

Leakage in Different Technology Node

- Leakage increases significantly as technology advances.

**MOSFET Gate Leakage**


- In today’s MOSFETs, gate leakage increases by orders for the decrease of Tox
$I_{D_{sat}}/I_{off}$ Universal Curves

- A trade-off between $I_{D_{sat}}$ and $I_{off}$.
- Better device design and material selection to reduce the slope of the universal curves.
Layout Dependent Device Performance

- Effects different to nfet and pfet.
- Impact both digital (changing drive current) and analog (changing both Gm and matching).


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Irregular device layouts are used in digital (even analog) cell libraries.

The layouts of the devices in the cell libraries may be different from those for device modeling.

• Parasitic components need to be well understood at HF.
HF Behavior: Effective $R_g$

- Effective $R_g$ extracted by:

$$R_g = \frac{\text{Re}\{Y_{12}\}}{\text{Im}\{Y_{11}\} \text{Im}\{Y_{12}\}}$$

- Effective $R_g$ does not follow equation below when $L_f$ is long:

$$R_{G,\text{poly}} = \frac{R_{Gsh}}{Nf L_f} (W_{ext} + \frac{W_f}{\alpha})$$

- Significant increase in effective $R_g$ due to non-quasi-static (NQS) effect.

HF Behavior: NQS Effects (1)

- Effective \( G_m, \) normalized:
  \[
  G_m, \text{ normalized} = \frac{\text{Re}(Y_{21})}{\text{Re}(Y_{21}(f_0))}
  \]

- Short \( L, \) \( G_m \) is “constant” over \( f. \)

- Longer \( L, \) \( G_m \) becomes frequency dependent;

The longer the \( L, \) the stronger the frequency dependence.

HF Behavior: NQS Effects (2)

- Effective Gate Capacitance $C_{gg,eff}$:

$$C_{GG, eff} = \left| \frac{\text{Im}\{Y_{11}\}}{\omega} \right|$$

- Short $L$, $C_{gg,eff}$ is "constant" over $f$.

- Longer $L$, $C_{gg,eff}$ becomes frequency dependent.

- The longer the $L$, the stronger the frequency dependence.

HF Behavior: Substrate Coupling

- At HF, signal is coupled to substrate through junction capacitance.
- This effect impacts primarily the output impedance.
HF Behavior: Bias and f Dependence of $R_{sub}$

- Substrate resistance is a very weak function of biases at the gate and drain.
- Up to 10GHz, substrate resistance is not sensitive to frequency.

HF Behavior: Thermal Noise

- HF noise reduces as the technology advances (and shorter L).
- Higher Gm, lower HF noise.
- Low Nf (<1dB) can be obtained at normal gate biases.

HF Behavior: Induced Gate Noise

Channel noise is frequency independent and induced gate noise is frequency dependent.

Induced gate noise is not negligible in devices with long $L$ or devices with short $L$ but at very high frequency.

HF Behavior: High “Low Frequency Limit”


• MOSFET has much higher “low frequency limit” (LFL)
• HF distortion characteristics (<f_{LFL}) can be described by its low-frequency behavior
Device Modeling for RF Applications

• Device Modeling at HF should at least include the modeling for:
  - MOSFET
  - Passive devices (R, C, inductor, varactors)
  - Special devices (LDMOS and PNP BJTs)
  - Interconnect
  - Substrate
  - Circuit blocks (behavior modeling)

• Today, we will mainly talk about MOSFET modeling.
MOSFET Modeling Challenges

• Core model with good continuity, accuracy and scalability over wide biases, temperatures and geometries.

• Modeling of classic well-known short channel and narrow width effects and recent advanced physical effects such as velocity overshoot, self-heating, channel charge quantization, tunneling, layout dependent behavior, ...

• Scalable parasitic capacitance and resistance models.

• Predicts accurately the small signal AC and noise and the distortion behavior.

• Non-quasi static (NQS) effects.

• Statistical modeling
Modeling Challenges – $G_m$ & $G_m/ID$  

- $G_m$, the most important parameters in analog design.
- $G_m/ID$, a universal characteristic of MOSFETs to evaluate the transconductance efficiency.
- Inversion Coefficient (IC), ratio of $I_D/I_S$, is proposed as a measure of MOS inversion level.

(Yuhua Cheng, "A study of figures of merit for the high frequency behavior of MOSFETs in RF IC applications", Eighth International Conference on modeling and Simulation of Microsystems, Anaheim, May 8-12, 2005)
Modeling Challenges - Capacitance

- Gate Capacitance is not constant in strong inversion.
- Bias dependence is caused by Poly-depletion effect.
- Both poly-depletion (PD) and channel quantization (CQ) effects will impact Cgg.

(Yuhua Cheng et al., "ICM-an analytical inversion charge model for accurate modeling of thin gate oxide MOSFETs,” Simulation of semiconductor Processes and Devices, Page(s) 109 -112, 1997.)
Modeling Challenges – Scalable Rsub

- $R_{sub}$ should be scalable in terms of channel width, length and fingers.
- All parameters should be extracted easily.

Modeling Challenges - NQS Effects

- NQS will significantly impact $Y_{11}$ and $Y_{21}$ behavior.

- Many approaches are proposed to model this effect:
  - Multi-segment approach
  - Relaxation time
  - $R_g/R_i$ equivalent circuit approach

- Efficient built-in NQS effect in intrinsic core model is preferred.

Modeling of Flicker noise

• Downscaling may degrade flicker noise behavior.
• Modeling of flicker noise in nano-scale devices becomes more challenging.
• Accurate prediction of corner frequency, $F_{\text{corner}}$, is critical for circuit design.

(Yuhua Cheng, "A study of figures of merit for the high frequency behavior of MOSFETs in RF IC applications", Eighth International Conference on modeling and Simulation of Microsystems, Anaheim, May 8-12, 2005)
• Parasitic resistance at gate, source, drain and substrate generate thermal noise
• Channel thermal noise is the dominant noise source at HF.
• Understanding of noise sources is important.
• Modeling of channel thermal noise and induced gate noise is the most challenging job.
Statistical Modeling

- Process variation (even within a wafer) in today’s advanced technologies becomes more significant.

- Need physical statistical models to predict process variation and local mismatch to optimize analog/RF circuits with high yield.

- Correlations between statistical modeling with considerations of both frontend and backend process variations and yield modeling/prediction should be developed.

- In nano-scale technologies, statistical model is more meaningful than traditional corner models.
RF Modeling in Nano-scale Era

Continuity  Scalability  Accuracy

New Physical Effects  Computation Efficiency

Modeling of Small Signal, Noises, Large Signal Distortion For RF Applications
$G_m/I_D$: Measured vs. Fitted

(Yuhua Cheng, "A study of figures of merit for the high frequency behavior of MOSFETs in RF IC applications", Eighth International Conference on modeling and Simulation of Microsystems, Anaheim, May 8-12, 2005)

- $G_m/I_D$ has been proposed a FoM for model validation for analog applications.

(Yuhua Cheng, Bridging the gap between IC designers and foundries)
**$f_T$: Measured vs. Fitted**

- **A standard device parameter for model validation.**
- **However, only $f_T$ is not enough to describe HF behavior of MOSFETs, especially at technology nodes such as 0.13um and below.**


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$G_{\text{max}}$ and $f_{\text{max}}$: Measured vs. Fitted

- $f_{\text{max}}$ contains the impacts from parasitics such as gate and substrate resistance and is a better FoM than $f_T$.

(Yuhua Cheng, "A study of figures of merit for the high frequency behavior of MOSFETs in RF IC applications", Eighth International Conference on modeling and Simulation of Microsystems, Anaheim, May 8-12, 2005)
C-parameters: Modeled vs. Fitted

- C-parameters are more sensitive to the bias dependence of gate resistance and capacitance.
- Useful FoMs for model validation.

(Yuhua Cheng, "A study of figures of merit for the high frequency behavior of MOSFETs in RF IC applications", Eighth International Conference on modeling and Simulation of Microsystems, Anaheim, May 8-12, 2005)
Large Signal Behavior: Measured vs. Fitted

Below certain (the “LFL”) frequency, the distortion behavior of MOSFETs is primarily determined by transconductance and capacitances.

With careful parameter extraction at DC and HF small signal, a model can well predict the large signal distortion behavior.

Something worth mentioning in RF Modeling

Validate Models Based On Meaningful Figures-of-Merit
Summary

• While all the requirements for continuity, scalability, accuracy and computation efficiency need to be met for device models for circuit simulation, the new physical effects in nano-scale devices make compact model development very challenging.

• A lot of additional modeling efforts to predict HF noise and large signal distortion behavior are needed for RF circuit design.

• It would be desirable in the future the modelers use certain FoMs at HF to qualify the device models targeted for analog/RF applications.

• Device modeling has become very critical component in the technology platform for RF SOC design in nano-scale technologies.
Thank you for your attention